

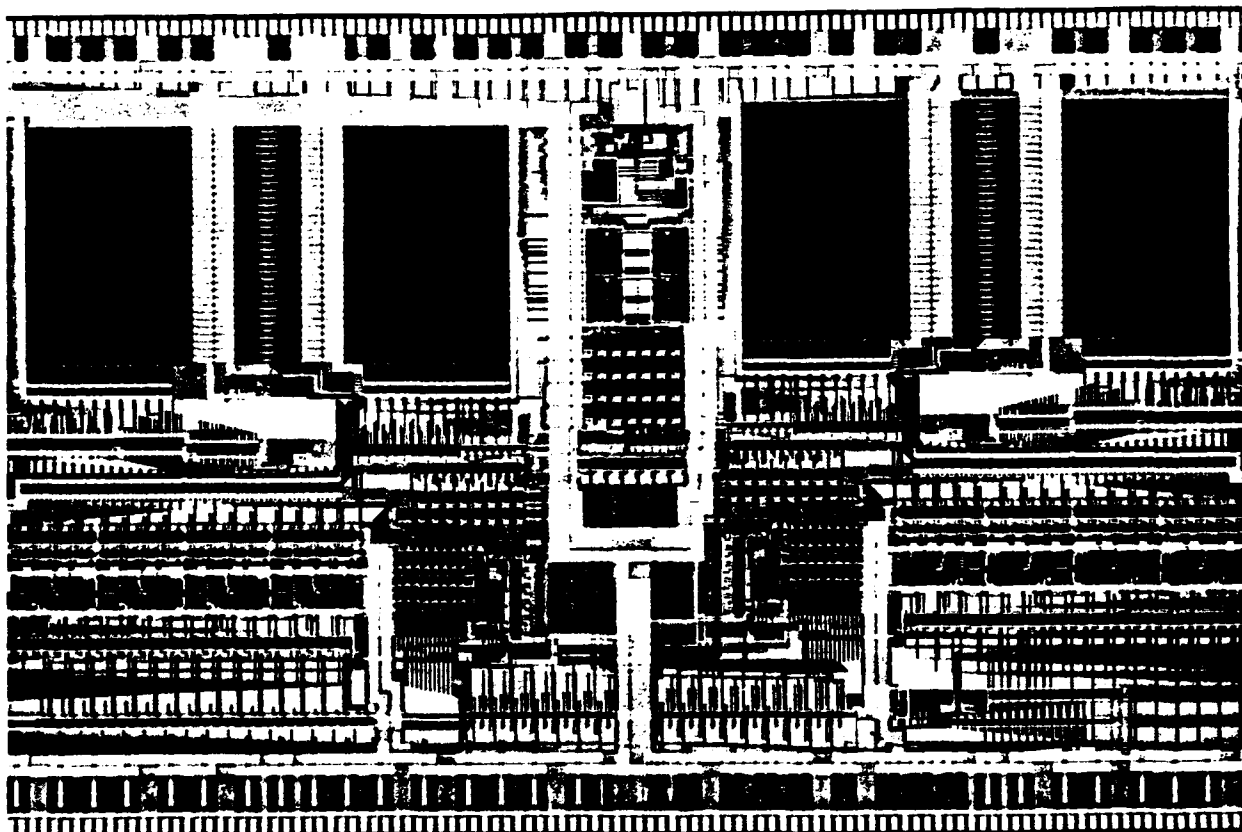


Project : Insertion Demonstrations of Digital Gallium Arsenide

CDRL Item A001

# OBP-80 FINAL TECHNICAL REPORT

## Volume 1/4 - Chip Set Schematics



Prepared for:

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## GLOSSARY

AALU	Address Arithmetic Logic Unit
ALU	Arithmetic Logic Unit
APG	Automatic Pattern Generation
ASIC	Application Specific Integrated Circuit
BCU	Bus Control Unit
BLM	Behavioral Language Model
CB	Communications Buffer
CDR	Critical Design Review
CMOS	Complementary Metal Oxide Semiconductor
CMOS/SOS	Complementary Metal Oxide Semiconductor/Silicon on Sapphire
CPU	Central Processing Unit
DALU	Data Arithmetic Logic Unit
DARPA	Defense Advanced Research Projects Administration
DC	Direct Current
DMSP	Defense Meteorological Satellite Program
DSP	Digital Signal Processing
FET	Field Effect Transistor
FIFO	First In First Out
FMEA	Failure Mode Effects Analysis
EDM	Engineering Development Model
GALU	Generic Arithmetic Logic Unit
GaAs	Gallium Arsenide
GTE	Ground Test Equipment
GFP	Government Furnished Property
I/O	Input/Output
IR&D	Independent Research and Development
MCS	Microcode Sequencer
MESFET	Metal Semiconductor Field Effect Transistor
MOPS	Million Operations Per Second
MOS	Metal Oxide Semiconductor
MPY	Multiplier Unit
MTBF	Mean Time Between Failures
NMOS	N channel Metal Oxide Semiconductor
NRL	Naval Research Laboratory
OBP	On Board Processor
OBP-80	On Board Processor - 80 MHz
OTS	Off The Shelf
PC	Personal Computer
PCA	Parts Characterization Analyzer
PCB	Printed Circuit Board
PDR	Preliminary Design Review
PIC	Priority Interrupt Controller
PS	Pipeline Slice
Qc	Critical Charge

**Insertion Demonstrations of Digital Gallium Arsenide  
VLSI Design Laboratory Glossary #2 V1.**

**Revised: 16 Jul 91**

<b>RAM</b>	<b>Random Access Memory</b>
<b>SEU</b>	<b>Single Event Upset</b>
<b>SSI</b>	<b>Small Scale Integration</b>
<b>TMA</b>	<b>Timing Margin Analysis</b>
<b>TTL</b>	<b>Transistor - Transistor Logic</b>
<b>VLSI</b>	<b>Very Large Scale Integration</b>
<b>WBS</b>	<b>Work Breakdown Structure</b>
<b>WCA</b>	<b>Worst Case Analysis</b>
<b>WCS</b>	<b>Writable Control Store</b>
<b>WS</b>	<b>Working Store</b>

Statement A per telecon  
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**APPLICABLE DOCUMENTS:**

1. 'OBP ASSEMBLER USER'S MANUAL', Document ID = SSD-D-AS239, Item A016, Naval Research Laboratory.
2. 'OBP LINKER USER'S MANUAL', Document ID = SSD-D-AS239, Item A015, Naval Research Laboratory.
3. 'PAYLOAD DATA MANAGEMENT SYSTEM OBP-CPU PROGRAMMER'S REFERENCE MANUAL', Document ID = OB87A014-3, Item A014, Naval Research Laboratory.
4. 'Schematic Diagram - CPU', Document ID = AS-OP-5395, Naval Research Laboratory.
5. OBP80 Final Technical Report, Vol 1-4, Document ID = 849GOBP0100, Martin Marietta Defense Space & Communications.



## **FOREWORD**

The OBP-80 is an Engineering Development Model (EDM) of a bit slice computer constructed by Martin Marietta Space Systems for the Naval Research Laboratory. The work described in this report was performed under contract N00014-89-C-2169, Insertion Demonstrations of Digital Gallium Arsenide - OBP Upgrade. The contract was performed in cooperation with the Defense Advanced Research Projects Agency technology insertion program for digital gallium arsenide.

This system has been developed to demonstrate, in a laboratory environment, an architecture that can be used to perform advanced signal processing functions onboard a spacecraft. Primary emphasis is placed on the transfer of an existing CMOS architecture to a higher performance, more radiation tolerant technology of Gallium Arsenide.

The following individuals provided technical direction and assistance:

Dr. Andrew J. Fox, Head, Advanced Systems Technology Branch, NRL  
Dr. Arati Prabhakar, Director, Defense Sciences Office, DARPA  
Dr. Alan Ross, Architecture Consultant

IDDGA Final Technical Report Volume 1 of 4 contains the chip set schematic diagrams.

This volume provides the schematic data which was used to generate the physical design of all seven VLSI components used in the OBP-80 EDM. It also presents top level graphical representations of the seven components. This data is provided as an aid to post-fabrication analysis.

The complete final technical report is composed of the following volumes:

Final Technical Report - Volume 1 of 4: Chip Set Schematic Diagrams

Final Technical Report - Volume 2 of 4: Chip Set Source Control Drawings

Final Technical Report - Volume 3 of 4: EDM Board Schematic Diagrams

Final Technical Report - Volume 4 of 4: OBP80 Software Model

## 1. INTRODUCTION

The OBP80 chip set is composed of the following circuits:

TABLE 1 OBP80 Chip Set Summary

DEVICE	PACKAGE	TRANSISTOR COUNT	EQUIVALENT GATES	POWER	I/O	MASK REVISION
GOBP001 - MPY VLSI	LDCC 256	27,105	9,035	3.35 W	43 GND, 27 VTT, 136 GaAs signal	Rev. A 7/15/91
GOBP002 - GALU VLSI	LDCC 344	73,564	24,521	6.6 W	80 GND, 36 VTT, 214 GaAs signal	Initial 3/15/91
GOBP003 - IPR VLSI	LDCC 344	26,600	8,867	4.4 W	64 GND, 24 VTT, 5 VREF, 112 ECL signal, 136 GaAs signal	Rev. A 7/30/91
GOBP004 - DMC VLSI	LDCC 344	14,887	4,962	2.95 W	77 GND, 31 VTT, 4 VREF, 102 ECL signal, 105 GaAs signal	Initial 3/15/91
GOBP005 - TICVLSI	LDCC 256	14,750	4,916			Initial 7/30/91
GOBP006 - COMM1 VLSI	LDCC 256	15,780	5,260		41 GND, 26 VTT, 15 PLUS5, 92 GaAs signal, 81 TTL signal	Initial 7/15/91
GOBP007 MCS VLSI	LDCC 344	37,094	12,364			Initial 8/15/91

The schematic diagrams provided in this manual are in Mentor Graphics Corporation format. The schematics provide a method for controlling design hierarchy within a CAE environment. Consequently, they do not resemble conventional 'flat' schematics very closely.

The designs are organized to help the reader quickly trace the hierarchy from top to bottom. The first sheet of each section contains a photomicrograph of the device with the major macrocells labeled. Following this header page, the integrated circuit macrocell symbols and schematics are presented alphabetically.

The macrocells are always presented in two pages. The macrocell symbol occurs first, and is always followed by a page schematic. The only exception to this is the representation of the complete chip. Here, the first page is always the chip symbol. This is followed by a two sheet schematic. The first sheet serves as a block diagram of entire chip and the second schematic

page is exclusively reserved for I/O cells. The cells may be traced downward to transistor equivalents by indexing each macrocell element that occurs in the block diagram schematic.

A good example might be the Data Memory Controller, DMC. Consider the top level schematic of the DMC shown in Figure 1. In this figure, the arrow tails and heads represent sheet to sheet connections. Since sheet 2 contains only I/O cells, these signals are identified as primary inputs and outputs respectively. Figure 2 is used to confirm this, and to identify the voltage level of the interface (TTL, MM GaAs, ECL 100K).

Suppose one is concerned with the functionality or the timing of a particular logic block. Any functional block encountered in the schematics may be expanded for logic simulation, VSPICE simulation, or comparison with layout. To investigate the effects of loading on the 'Q' output of the DMA register shown in Figure 1, it is necessary to lookup the macrocell 'VOTEREG16' towards the rear of the DMC schematics.

Once there, it is easy to see that the 'VOTEREG16' macrocell is composed of 16 occurrences of 'VOTEBIT' and one occurrence of 'VOTEBUF'. Since the 'VOTEBUF' circuit appears to be buffering only the inputs, the output drive for the DMA register comes from the 'VOTEBIT' macrocell. Figure 3 shows the 'VOTEREG16' cell.

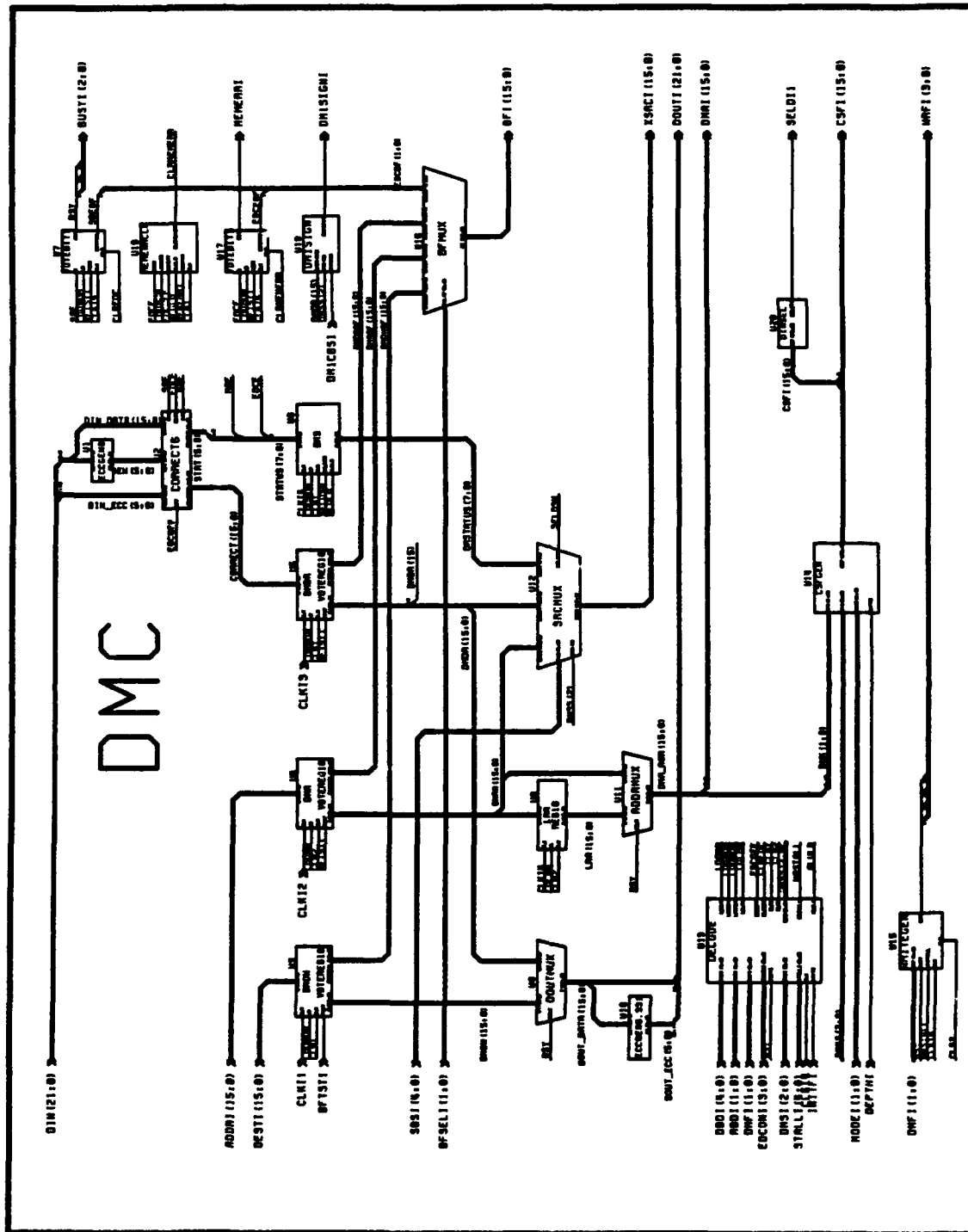


Figure 1 DMC Schematic Diagram, Page 1/2

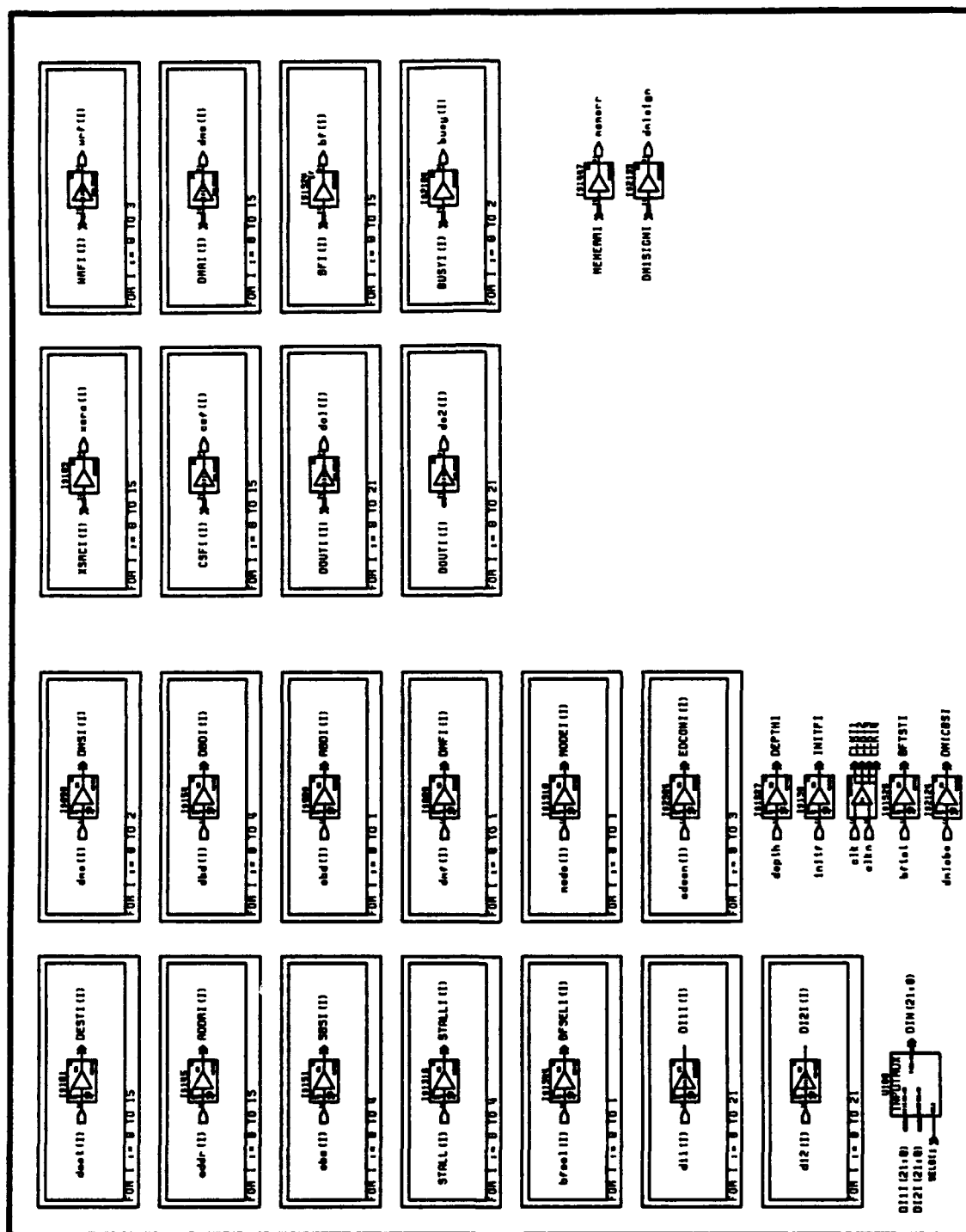


Figure 2 DMC Schematic Diagram, Page 2/2

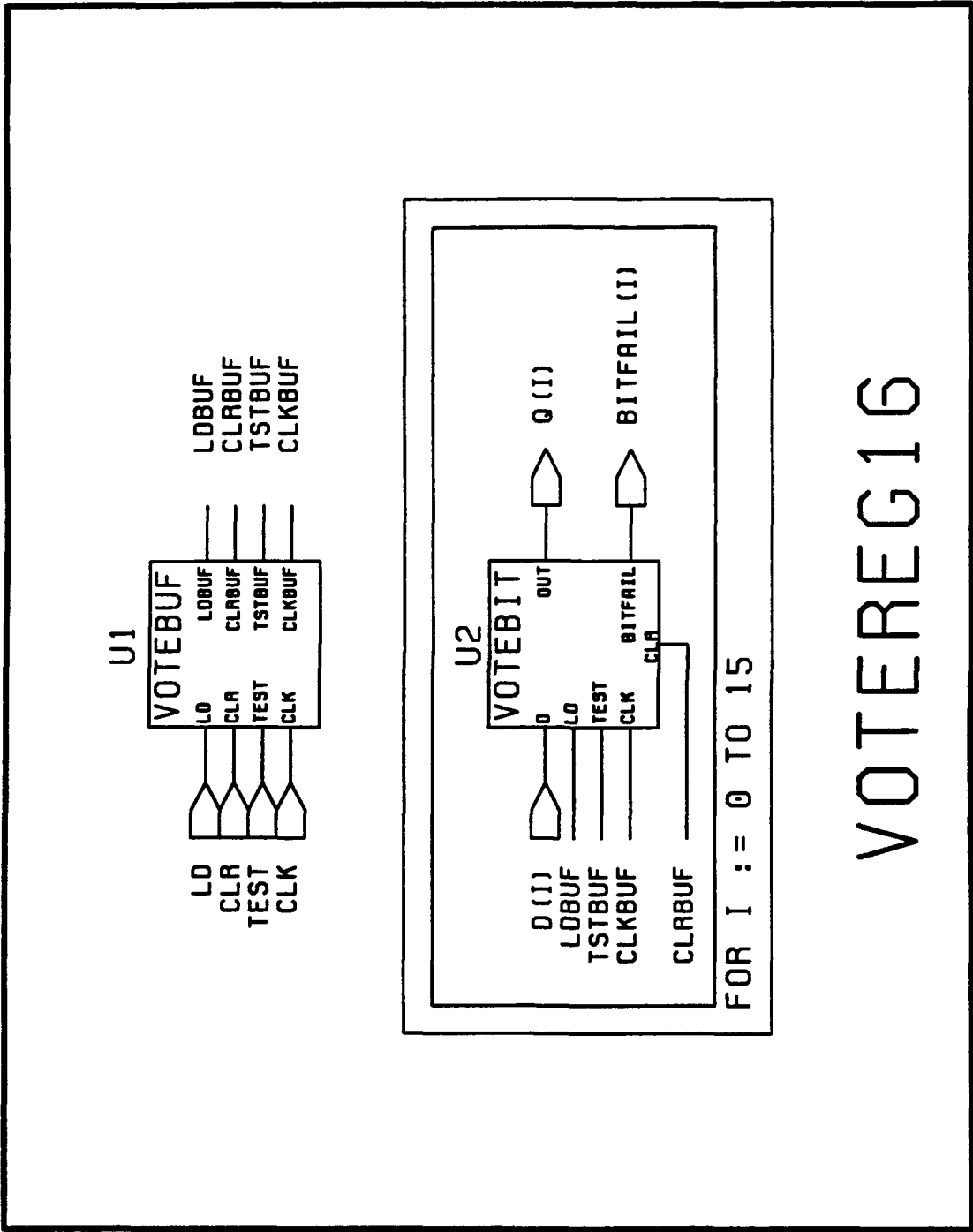


Figure 3 VOTEREG Macrocell Schematic Diagram

To locate the actual output drive capability of the 'VOTE BIT' macrocell, it is necessary to back up several pages in the alphabetized macrocell listing of schematics. Figure 4 at last locates the driver circuit for the DMA register. It is important to note that the feedback path load must also be added into the output delay.

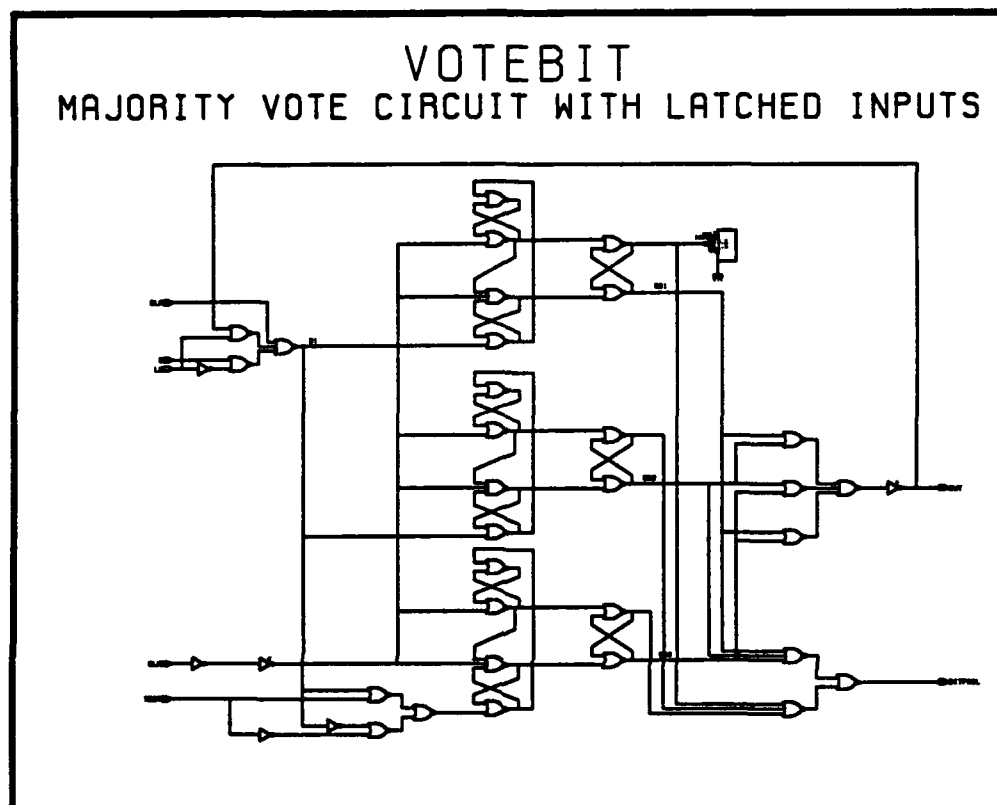


Figure 4 VOTE BIT Macrocell Schematic Diagram

The inverter output stage has the necessary properties attached to the symbol to determine the length/width ratio. A blowup of the inverter reveals that the output stage is actually a superinverter. This is seen by the 'S' designator shown on the inverter symbol in Figure 5. This symbol specifies the transistor topology shown in Figure 6.

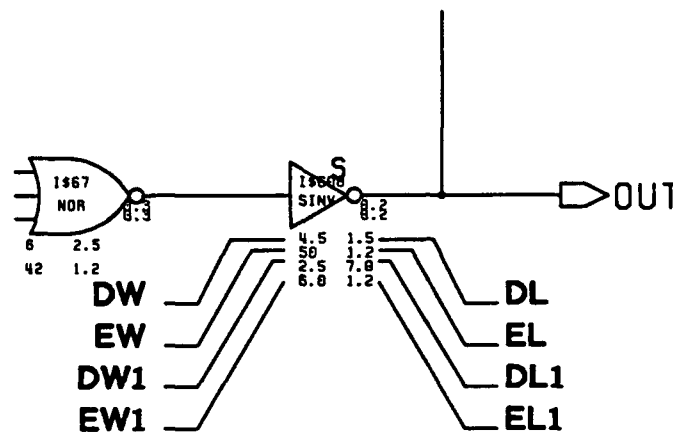


Figure 5 VOTEBIT Output Drive Inverter

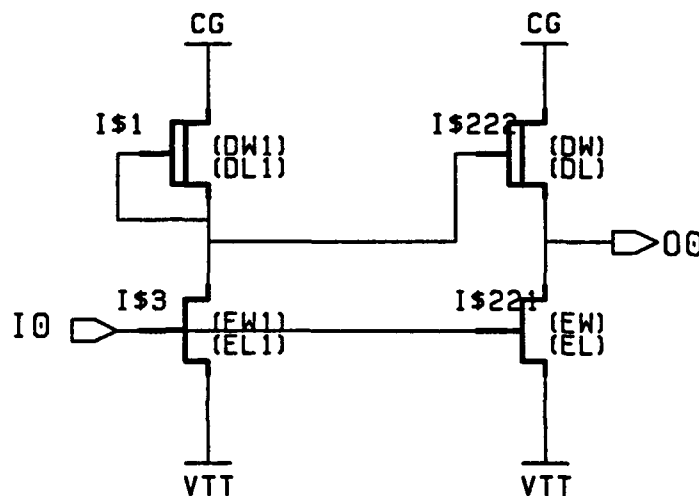


Figure 6 GaAs Super-Inverter Schematic

From Figures 5 and 6, it is easy to see the 'as-built' sizes of the transistors used in the super buffer. In a hierarchical schematic, the FET sizes are handed down to a generic super-inverter topology. The format is always that the widths appear on the left side of the symbol, and the lengths on the right. The depletion transistors always appear on top of the enhancements.

From the 'VOTEBIT' circuit directly, we can extract a VSPICE netlist. This was done using the Martin Marietta utilities mexpand and vspicenet. This produces only a netlist of the circuit. Figure 7 illustrates the generated netlist. The length of the circuit results directly from the number of transistors in 'VOTEBIT'. These can be summarized from:



```
* VSPICE netlist for VOTEBIT
*
* VOTEBIT SEU simulation 3/23/91
*
.MODEL ENH NGAAS (KIND=1)
.MODEL DEP NGAAS (KIND=4)
* power sources
VGND 1 0 -1.9
* circuit load
C1 538 546 2.2PF
B200 546 538 546 546 ENH W=50 L=1.2
B201 546 51 546 546 ENH W=50 L=1.2
* seu current pulse
ISEU 546 700 PULSE(.005P,0.6M,1NS,10P,10P,90P,10N)
VSEU 514 700 0
* zero value voltage sources
VCG 0 545 0
VTT 1 546 0
VCLR 53 0 -1.9
VLD 56 0 -1.9
VD 54 0 -1.9
VCLK 52 0 -1.4
VTST 542 0 -1.9
* initial conditions
.NODESET V(535) = -1.4 V(538) = -1.9
.NODESET V(522) = -1.4 V(55) = -1.9
.NODESET V(529) = -1.9 V(536) = -1.9
.NODESET V(530) = -1.9 V(539) = -1.4
.NODESET V(540) = -1.4 V(541) = -1.4
.NODESET V(526) = -1.9 V(527) = -1.9
.NODESET V(59) = -1.9 V(512) = -1.4
.NODESET V(515) = -1.4 V(524) = -1.4
.NODESET V(523) = -1.9 V(520) = -1.4
.NODESET V(57) = -1.9 V(58) = -1.4
*.NODESET V(51) = -1.9 V(510) = -1.9
.NODESET V(514) = -1.9 V(517) = -1.9
.NODESET V(528) = -1.9 V(518) = -1.4
.NODESET V(531) = -1.9 V(532) = -1.4
.NODESET V(543) = -1.85 V(544) = -0.6
.NODESET V(533) = -1.9 V(537) = -1.9
* SPICE Net List Extracted for Votebit
B1 532 55 546 546 ENH W=14 L=1.2
B2 532 532 545 546 DEP W=2 L=2.5
B3 525 542 546 546 ENH W=14 L=1.2
B4 525 525 545 546 DEP W=2 L=2.5
B5 534 56 546 546 ENH W=14 L=1.2
B6 534 534 545 546 DEP W=2 L=2.5
B7 537 52 546 546 ENH W=28 L=1.2
B8 537 537 545 546 DEP W=4 L=2.5
B9 51 57 546 546 ENH W=35 L=1.2
B10 51 58 546 546 ENH W=35 L=1.2
B11 51 51 545 546 DEP W=5 L=2.5
B12 529 539 546 546 ENH W=21 L=1.2
B13 529 540 546 546 ENH W=21 L=1.2
```

Figure 7 Extracted VSPICE Netlist for Votebit

B14	529	529	545	546	DEP W=3 L=2.5
B15	536	540	546	546	ENH W=21 L=1.2
B16	536	541	546	546	ENH W=21 L=1.2
B17	536	536	545	546	DEP W=3 L=2.5
B18	530	539	546	546	ENH W=21 L=1.2
B19	530	541	546	546	ENH W=21 L=1.2
B20	530	530	545	546	DEP W=3 L=2.5
B21	526	511	546	546	ENH W=28 L=1.2
B22	526	539	546	546	ENH W=28 L=1.2
B23	526	526	545	546	DEP W=4 L=2.5
B24	539	526	546	546	ENH W=42 L=1.2
B25	539	514	546	546	ENH W=42 L=1.2
B26	539	539	545	546	DEP W=6 L=2.5
B27	527	516	546	546	ENH W=28 L=1.2
B28	527	540	546	546	ENH W=28 L=1.2
B29	527	527	545	546	DEP W=4 L=2.5
B30	540	527	546	546	ENH W=42 L=1.2
B31	540	528	546	546	ENH W=42 L=1.2
B32	540	540	545	546	DEP W=6 L=2.5
B33	59	519	546	546	ENH W=28 L=1.2
B34	59	541	546	546	ENH W=28 L=1.2
B35	59	59	545	546	DEP W=4 L=2.5
B36	541	59	546	546	ENH W=42 L=1.2
B37	541	531	546	546	ENH W=42 L=1.2
B38	541	541	545	546	DEP W=6 L=2.5
B39	510	512	546	546	ENH W=21 L=1.2
B40	510	511	546	546	ENH W=21 L=1.2
B41	510	510	545	546	DEP W=3 L=2.5
B42	511	510	546	546	ENH W=35 L=1.2
B43	511	513	546	546	ENH W=35 L=1.2
B44	511	511	545	546	DEP W=5 L=2.5
B45	512	514	546	546	ENH W=21 L=1.2
B46	512	55	546	546	ENH W=21 L=1.2
B47	512	512	545	546	DEP W=3 L=2.5
B48	517	515	546	546	ENH W=21 L=1.2
B49	517	516	546	546	ENH W=21 L=1.2
B50	517	517	545	546	DEP W=3 L=2.5
B51	516	517	546	546	ENH W=35 L=1.2
B52	516	513	546	546	ENH W=35 L=1.2
B53	516	516	545	546	DEP W=5 L=2.5
B54	515	528	546	546	ENH W=21 L=1.2
B55	515	55	546	546	ENH W=21 L=1.2
B56	515	515	545	546	DEP W=3 L=2.5
B57	518	520	546	546	ENH W=21 L=1.2
B58	518	519	546	546	ENH W=21 L=1.2
B59	518	518	545	546	DEP W=3 L=2.5
B60	519	518	546	546	ENH W=35 L=1.2
B61	519	513	546	546	ENH W=35 L=1.2
B62	519	519	545	546	DEP W=5 L=2.5
B63	520	531	546	546	ENH W=21 L=1.2
B64	520	533	546	546	ENH W=21 L=1.2
B65	520	520	545	546	DEP W=3 L=2.5
B66	533	524	546	546	ENH W=14 L=1.2
B67	533	523	546	546	ENH W=14 L=1.2

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

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B68 533 533 545 546 DEP W=2 L=2.5
B69 524 55 546 546 ENH W=14 L=1.2
B70 524 542 546 546 ENH W=14 L=1.2
B71 524 524 545 546 DEP W=2 L=2.5
B72 523 532 546 546 ENH W=14 L=1.2
B73 523 525 546 546 ENH W=14 L=1.2
B74 523 523 545 546 DEP W=2 L=2.5
B75 522 538 546 546 ENH W=14 L=1.2
B76 522 56 546 546 ENH W=14 L=1.2
B77 522 522 545 546 DEP W=2 L=2.5
B78 521 54 546 546 ENH W=14 L=1.2
B79 521 534 546 546 ENH W=14 L=1.2
B80 521 521 545 546 DEP W=2 L=2.5
B81 543 535 546 546 ENH W=6.0 L=1.2
B82 538 535 546 546 ENH W=50 L=1.2
B83 543 543 545 546 DEP W=2.5 L=7.0
B84 538 543 545 546 DEP W=4.5 L=1.5
B85 544 537 546 546 ENH W=6.0 L=1.2
B86 513 537 546 546 ENH W=50 L=1.2
B87 544 544 545 546 DEP W=2.5 L=7.0
B88 513 544 545 546 DEP W=4.5 L=1.5
B89 535 529 546 546 ENH W=42 L=1.2
B90 535 536 546 546 ENH W=42 L=1.2
B91 535 530 546 546 ENH W=42 L=1.2
B92 535 535 545 546 DEP W=6 L=2.5
B93 57 539 546 546 ENH W=14 L=1.2
B94 57 540 546 546 ENH W=14 L=1.2
B95 57 541 546 546 ENH W=14 L=1.2
B96 57 57 545 546 DEP W=2 L=2.5
B97 58 526 546 546 ENH W=14 L=1.2
B98 58 527 546 546 ENH W=14 L=1.2
B99 58 59 546 546 ENH W=14 L=1.2
B100 58 58 545 546 DEP W=2 L=2.5
B101 514 511 546 546 ENH W=28 L=1.2
B102 514 513 546 546 ENH W=28 L=1.2
B103 514 512 546 546 ENH W=28 L=1.2
B104 514 514 545 546 DEP W=4 L=2.5
B105 528 516 546 546 ENH W=28 L=1.2
B106 528 513 546 546 ENH W=28 L=1.2
B107 528 515 546 546 ENH W=28 L=1.2
B108 528 528 545 546 DEP W=4 L=2.5
B109 531 519 546 546 ENH W=28 L=1.2
B110 531 513 546 546 ENH W=28 L=1.2
B111 531 520 546 546 ENH W=28 L=1.2
B112 531 531 545 546 DEP W=4 L=2.5
B113 55 53 546 546 ENH W=35 L=1.2
B114 55 522 546 546 ENH W=35 L=1.2
B115 55 521 546 546 ENH W=35 L=1.2
B116 55 55 545 546 DEP W=5 L=2.5
B117 546 526 546 546 DEP W=3.5 L=1.5
***** LIST OF MODELS USED *****
*
* ENH
* DEP
*

```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

\* LIST OF REPLACED NAMES.

\*  
\* I\$592/I\$3/B1 ==> B1  
\* I\$592/I\$1/B1 ==> B2  
\* I\$1263/I\$3/B1 ==> B3  
\* I\$1263/I\$1/B1 ==> B4  
\* I\$1261/I\$3/B1 ==> B5  
\* I\$1261/I\$1/B1 ==> B6  
\* I\$901/I\$3/B1 ==> B7  
\* I\$901/I\$1/B1 ==> B8  
\* I\$106/I\$3/B1 ==> B9  
\* I\$106/I\$2/B1 ==> B10  
\* I\$106/I\$1/B1 ==> B11  
\* I\$57/I\$3/B1 ==> B12  
\* I\$57/I\$2/B1 ==> B13  
\* I\$57/I\$1/B1 ==> B14  
\* I\$58/I\$3/B1 ==> B15  
\* I\$58/I\$2/B1 ==> B16  
\* I\$58/I\$1/B1 ==> B17  
\* I\$59/I\$3/B1 ==> B18  
\* I\$59/I\$2/B1 ==> B19  
\* I\$59/I\$1/B1 ==> B20  
\* I\$20/I\$3/B1 ==> B21  
\* I\$20/I\$2/B1 ==> B22  
\* I\$20/I\$1/B1 ==> B23  
\* I\$19/I\$3/B1 ==> B24  
\* I\$19/I\$2/B1 ==> B25  
\* I\$19/I\$1/B1 ==> B26  
\* I\$37/I\$3/B1 ==> B27  
\* I\$37/I\$2/B1 ==> B28  
\* I\$37/I\$1/B1 ==> B29  
\* I\$36/I\$3/B1 ==> B30  
\* I\$36/I\$2/B1 ==> B31  
\* I\$36/I\$1/B1 ==> B32  
\* I\$52/I\$3/B1 ==> B33  
\* I\$52/I\$2/B1 ==> B34  
\* I\$52/I\$1/B1 ==> B35  
\* I\$51/I\$3/B1 ==> B36  
\* I\$51/I\$2/B1 ==> B37  
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\* I\$1144/I\$3/B1 ==> B48  
\* I\$1144/I\$2/B1 ==> B49  
\* I\$1144/I\$1/B1 ==> B50  
\* I\$586/I\$3/B1 ==> B51  
\* I\$586/I\$2/B1 ==> B52

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

```
* I$586/I$1/B1 ==> B53
* I$585/I$3/B1 ==> B54
* I$585/I$2/B1 ==> B55
* I$585/I$1/B1 ==> B56
* I$1146/I$3/B1 ==> B57
* I$1146/I$2/B1 ==> B58
* I$1146/I$1/B1 ==> B59
* I$590/I$3/B1 ==> B60
* I$590/I$2/B1 ==> B61
* I$590/I$1/B1 ==> B62
* I$589/I$3/B1 ==> B63
* I$589/I$2/B1 ==> B64
* I$589/I$1/B1 ==> B65
* I$114/I$3/B1 ==> B66
* I$114/I$2/B1 ==> B67
* I$114/I$1/B1 ==> B68
* I$112/I$3/B1 ==> B69
* I$112/I$2/B1 ==> B70
* I$112/I$1/B1 ==> B71
* I$113/I$3/B1 ==> B72
* I$113/I$2/B1 ==> B73
* I$113/I$1/B1 ==> B74
* I$596/I$3/B1 ==> B75
* I$596/I$2/B1 ==> B76
* I$596/I$1/B1 ==> B77
* I$595/I$3/B1 ==> B78
* I$595/I$2/B1 ==> B79
* I$595/I$1/B1 ==> B80
* I$608/I$3/B1 ==> B81
* I$608/I$221/B1 ==> B82
* I$608/I$1/B1 ==> B83
* I$608/I$222/B1 ==> B84
* I$605/I$3/B1 ==> B85
* I$605/I$221/B1 ==> B86
* I$605/I$1/B1 ==> B87
* I$605/I$222/B1 ==> B88
* I$67/I$3/B1 ==> B89
* I$67/I$2/B1 ==> B90
* I$67/I$261/B1 ==> B91
* I$67/I$1/B1 ==> B92
* I$101/I$3/B1 ==> B93
* I$101/I$2/B1 ==> B94
* I$101/I$261/B1 ==> B95
* I$101/I$1/B1 ==> B96
* I$102/I$3/B1 ==> B97
* I$102/I$2/B1 ==> B98
* I$102/I$261/B1 ==> B99
* I$102/I$1/B1 ==> B100
* I$1142/I$3/B1 ==> B101
* I$1142/I$2/B1 ==> B102
* I$1142/I$261/B1 ==> B103
* I$1142/I$1/B1 ==> B104
* I$1143/I$3/B1 ==> B105
* I$1143/I$2/B1 ==> B106
```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

```
* I$1143/I$261/B1 ==> B107
* I$1143/I$1/B1 ==> B108
* I$1145/I$3/B1 ==> B109
* I$1145/I$2/B1 ==> B110
* I$1145/I$261/B1 ==> B111
* I$1145/I$1/B1 ==> B112
* I#/I$3/B1 ==> B113
* I#/I$2/B1 ==> B114
* I#/I$261/B1 ==> B115
* I#/I$1/B1 ==> B116
* I$944/B1 ==> B117
* NETLIST COMPLETED *
* run control
.TEMP=95
.TRAN 20PS 5NS
.OPTIONS LIMPTS=1000
.PRINT TRAN V(535) V(529) V(511) V(526) V(539) V(514) I(VSEU)
.END
```

Figure 7 Extracted VSPICE Netlist for Votebit (Con't)

4 Inverters x 2 FET's/Inverter	= 8 FET's
2 Super-Inverters x 4 FET's/Super-Inverter	= 8 FET's
7 NOR3 x 4 FET's/NOR3	= 28 FET's
24 NOR2 x 3 FET's/NOR2	= 72 FET's
1 Isolated FET	= 1 FET
<b>TOTAL</b>	<b>= 117 FET's</b>

From the information contained on two primitive instances shown in Figure 5, we can easily identify their transistors in the VSPICE netlist. Notice the NOR3 gate is instance number I\$67 and that the super-inverter is instance I\$608. We expect to find 1 D mode transistor and 3 E mode transistors for the NOR 3, and two of each type for the super-inverter. Included at the back end of the netlist is a set of 'comments' which map the instance names into the actual VSPICENET transistor designation.

Consider the case of the super-inverter specification of Figure 6. This generic schematic has four instances within it: I\$1, I\$3, I\$222, and I\$221. Since there could be many instances of the super-inverter used in the DMC, we need to specify only that super-inverter which has been 'programmed' with the sizes from the 'VOTEbit' application. Therefore, the instances we are looking for are I\$608/I\$1, I\$608/I\$3, etc. The comment list identifies that the FET's that implement the super-inverter in the VSPICE netlist are B81, B82, B83, and B84.

This netlist can now be used to simulate the circuit in various applications by appending the correct stimulus file. For example, it is possible to determine the critical charge needed to upset the 'VOTEBIT'. One potential weakness for any majority vote latch is to be struck in one of the single points of the feedback path that occur after the vote circuitry. It is known that only 60 fC of charge is needed to upset the latch elements. It is interesting to speculate how much charge is required to upset the circuit if the super-inverter or the NOR3 is struck.

Recall that the feedback path of the latch is loaded with the output load capacitance, and is driven by the super-inverter. This constitutes the SEU pulse swallowing filter which helps the 'VOTEBIT' resist SEU.

To locate the actual capacitance found on a node, we only have to look up the results from the Silvar-Lisco NCA parametric extraction run. We started out by trying to locate the DMA register circuit for simulation. We found this register on the top level schematic diagram of Figure 1. Notice that the output of the DMA register feeds a bus named 'DMAA(15:0)'. To properly simulate the circuit, we investigate the capacitance connected to each element of this bus.

Figure 8 contains a small portion of the parametric extractor output. A few busses of interest are shown. The parametric extractor calculates these values based the physical sizes of the load devices, and on a configuration table that identifies interconnect parallel plate and fringing capacitance. The resulting capacitances are shown for parallel plate and total node capacitance in FemtoFarads.

The bus name, X and Y coordinates of the bus origin, and capacitive values make it easy to identify the load spread on the DMAA bus. We see that the VOTEBIT is connected to a bus that exhibits between 1.9 pF and 2.7 pF of total load capacitance. The squirt buffer structure was chosen to drive this load capacitance spread. The capacitive variation arises from the interconnect, since the number of, and physical size of the loads are identical for each signal in the DMAA bus. Thus, chip designs can be speed limited by elements not visible on the schematic.

The capacitive value of 2.2 pF was chosen for the simulation. The VSPICE statements which drive the simulation for this case are shown in the netlist of Figure 7. Iterative SPICE simulations were run until two simulations were achieved that bound the critical charge of the circuit. The results of these simulations are shown in Figure 9.

These simulations indicate an approximate critical charge of fC. This should be compared against the intrinsic critical charge of a latch element, 60 fC.

3-27-91 N C A E P C N O D E R E P O R T F O R E P E

NODE NAME	COORDINATES		TOTAL CAPACITANCE	
	X	Y	XCAP	CAP
(DMAA<0>) .....	8308.50	1458.00	221.129	1913.963
(DMAA<10>) .....	6858.50	1458.00	291.401	2234.483
(DMAA<11>) .....	6728.50	1458.00	326.537	2506.187
(DMAA<12>) .....	6568.50	1458.00	303.113	2296.859
(DMAA<13>) .....	6438.50	1458.00	342.153	2584.731
(DMAA<14>) .....	6278.50	1458.00	314.825	2359.659
(DMAA<15>) .....	6148.50	1458.00	351.913	2654.875
(DMAA<1>) .....	8178.50	1458.00	238.697	2137.987
(DMAA<2>) .....	8018.50	1458.00	236.745	1979.219
(DMAA<3>) .....	7888.50	1458.00	258.217	2207.147
(DMAA<4>) .....	7728.50	1458.00	252.361	2044.475
(DMAA<5>) .....	7598.50	1458.00	277.737	2276.307
(DMAA<6>) .....	7438.50	1458.00	267.977	2112.187
(DMAA<7>) .....	7308.50	1458.00	295.305	2349.947
(DMAA<8>) .....	7148.50	1458.00	279.689	2172.107
(DMAA<9>) .....	7018.50	1458.00	310.921	2428.067
(XSRCI<0>) .....	9892.50	519.50	101.002	1792.325
(XSRCI<10>) .....	8116.00	519.50	93.194	1483.555
(XSRCI<11>) .....	7834.00	519.50	97.098	1416.733
(XSRCI<12>) .....	7416.00	519.50	101.002	1455.859
(XSRCI<13>) .....	7384.50	519.50	101.002	1434.699
(XSRCI<14>) .....	7108.00	519.50	83.434	1484.761
(XSRCI<15>) .....	7076.50	519.50	83.434	1463.601
(XSRCI<1>) .....	9610.50	519.50	101.002	1749.885
(XSRCI<2>) .....	9579.00	519.50	108.810	1754.269
(XSRCI<3>) .....	9297.00	519.50	108.810	1713.949
(XSRCI<4>) .....	9265.50	519.50	116.618	1718.333
(XSRCI<5>) .....	8879.00	519.50	89.290	1439.211
(XSRCI<6>) .....	8847.50	519.50	89.290	1435.315
(XSRCI<7>) .....	8461.00	519.50	89.290	1369.659
(XSRCI<8>) .....	8429.50	519.50	89.290	1433.403
(XSRCI<9>) .....	8147.50	519.50	89.290	1363.651
(DMAI<0>) .....	13104.50	519.50	24.874	1963.229
(DMAI<10>) .....	11328.00	519.50	24.874	1866.733
(DMAI<11>) .....	11178.50	519.50	24.874	1893.373
(DMAI<12>) .....	11014.50	519.50	28.778	1864.421
(DMAI<13>) .....	10865.00	519.50	28.778	1889.877
(DMAI<1>) .....	12955.00	519.50	24.874	1989.869
(DMAI<2>) .....	12791.00	519.50	20.970	1952.517
(DMAI<3>) .....	12641.50	519.50	20.970	1979.749
(DMAI<4>) .....	12373.00	519.50	17.066	1910.429
(DMAI<5>) .....	12223.50	519.50	17.066	1939.156
(DMAI<6>) .....	12059.50	519.50	17.066	1904.213
(DMAI<7>) .....	11910.00	519.50	17.066	1929.887
(DMAI<8>) .....	11746.00	519.50	20.970	1901.605
(DMAI<9>) .....	11596.50	519.50	20.970	1927.653
(CSFI<0>) .....	12972.00	7184.00	37.088	2505.721
(CSFI<10>) .....	12123.00	5847.00	52.704	2420.593

Figure 8 Partial Output from Electrical Parameter Extractor (EPE) Run for DMC



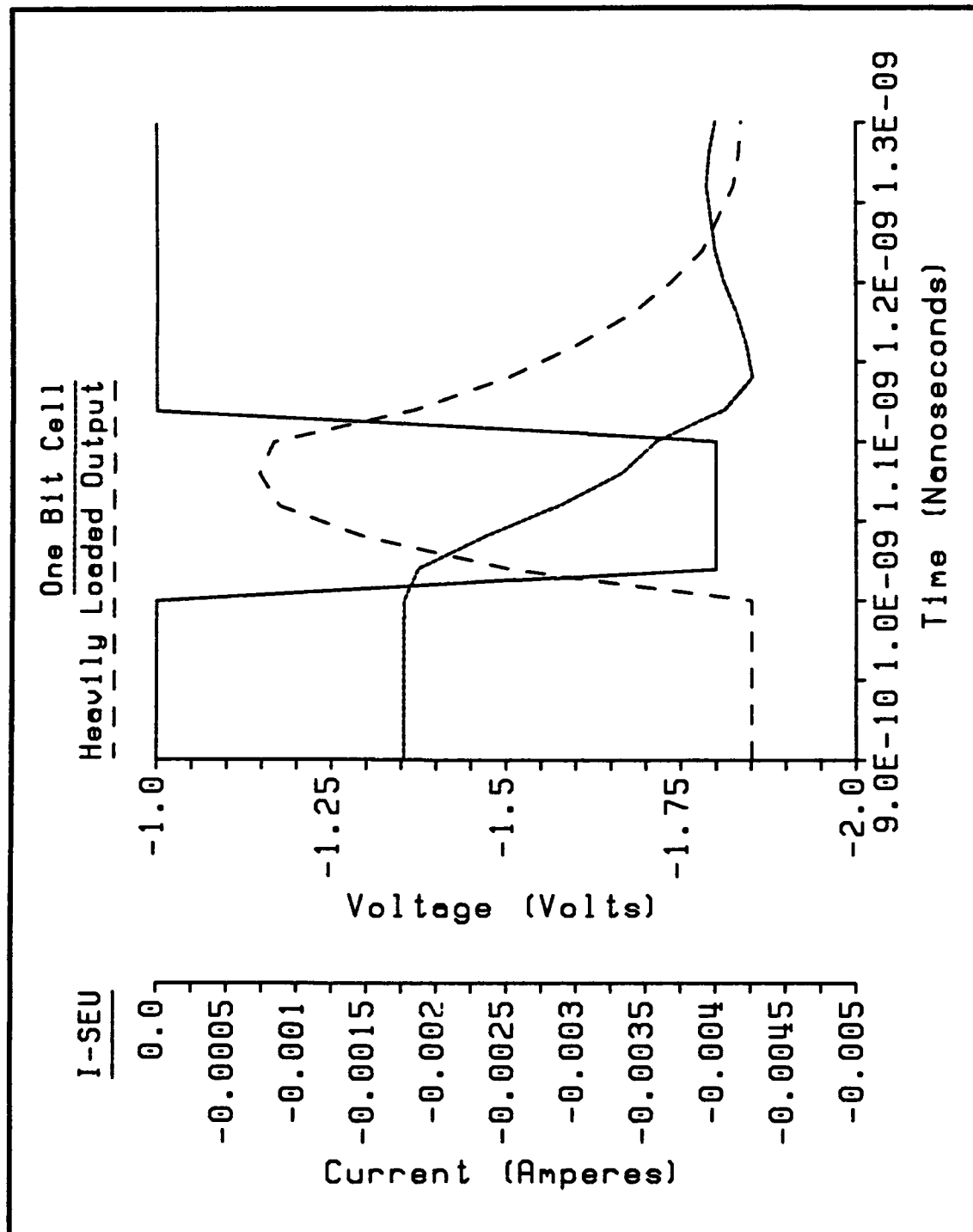


Figure 9 VOTEbit SEU Simulation

Figure 9 is a simulation of the critical charge of the VOTE<sub>BIT</sub>. The trapezoidal pulse is an estimation of the amount of current produced during a single event upset. The current arises from the gate electric field sweeping the free carriers that were produced by ionization into the conduction channel. This current is expressed in Coulombs/second (Amperes) for a given time period. Since the duration of the event is thought to be fast, a 100 pS pulse was used. Thus the simulated charge deposition is represented by the area under the waveform.

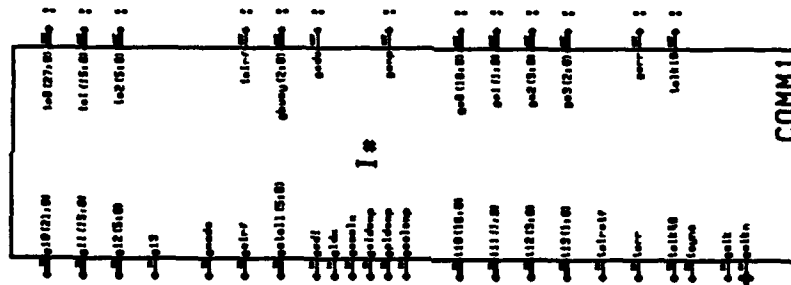
The simulation results shown the impact of depositing the SEU current pulse at different points in the circuit. If the current pulse is deposited on the 2.2 pF output node of the VOTE<sub>BIT</sub> register, no upset occurs. The current level is high enough to perturb the output, but not high enough or long enough to be loaded into the registers. This indicates that it is extremely difficult to upset the majority vote register from a hit to the logic that votes the output.

If the same current pulse is deposited into one of the internal nodes that is loaded with only 100 Femtofarads or so, an upset easily occurs. The upset occurs with deposited charge as little as 1/10 of the current shown in the figure, or approximately 40 fC. This indicates that the individual bits are very soft.

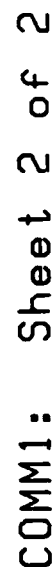
Thus, the following characteristics are expected:

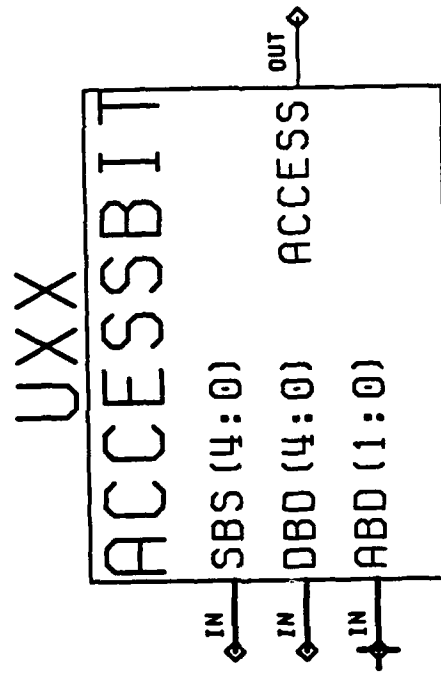
1. The individual bits will be upsetable by a much larger number of particles than 2 micron CMOS. This is because the particle spectrum in Earth orbit contains a large number ( $\sim 10^2$  particles/cm) of low energy particles that would normally not cause an upset in that technology.
2. The individual GaAs bits will exhibit a much lower critical charge than two micron CMOS. This results from geometry (1.2 micron gate length) and electric field intensity (gate voltage of 0.6 V instead of 5.0 V).
3. The VOTE<sub>BIT</sub> will not be sensitive to SEU hits in the logic where the vote is performed, nor will it propagate back into the individual storage elements.
4. The 'in circuit' hardness of the VOTE<sub>BIT</sub> element will be proportional to the operating clock speed. This follows since the scrub repetition rate is increasing, and there appear to be no single points of sensitivity.

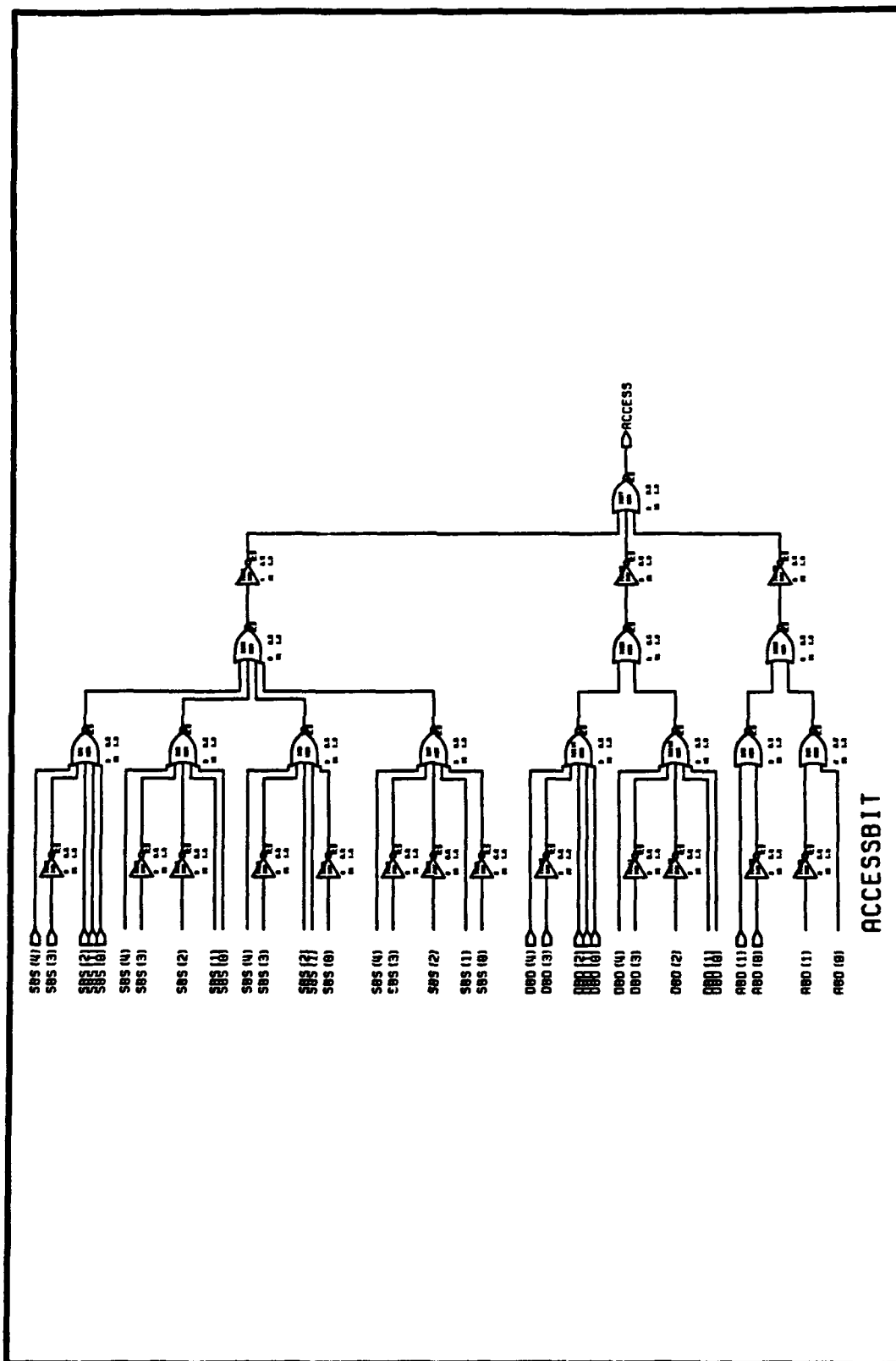
The previous analysis is indicative of the ways in which the schematics for the OBP80 Chipset can be used. The actual SEU response of the VOTE<sub>BIT</sub> should be determined by experimentation. The schematics can be prepared for logic simulation, fault analysis, layout, or critical path analysis in the same manner.

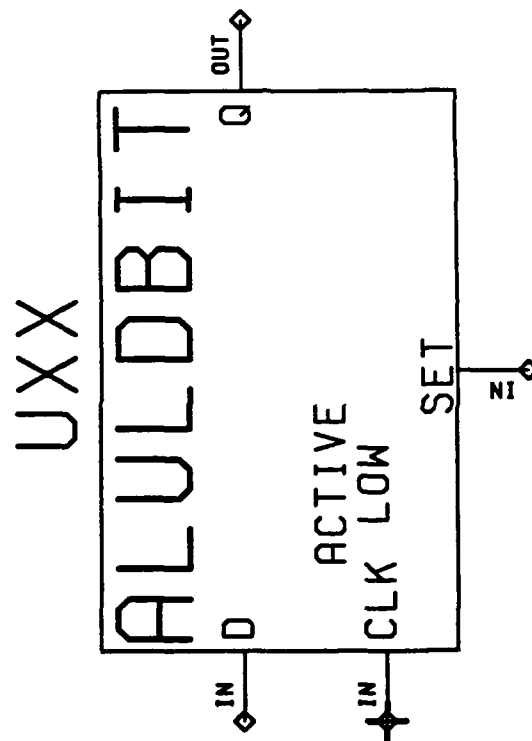




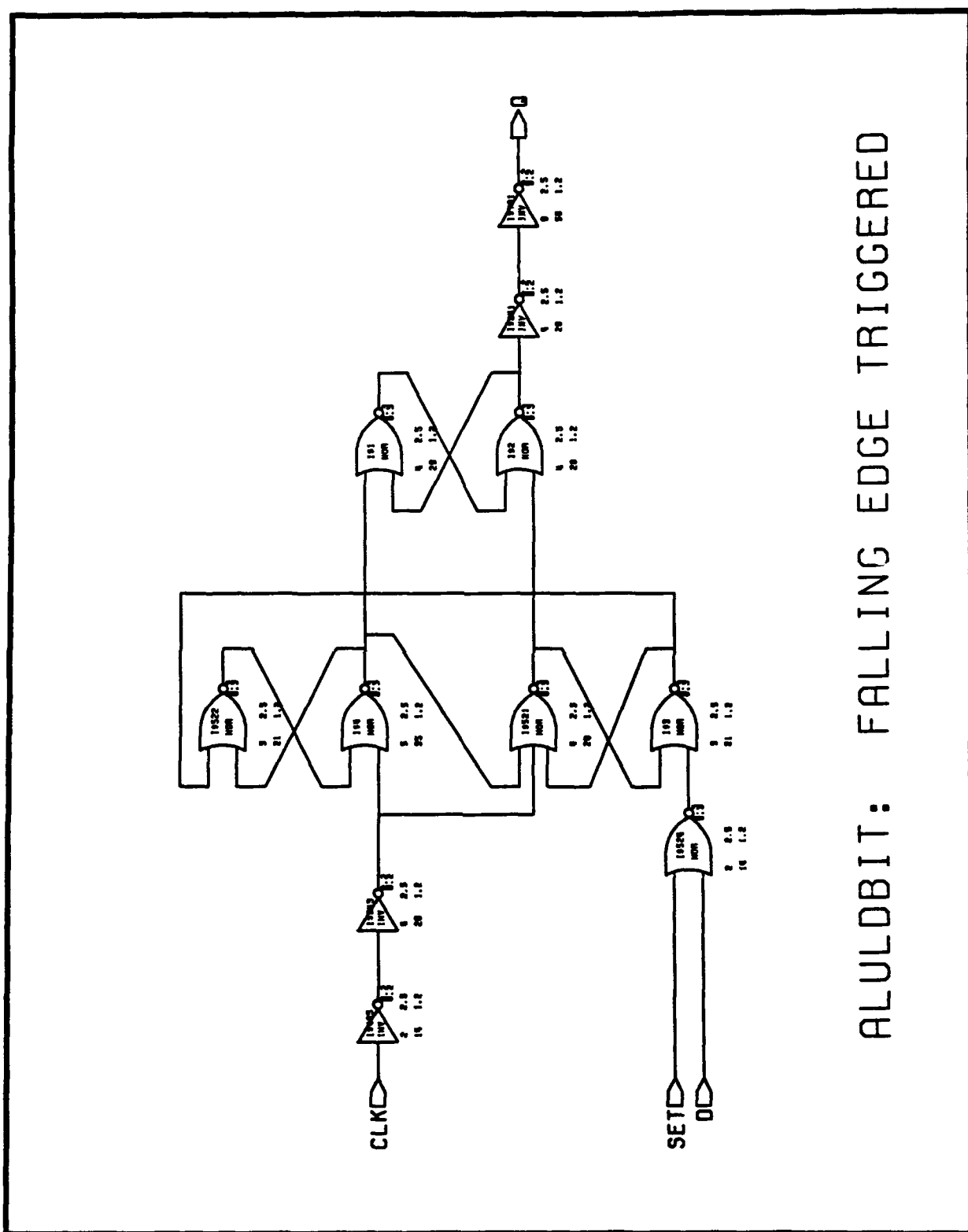




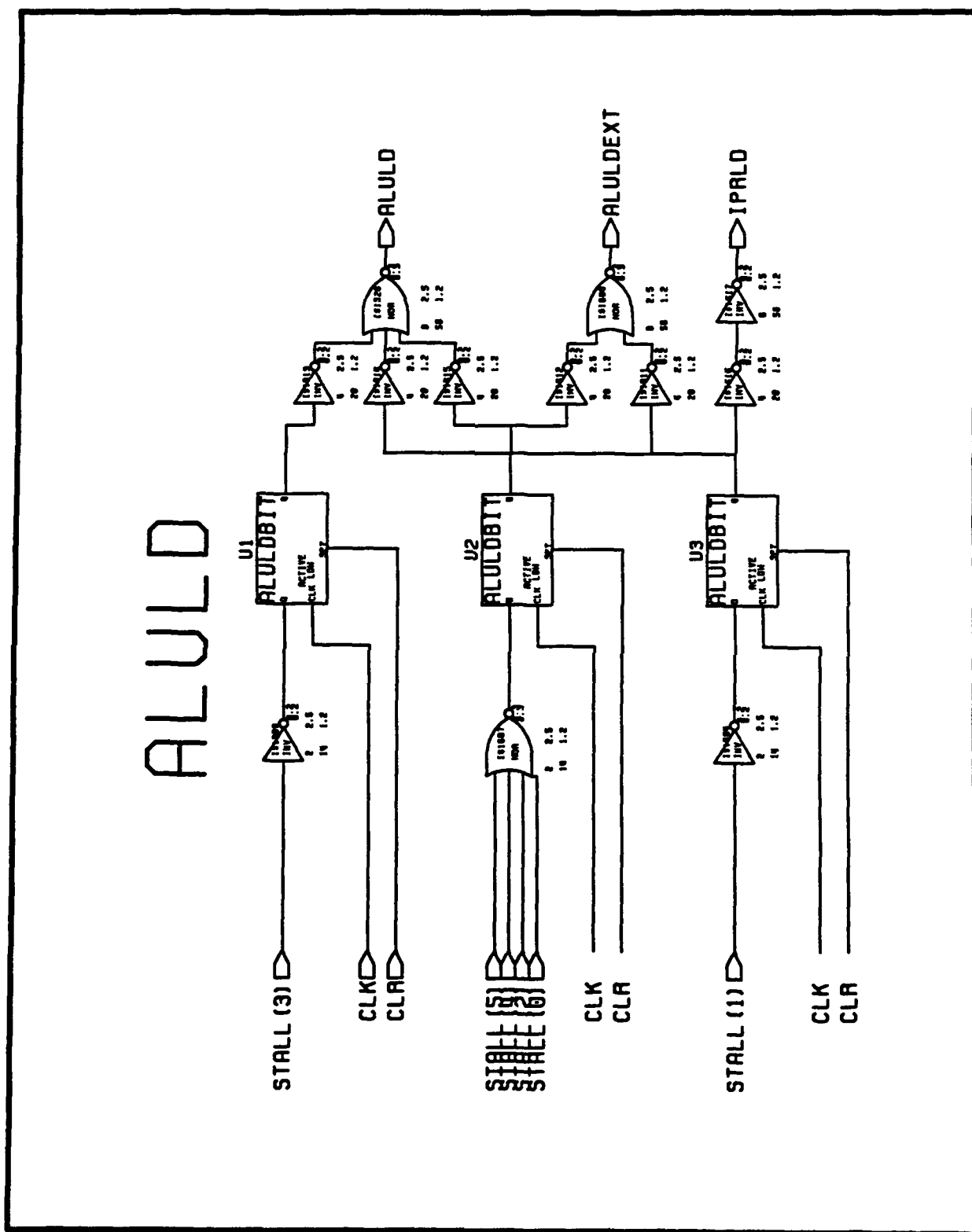


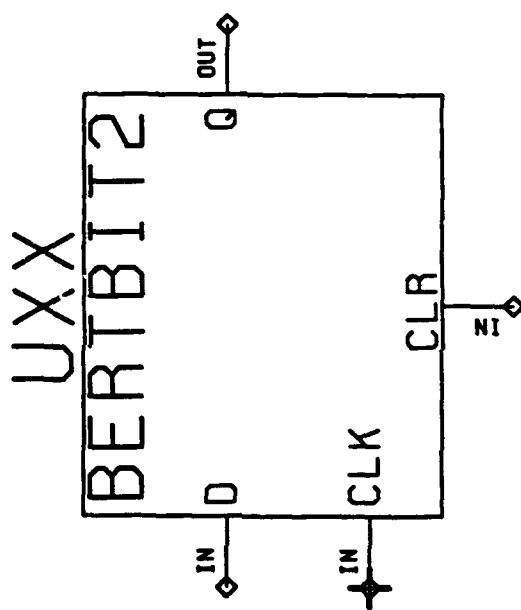


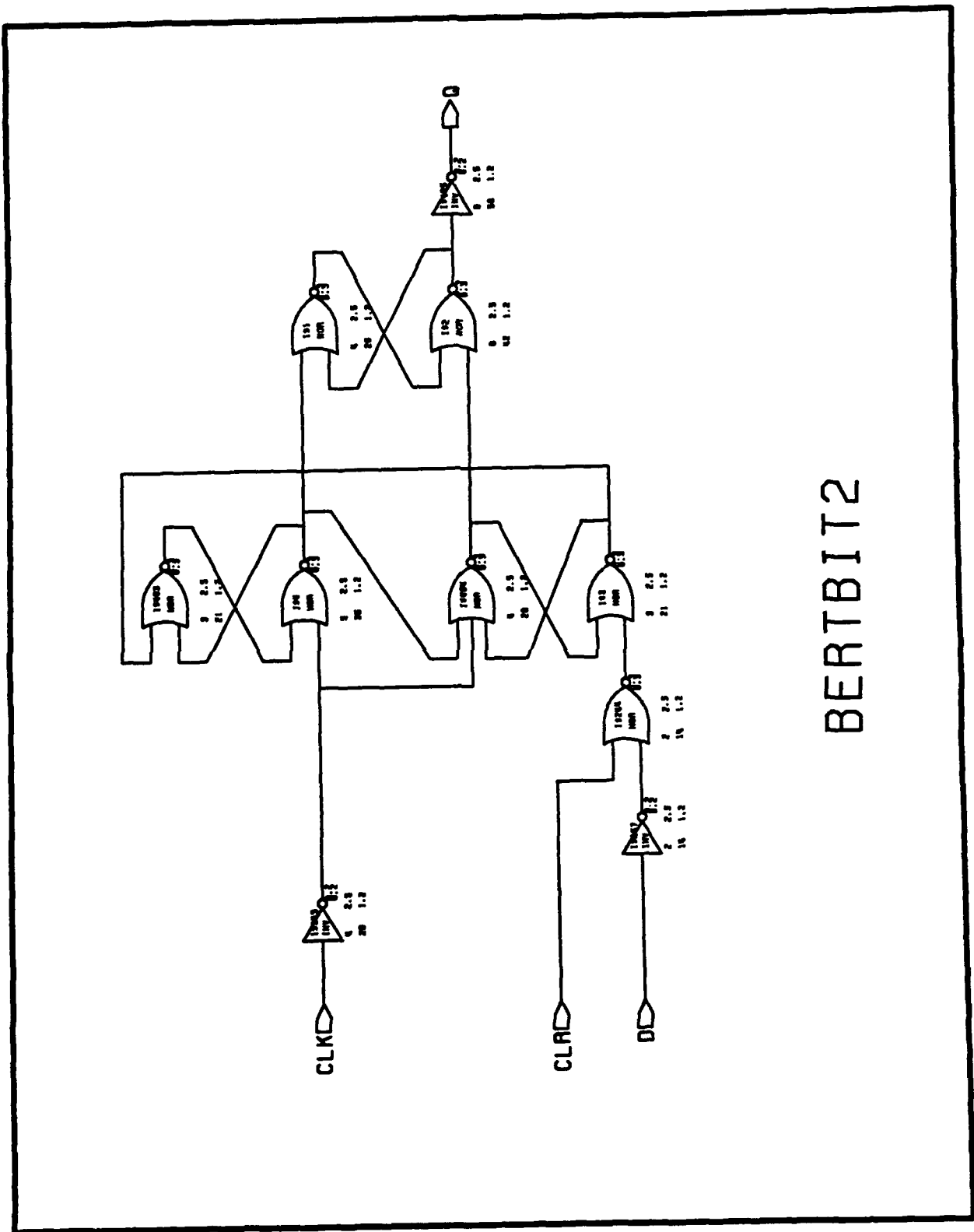




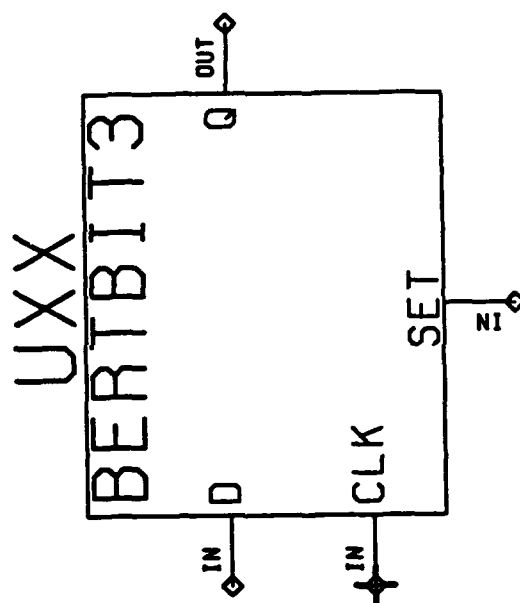


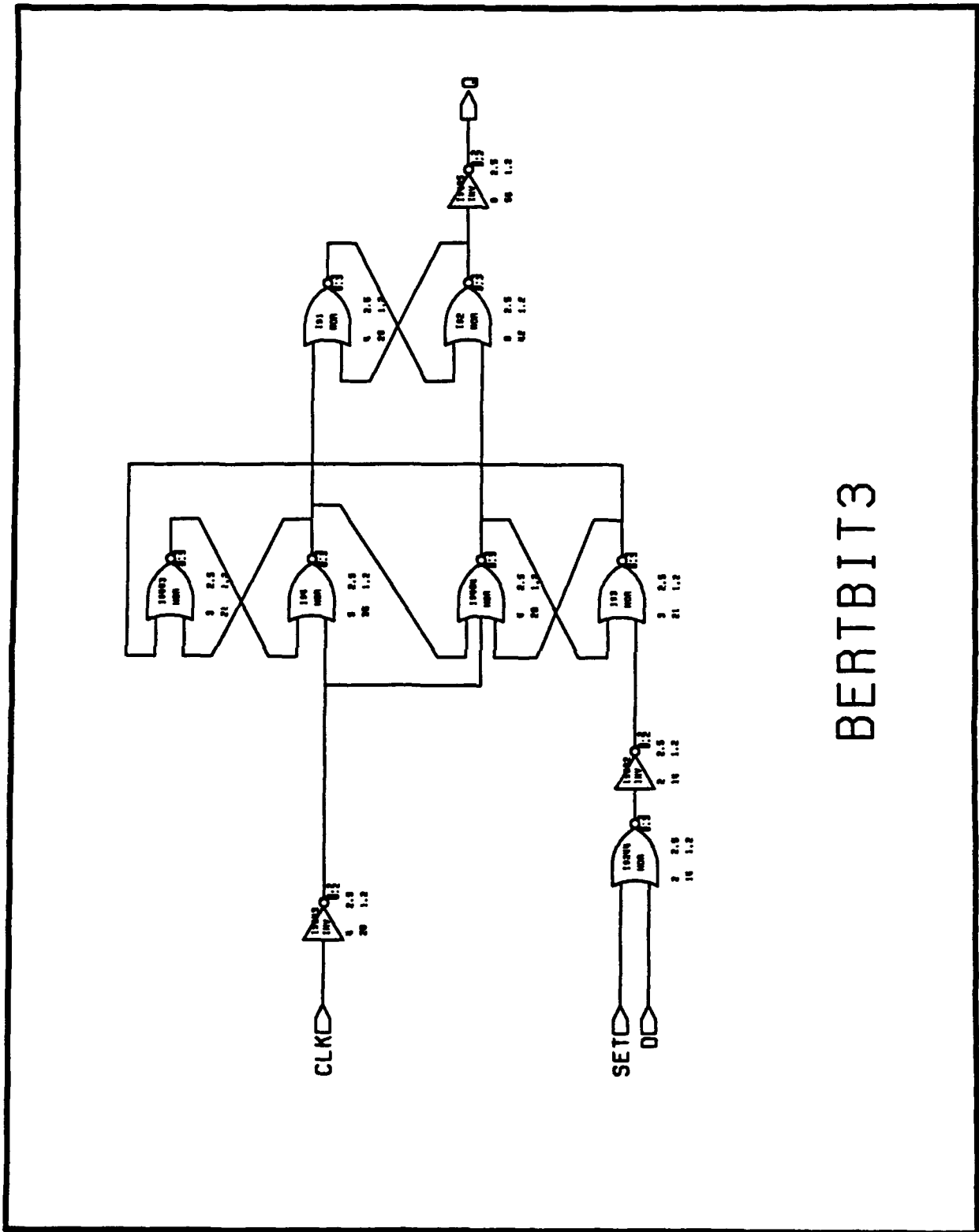


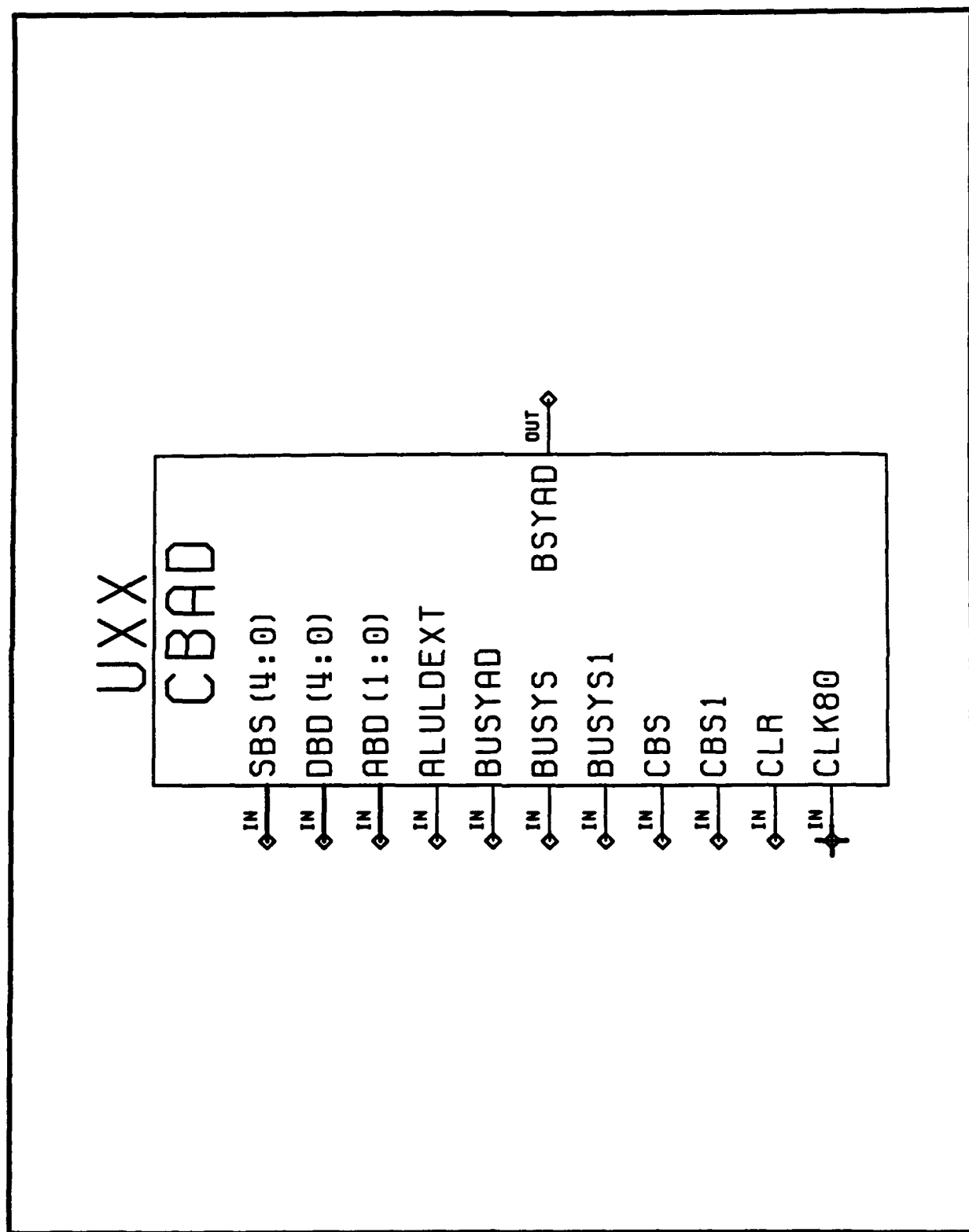




BERTBIT2

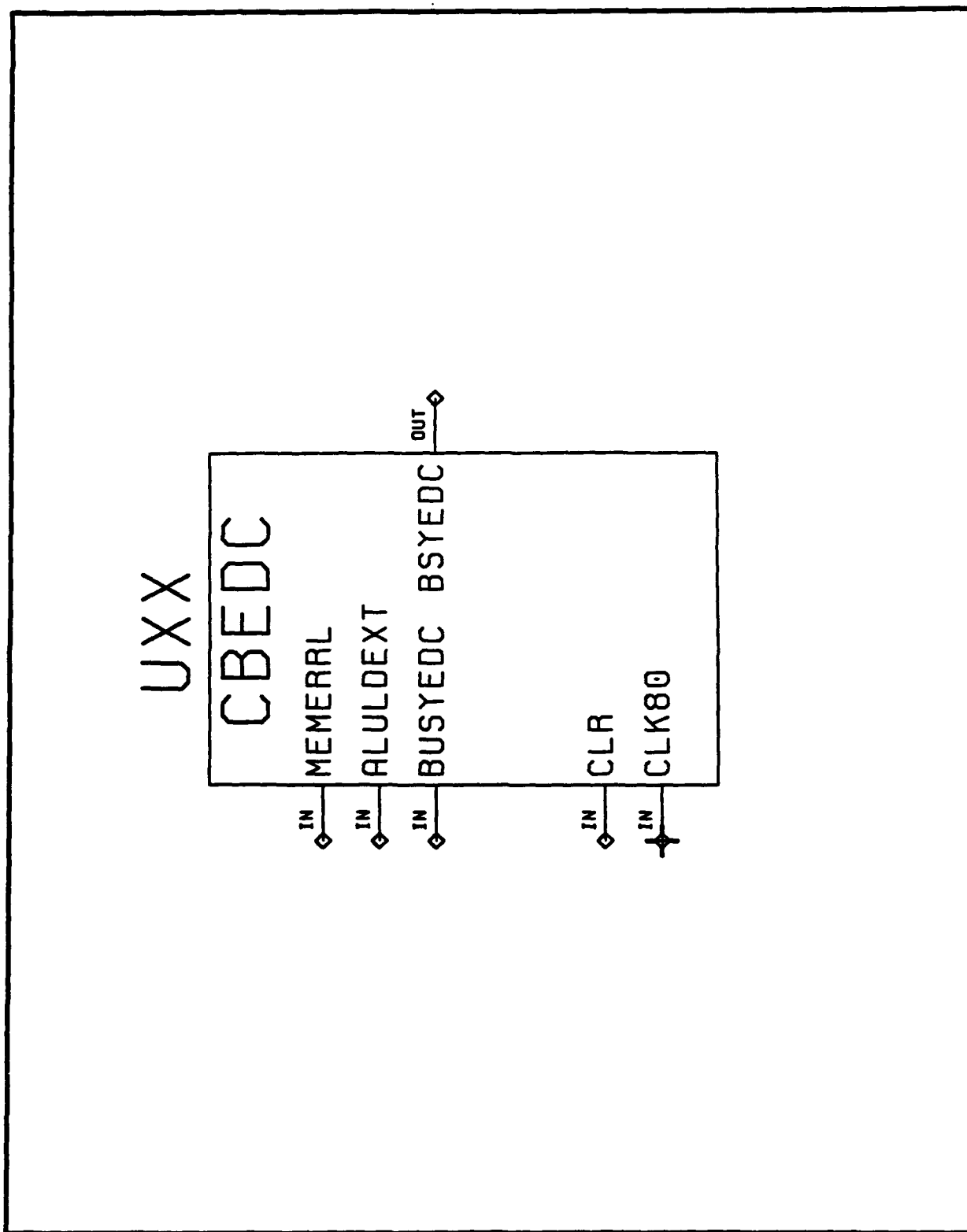


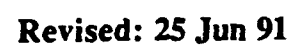


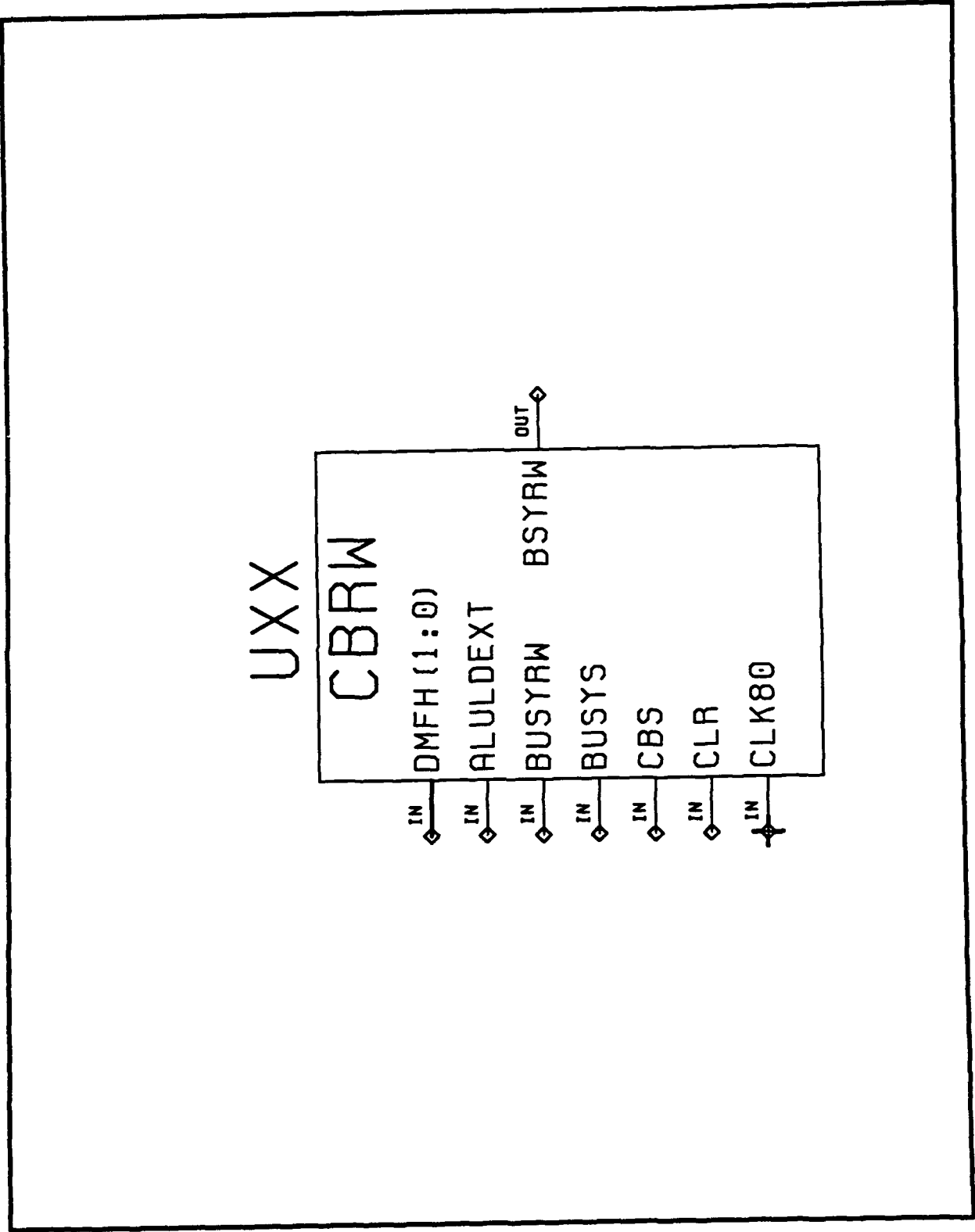




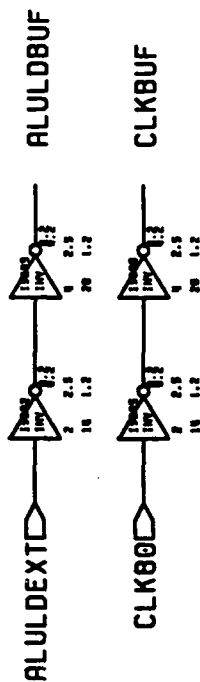
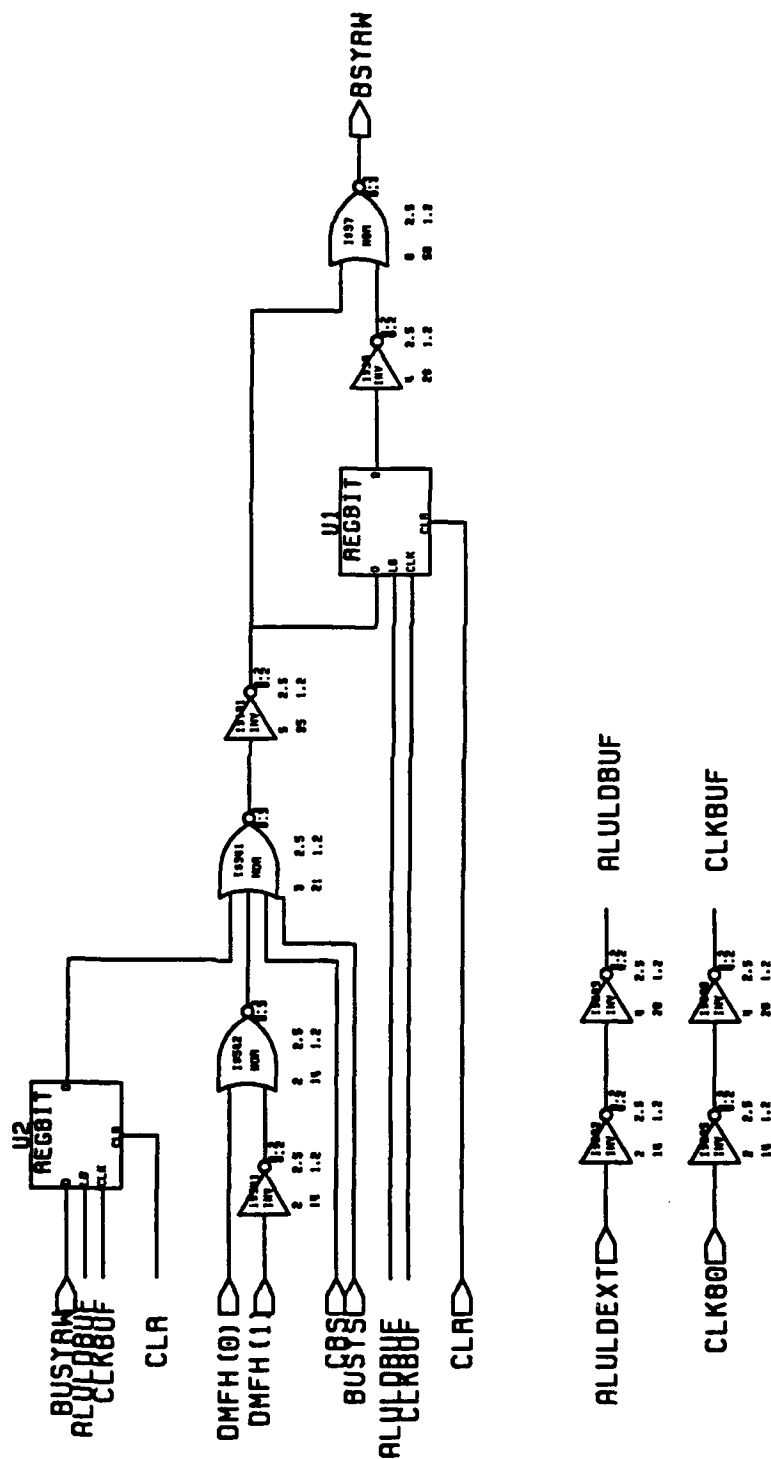


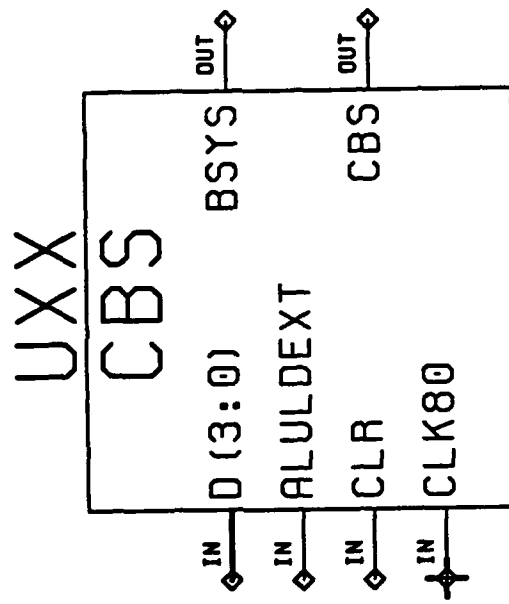




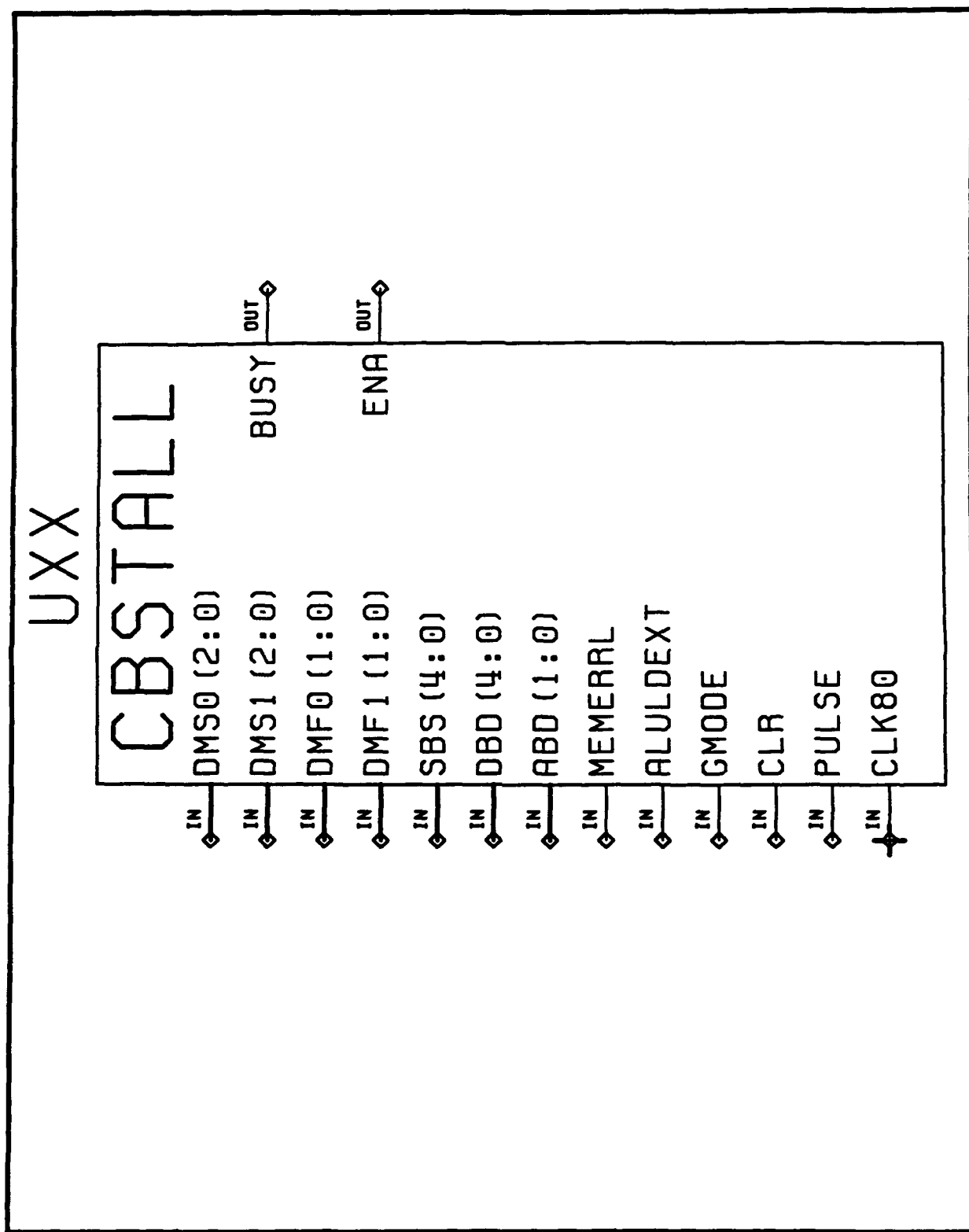


CBRW

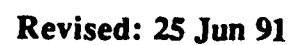








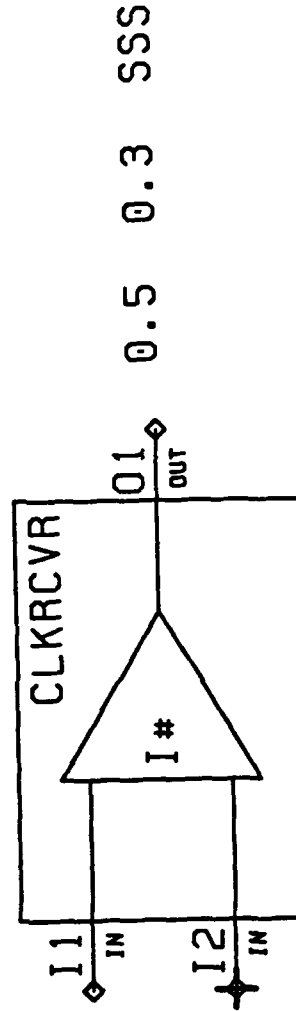




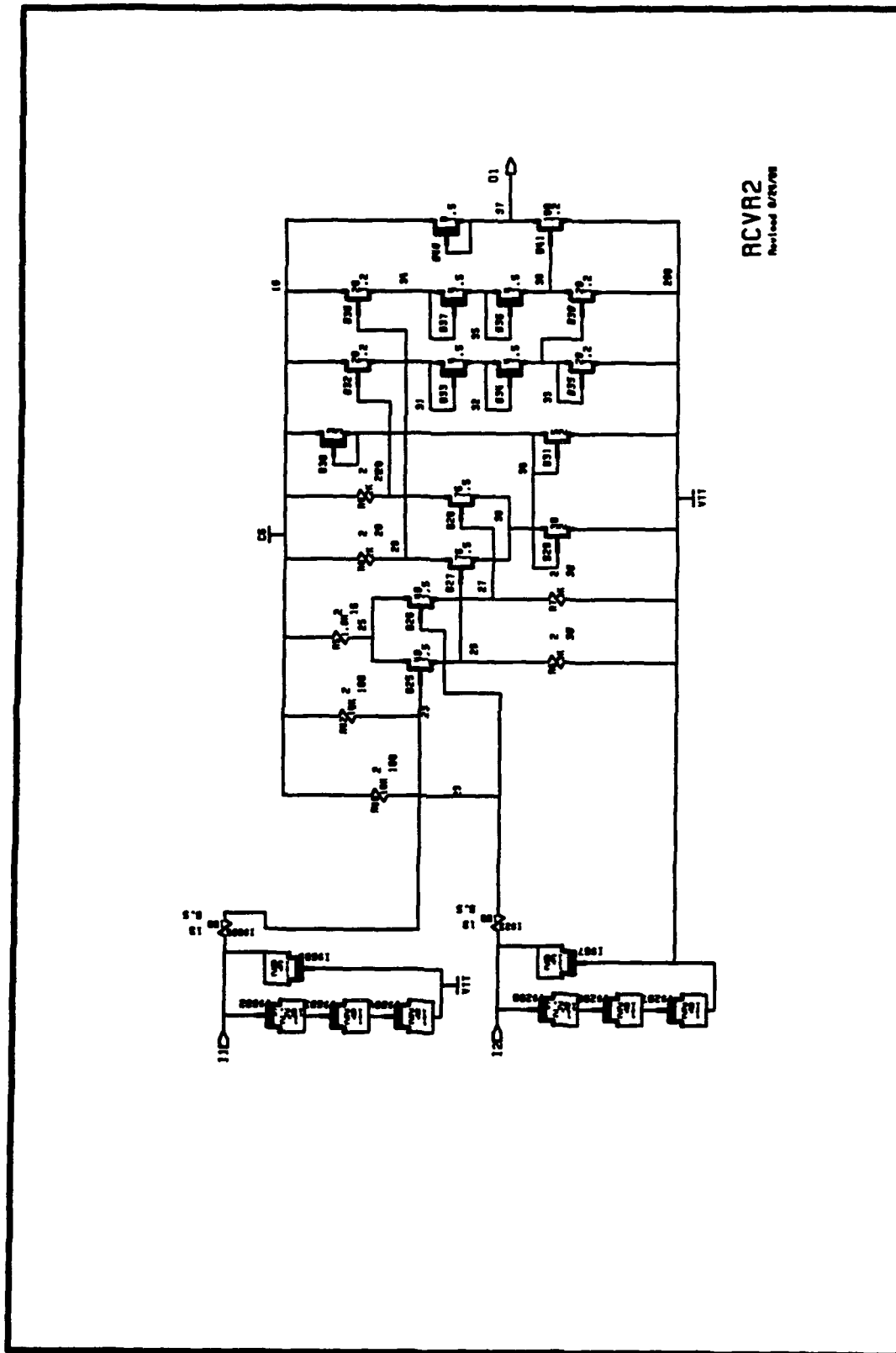
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Version 0.8

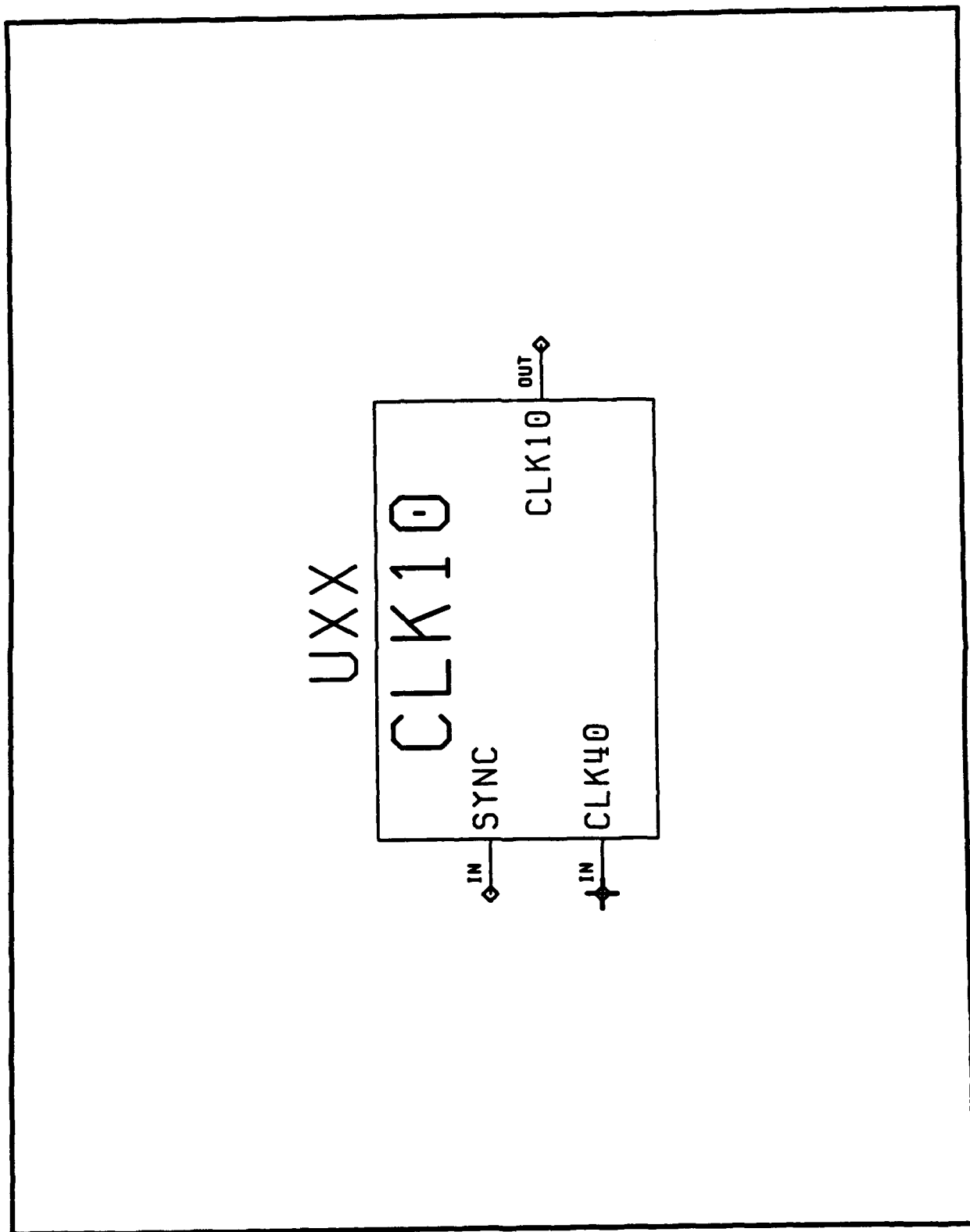
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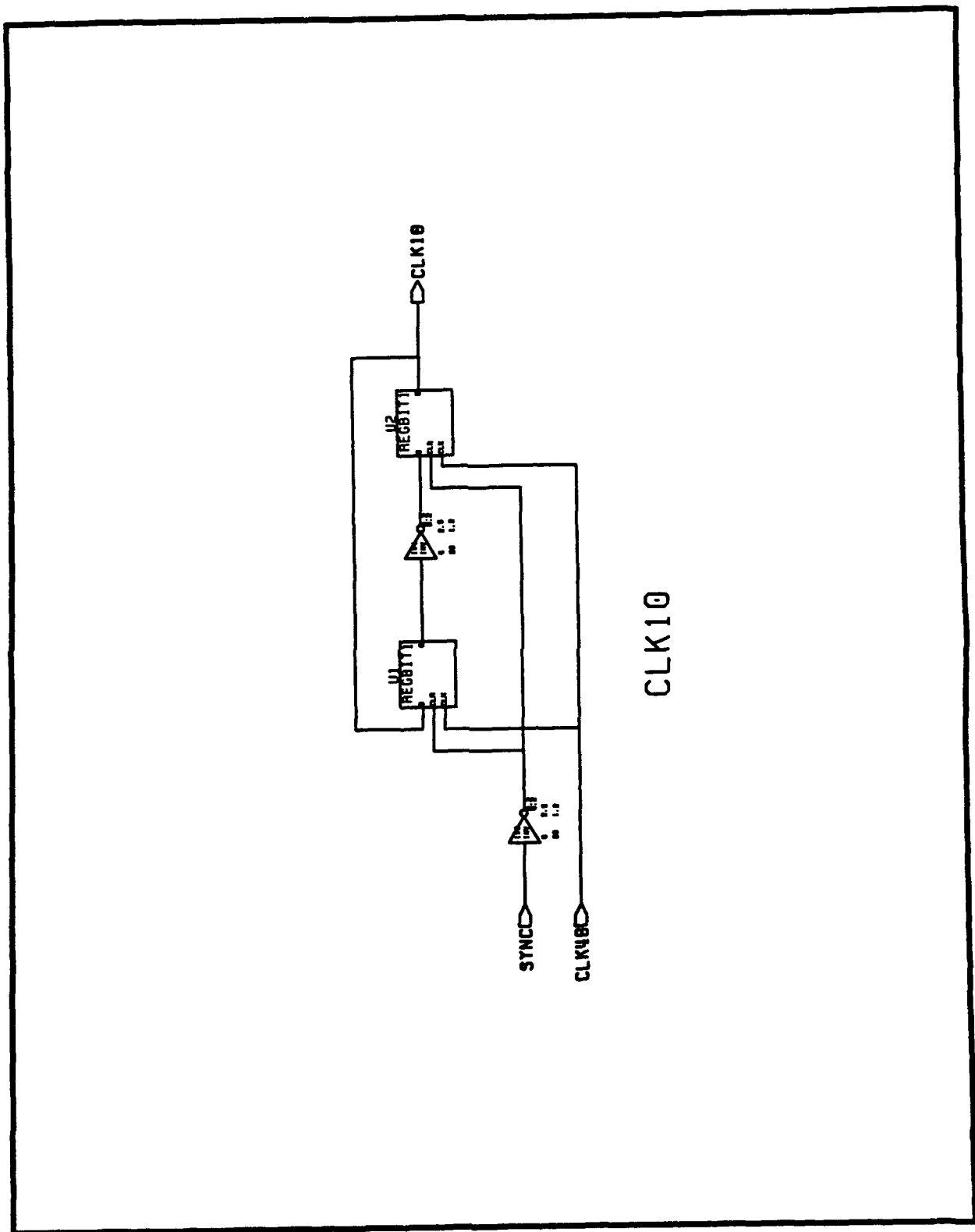
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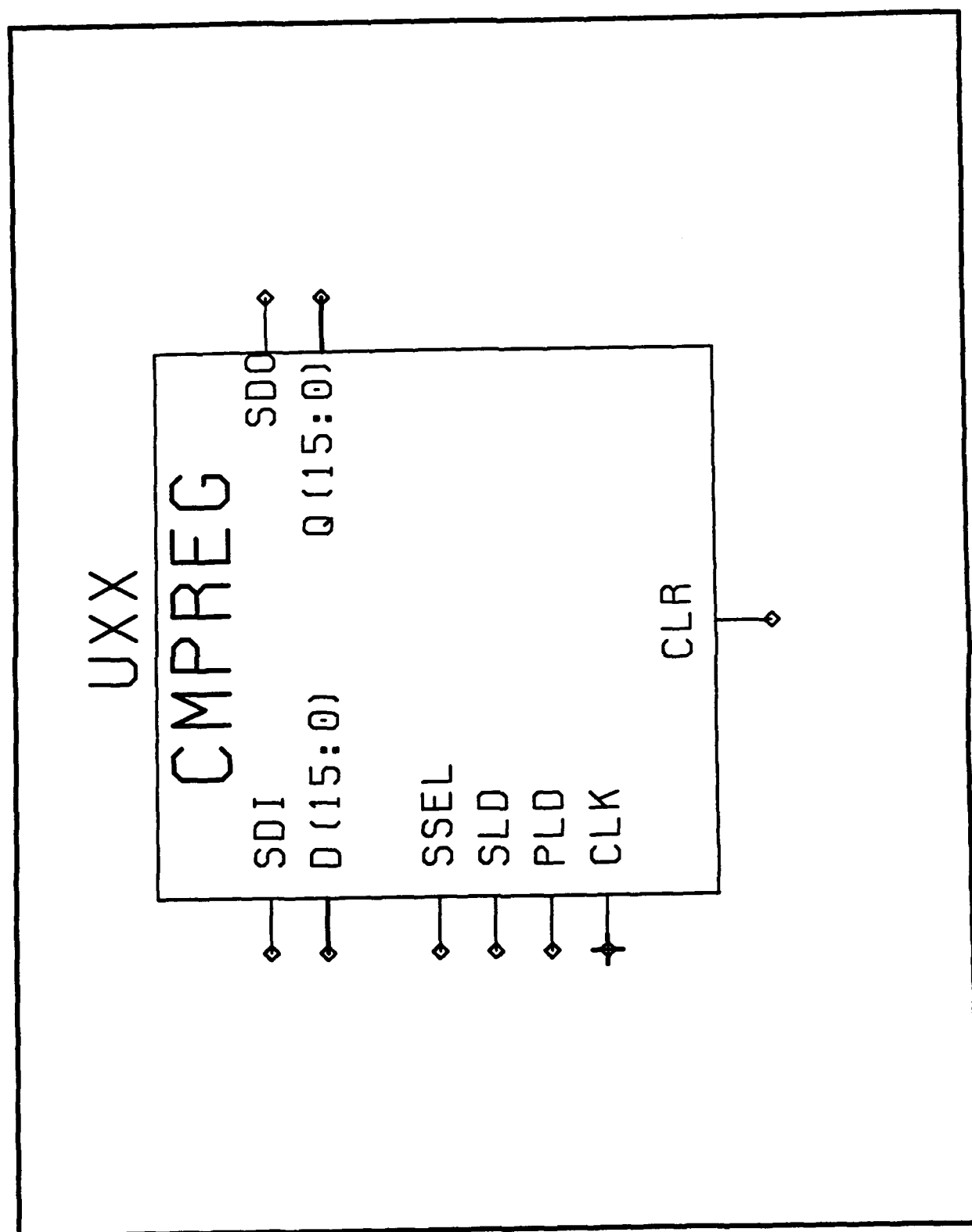


CLKRCVR  
clkrcvr.bin

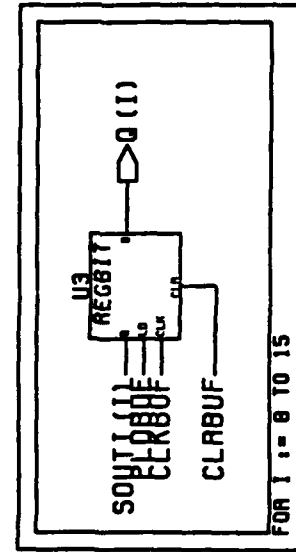
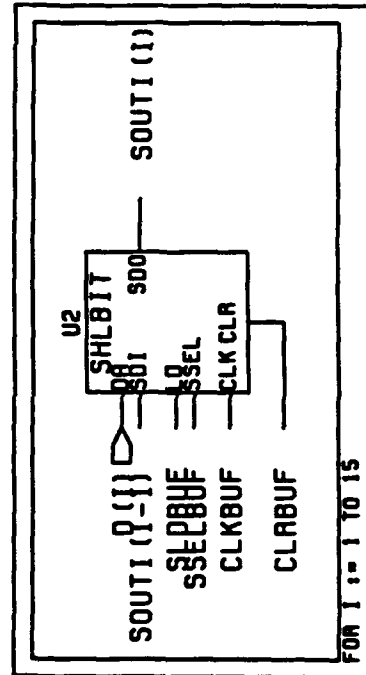
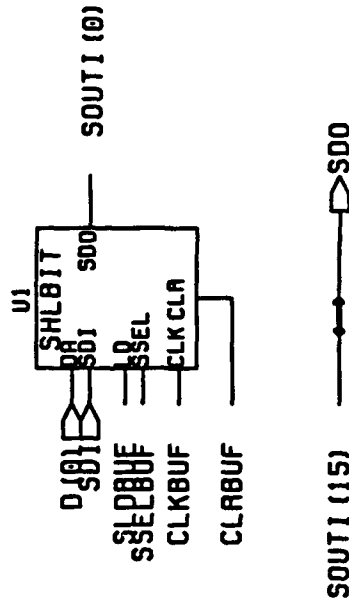
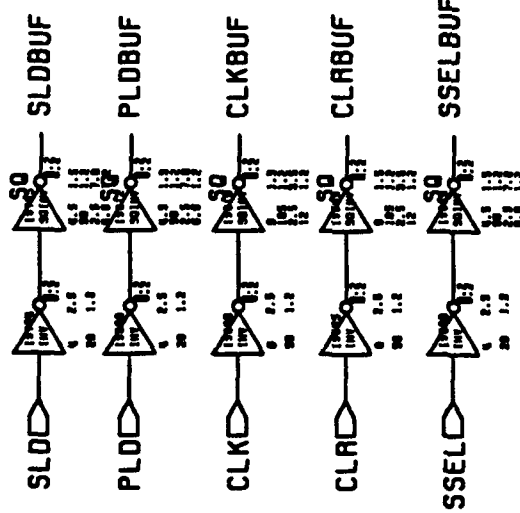


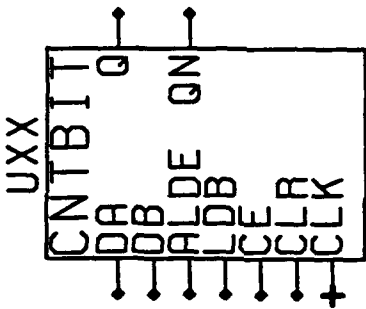




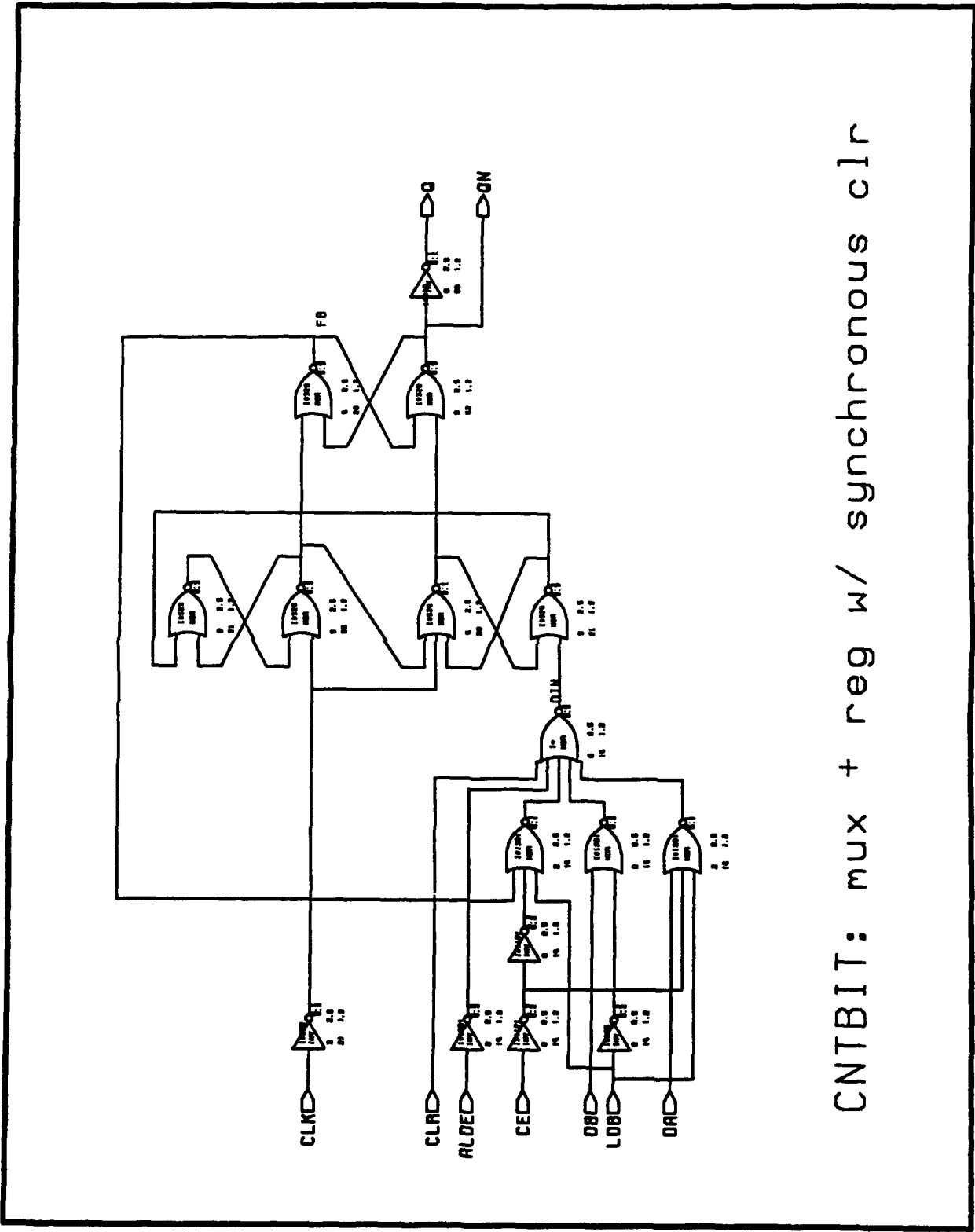


# CMPREG

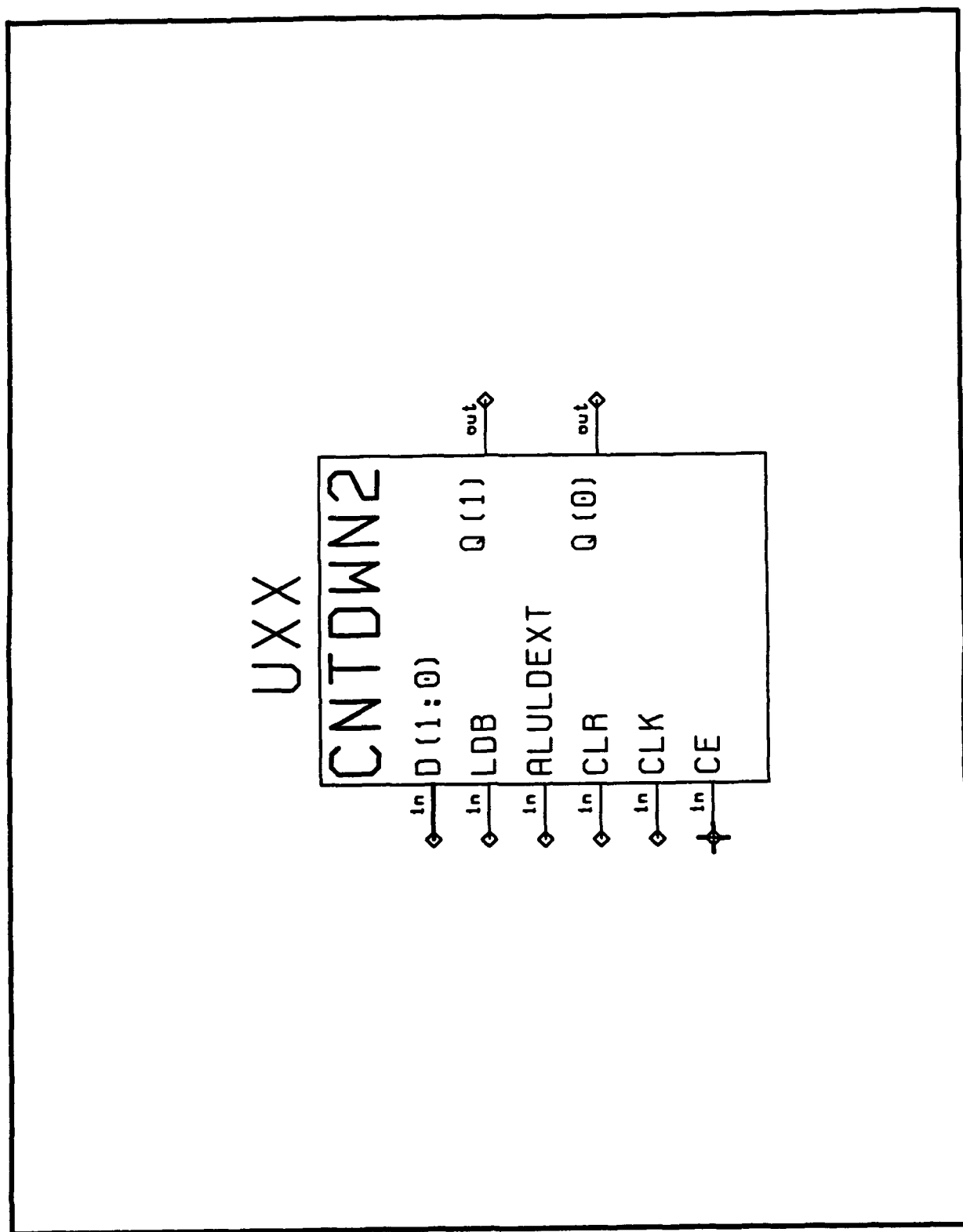




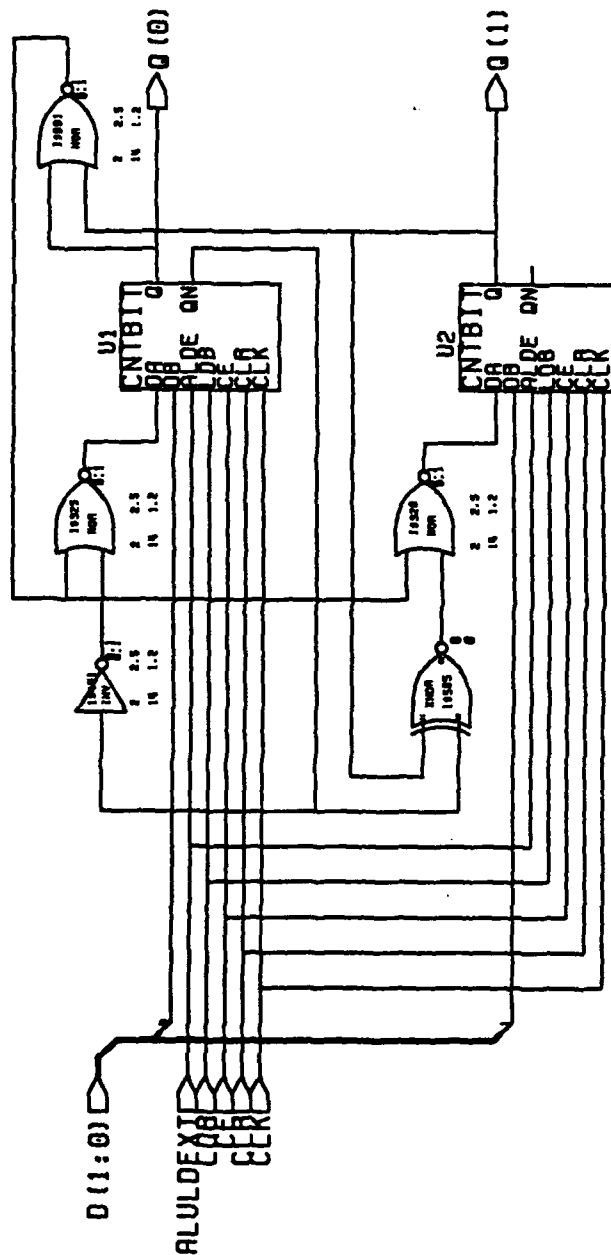


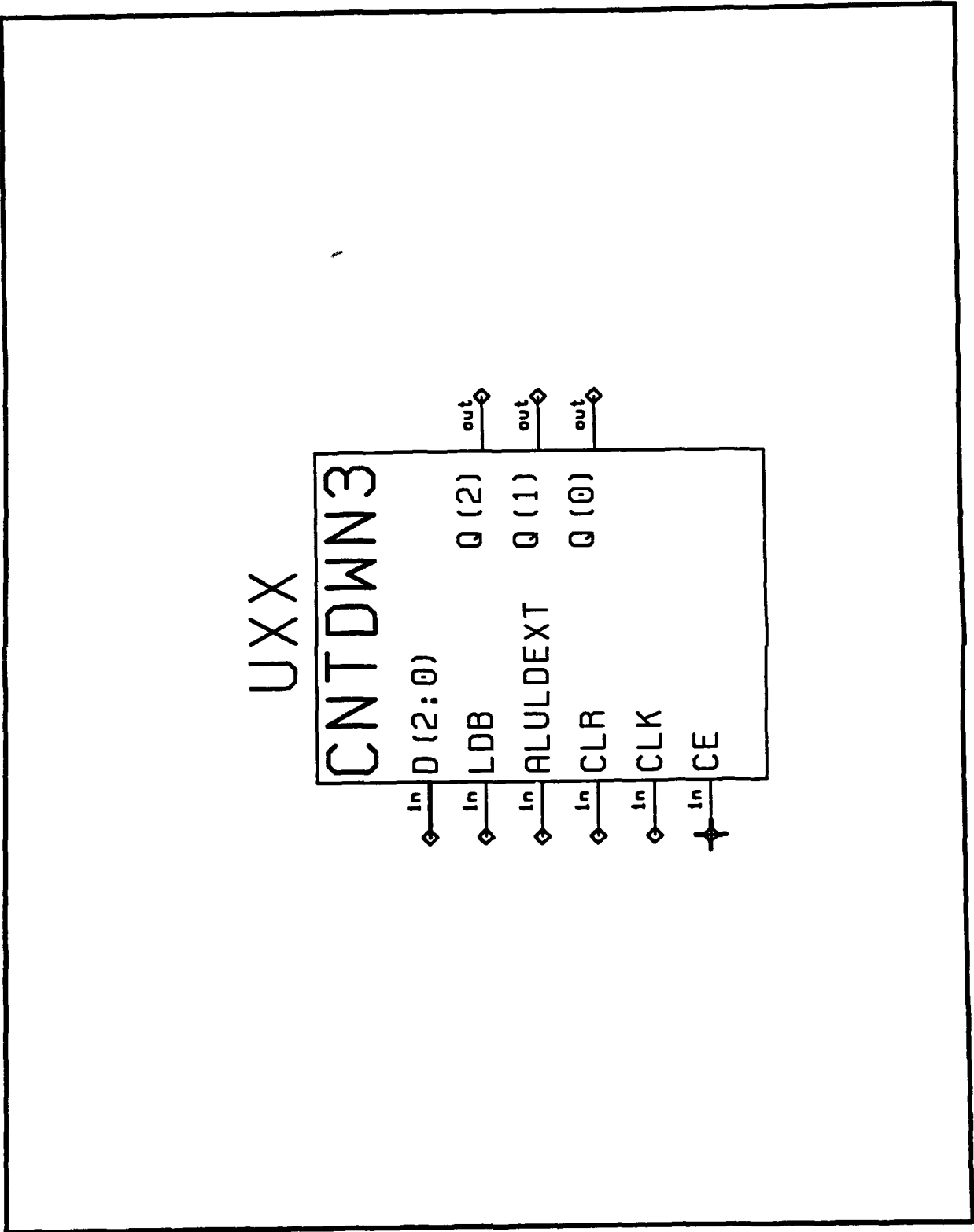


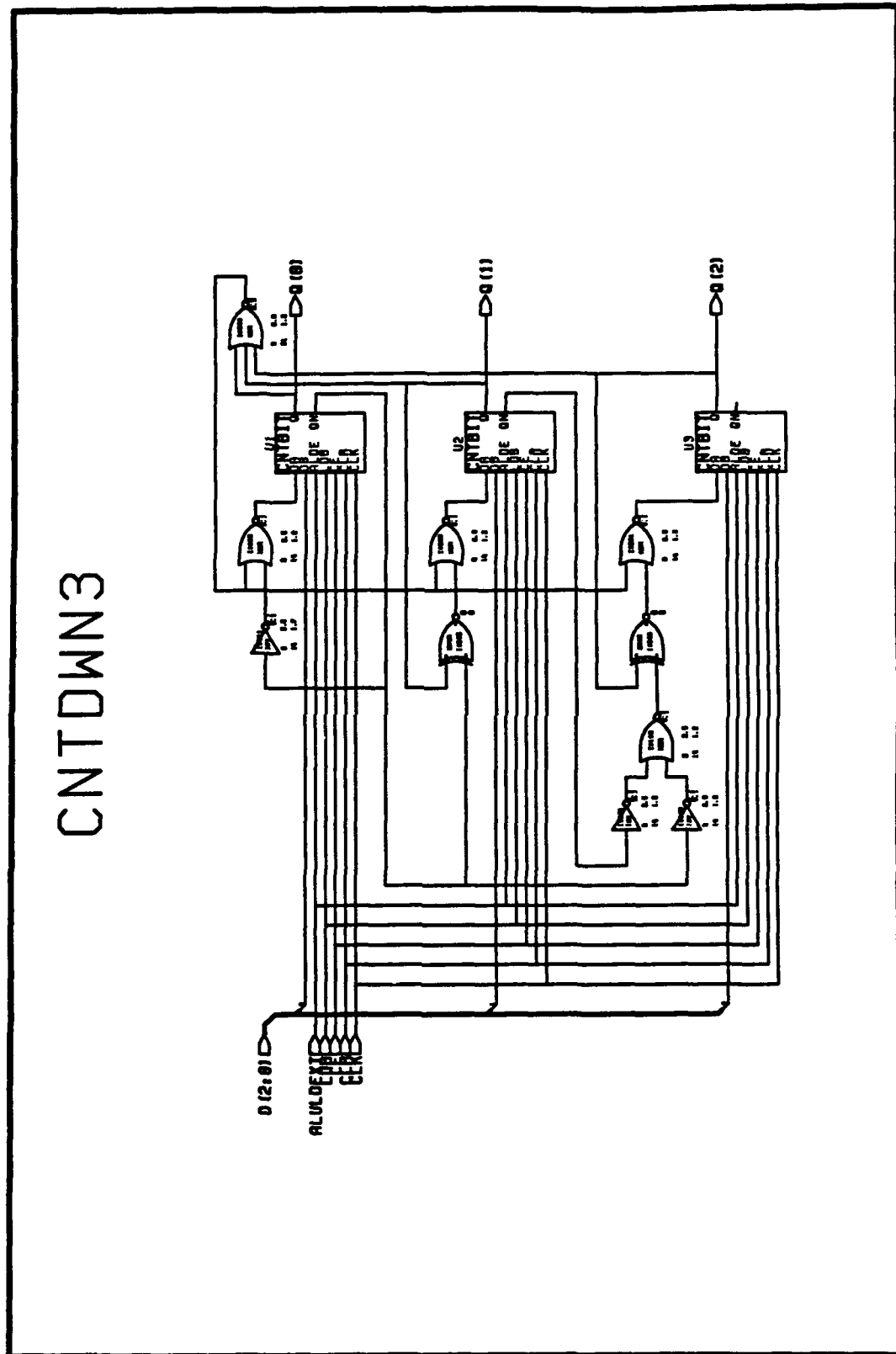
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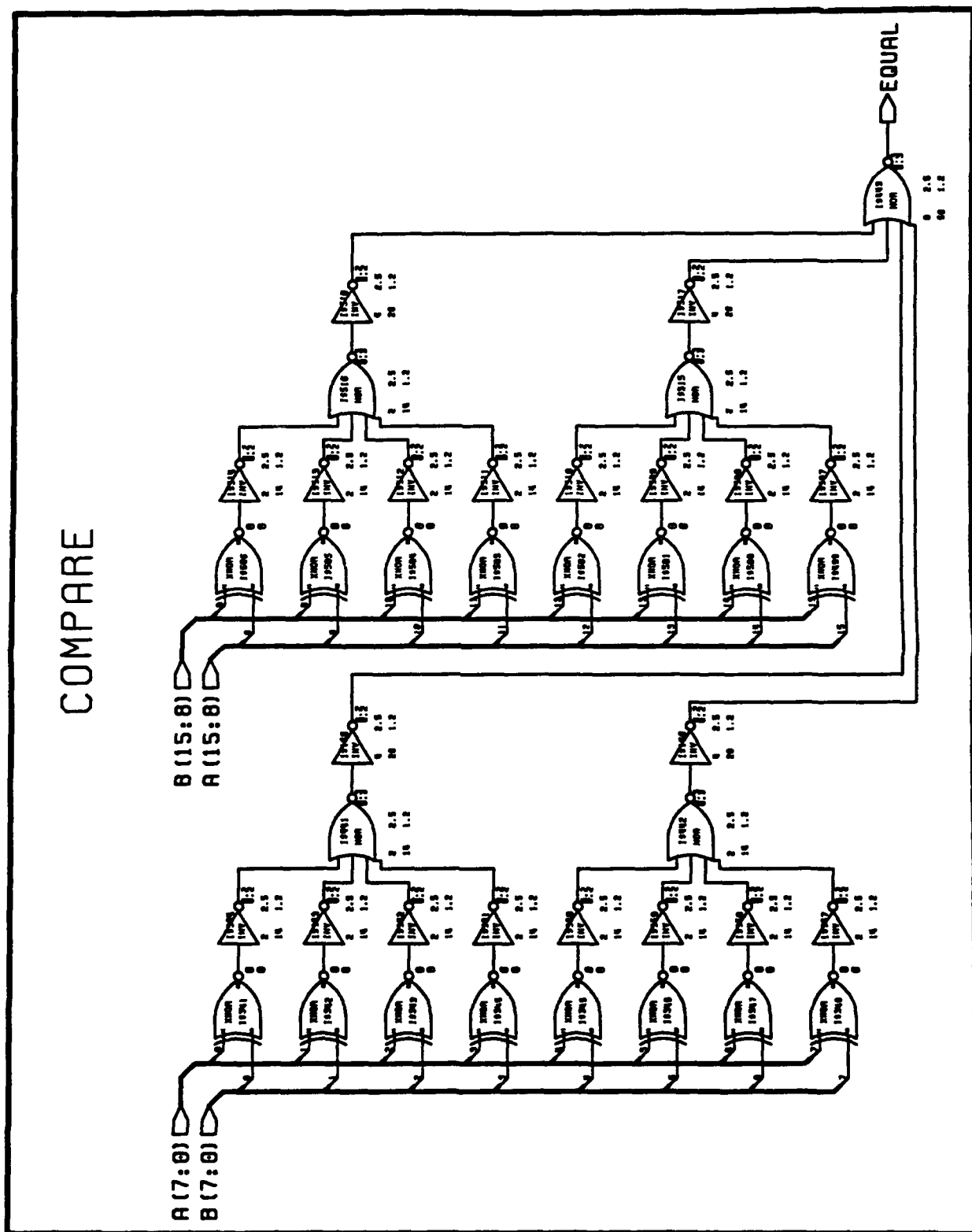
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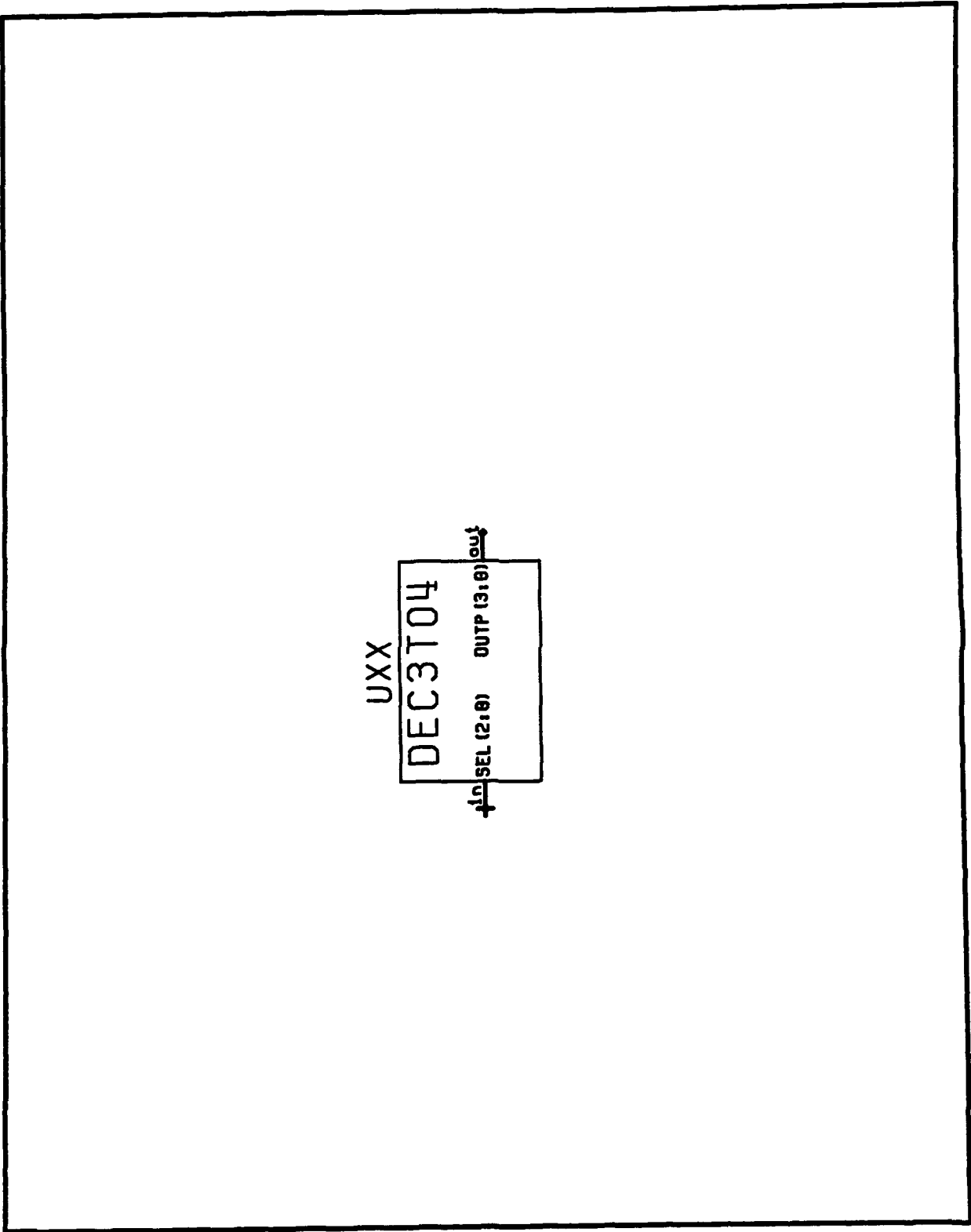




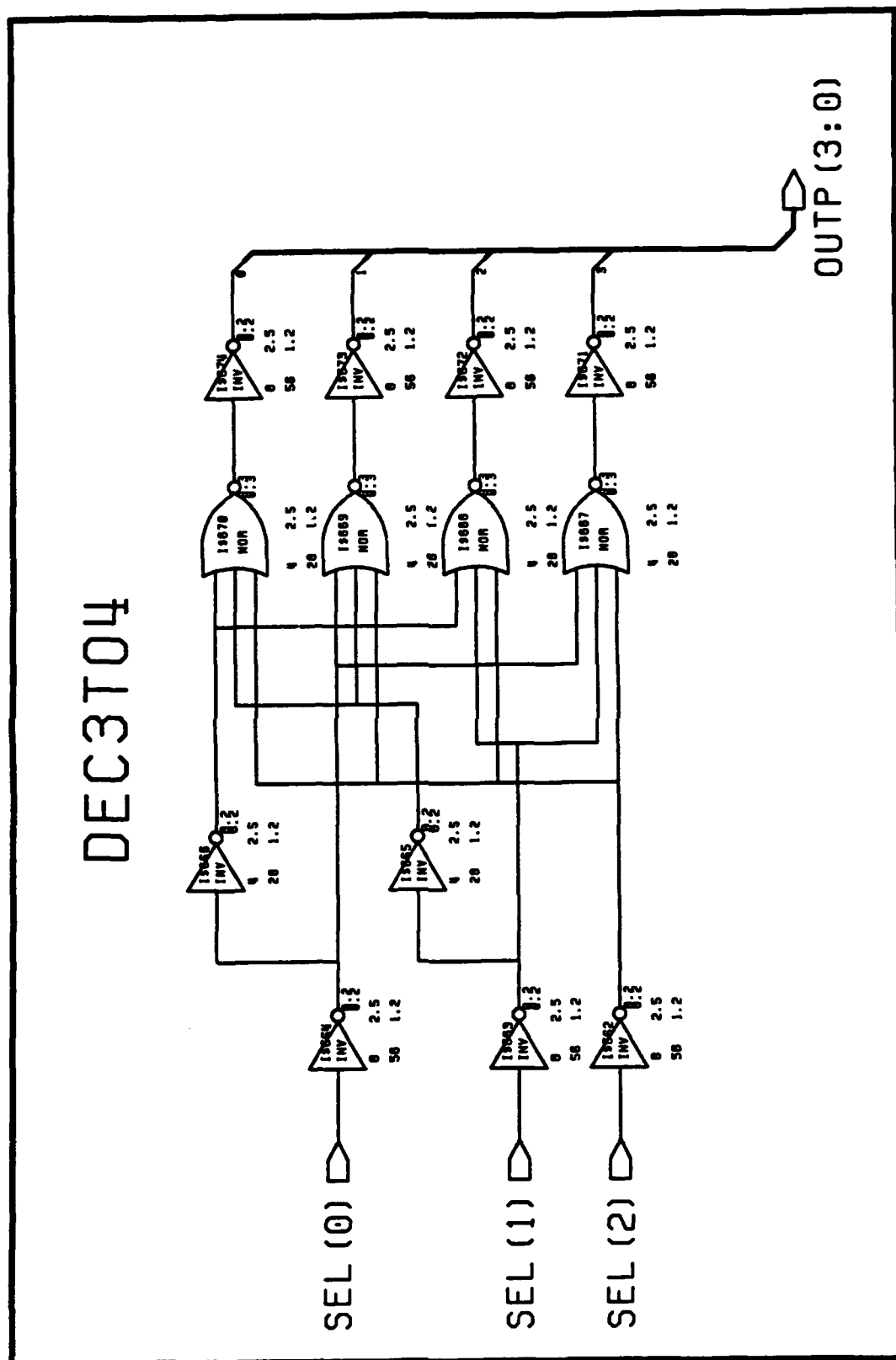










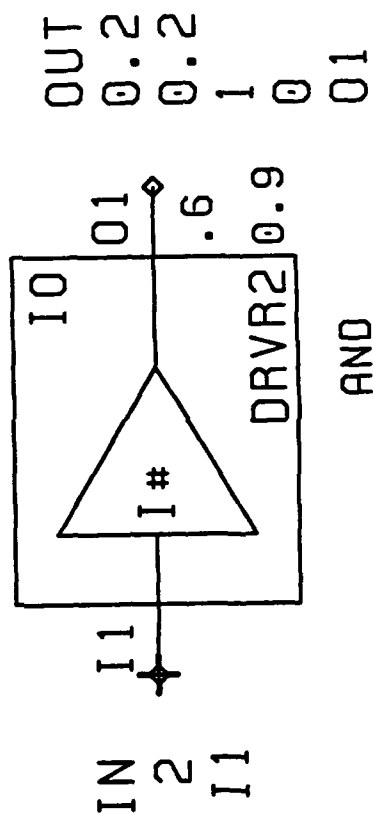


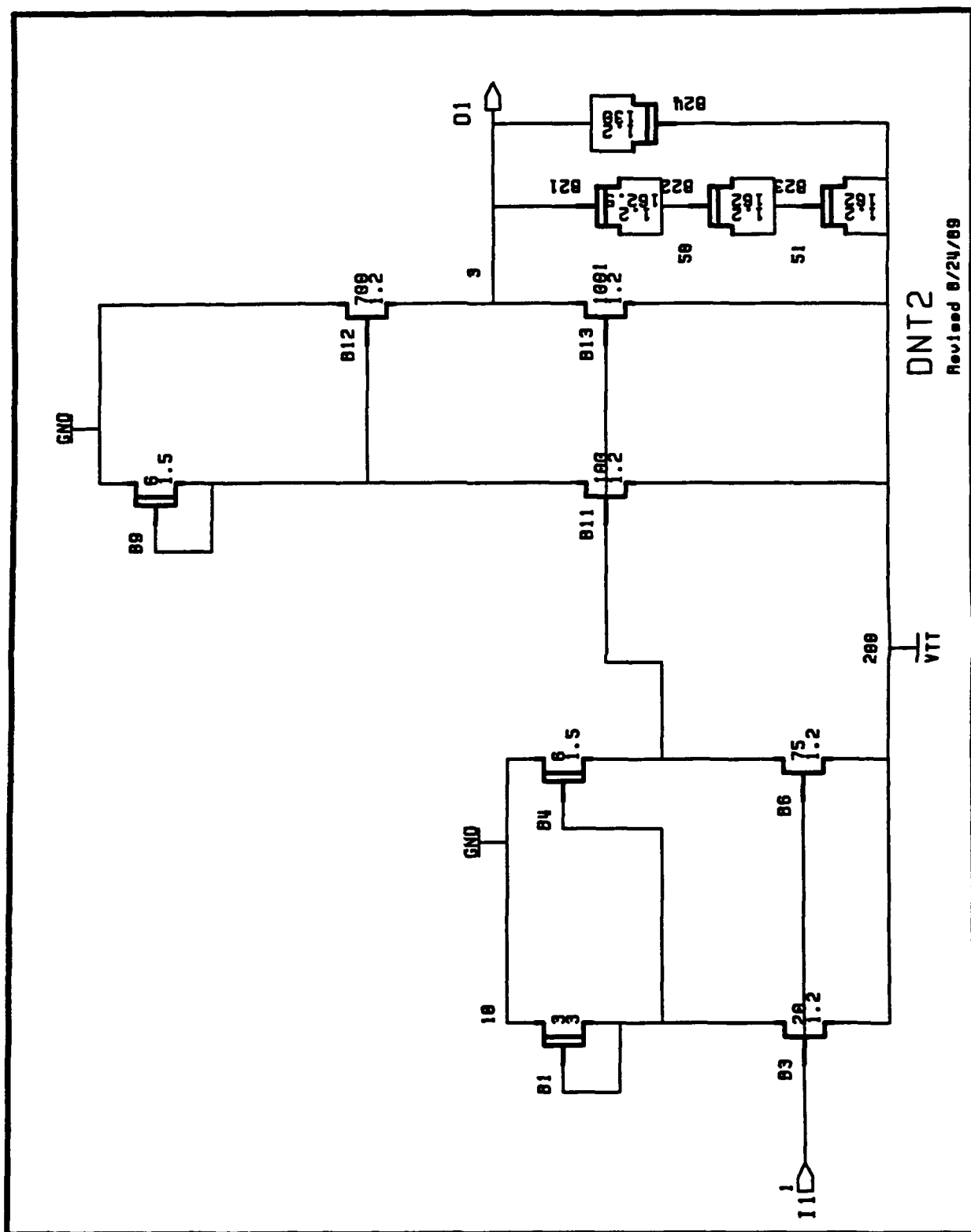
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Version 0.8

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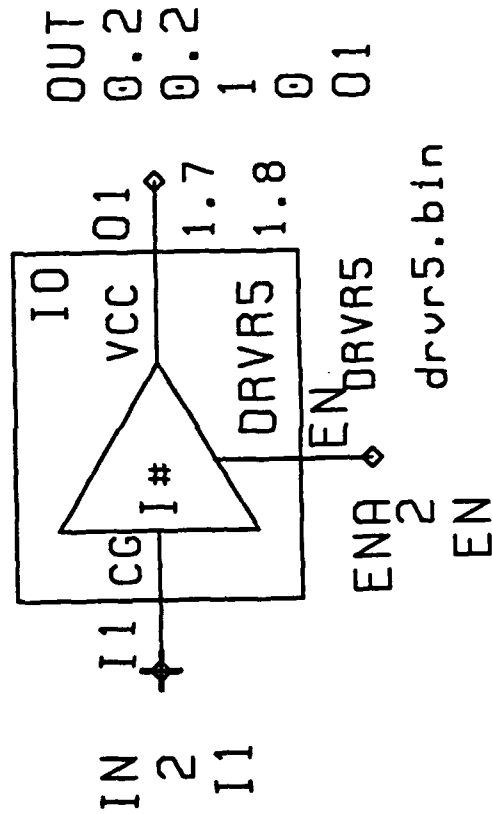


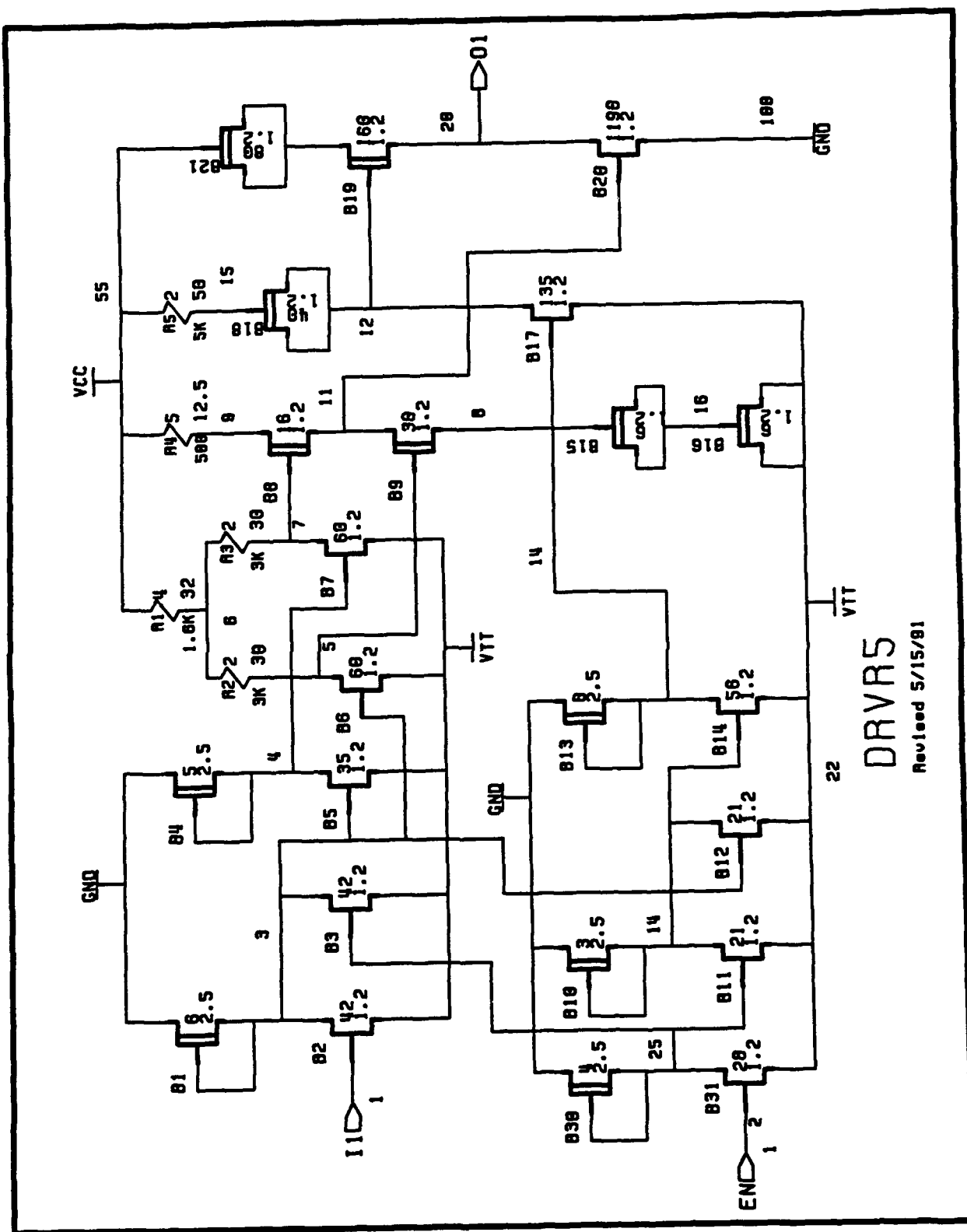
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Version 0.8

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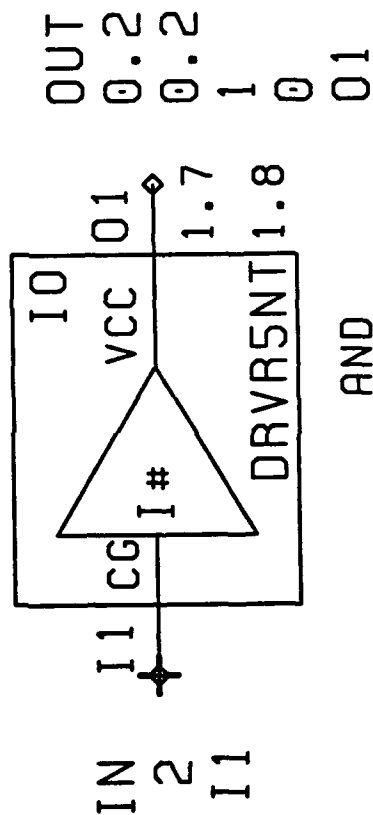


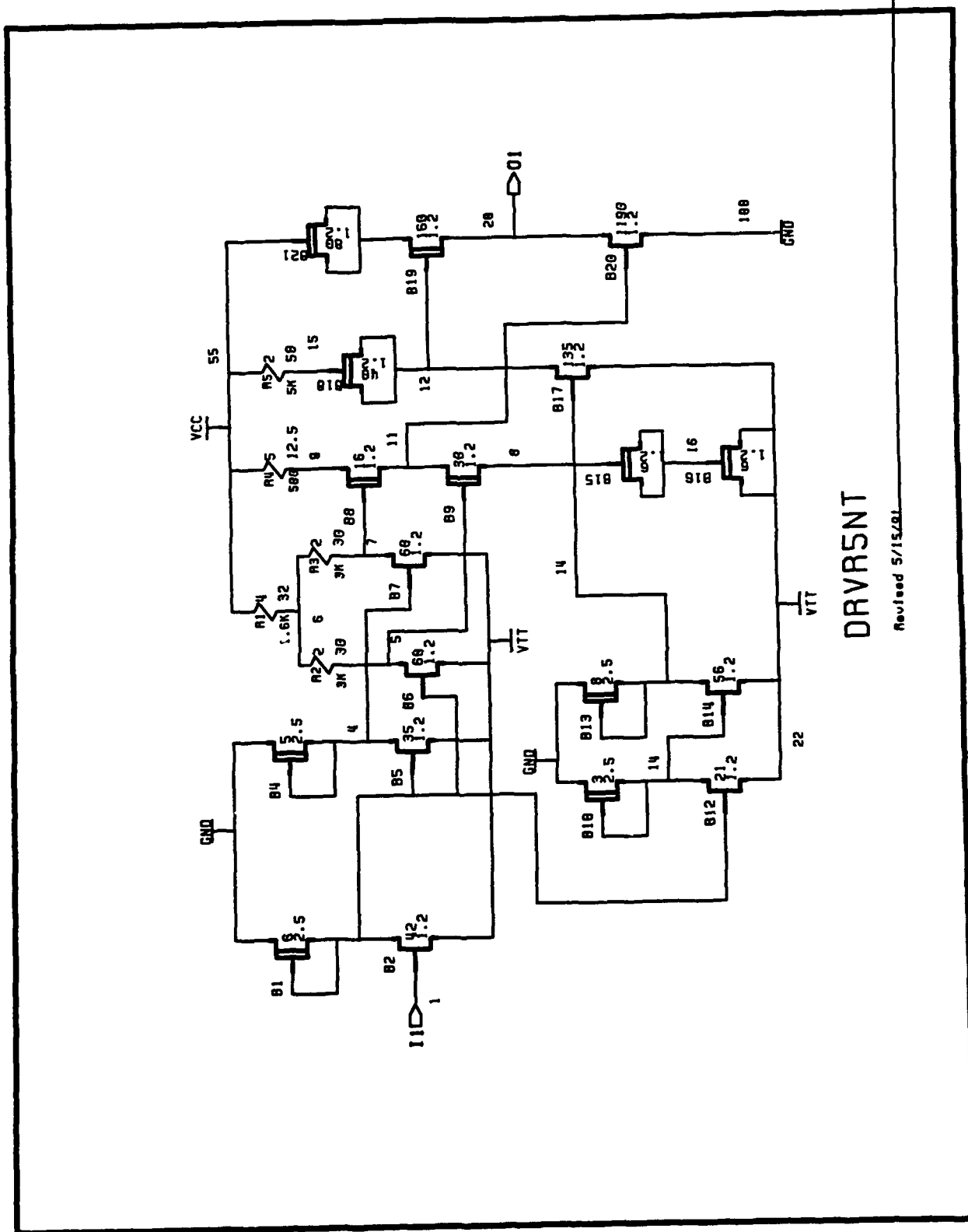
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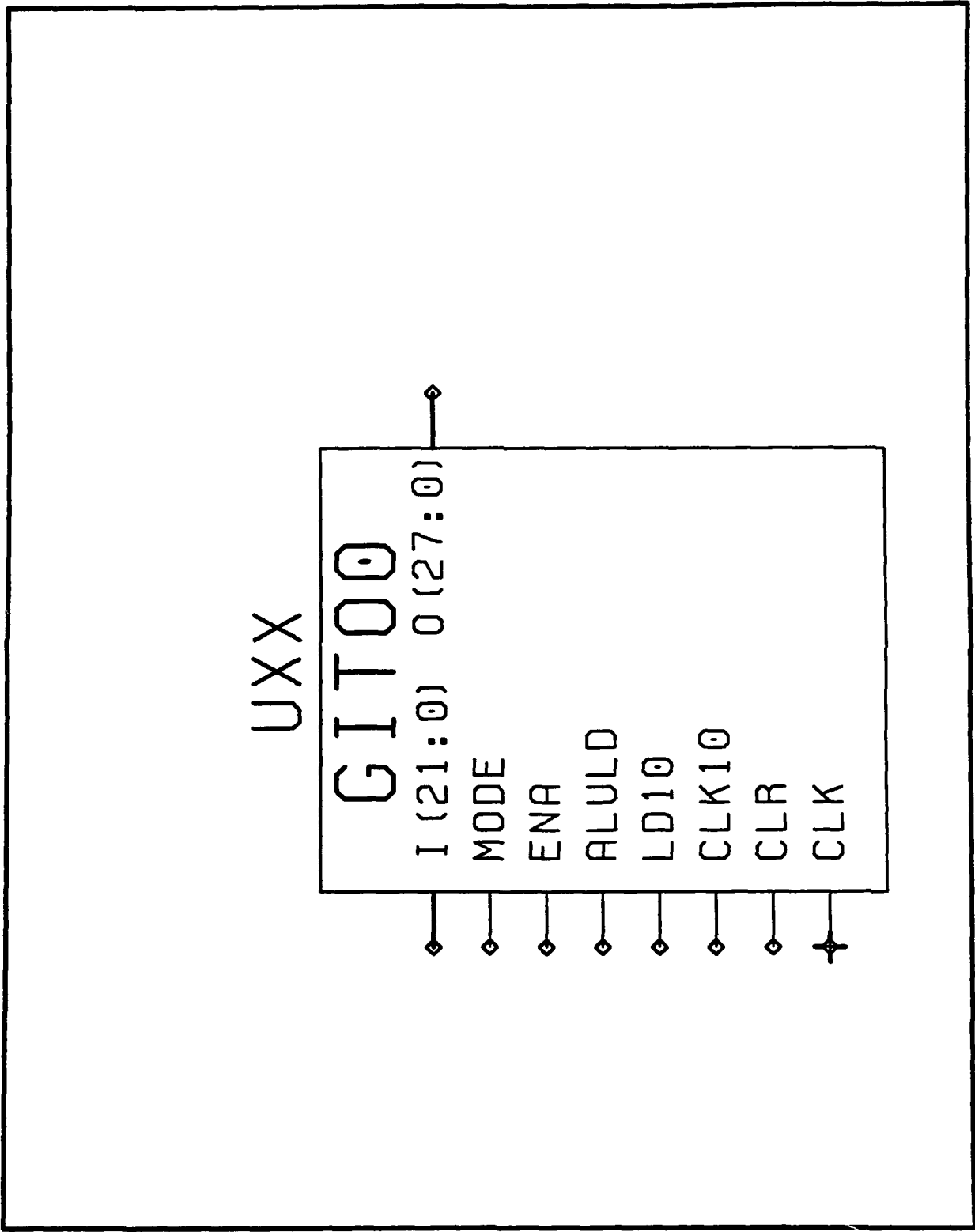
Version 0.8

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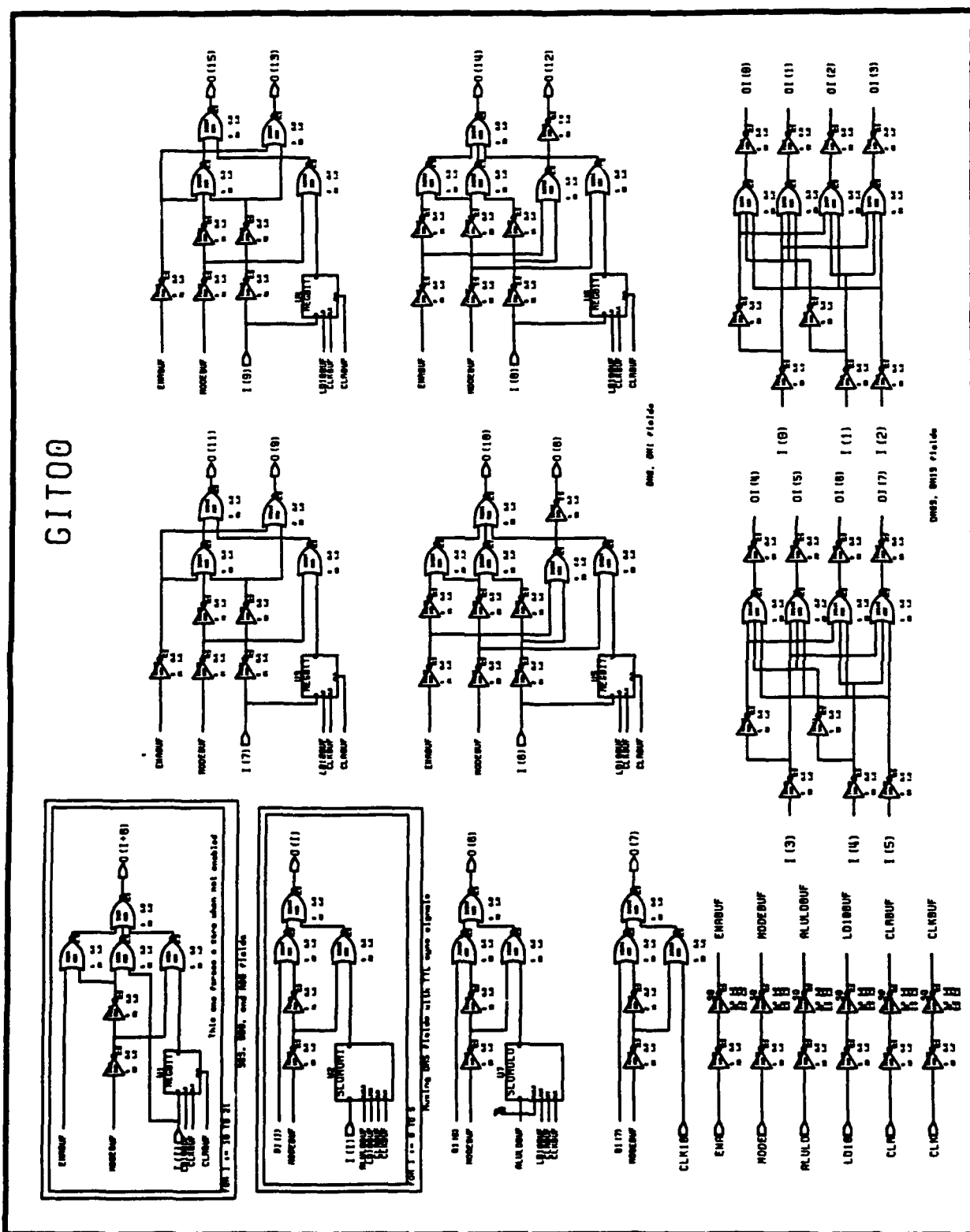
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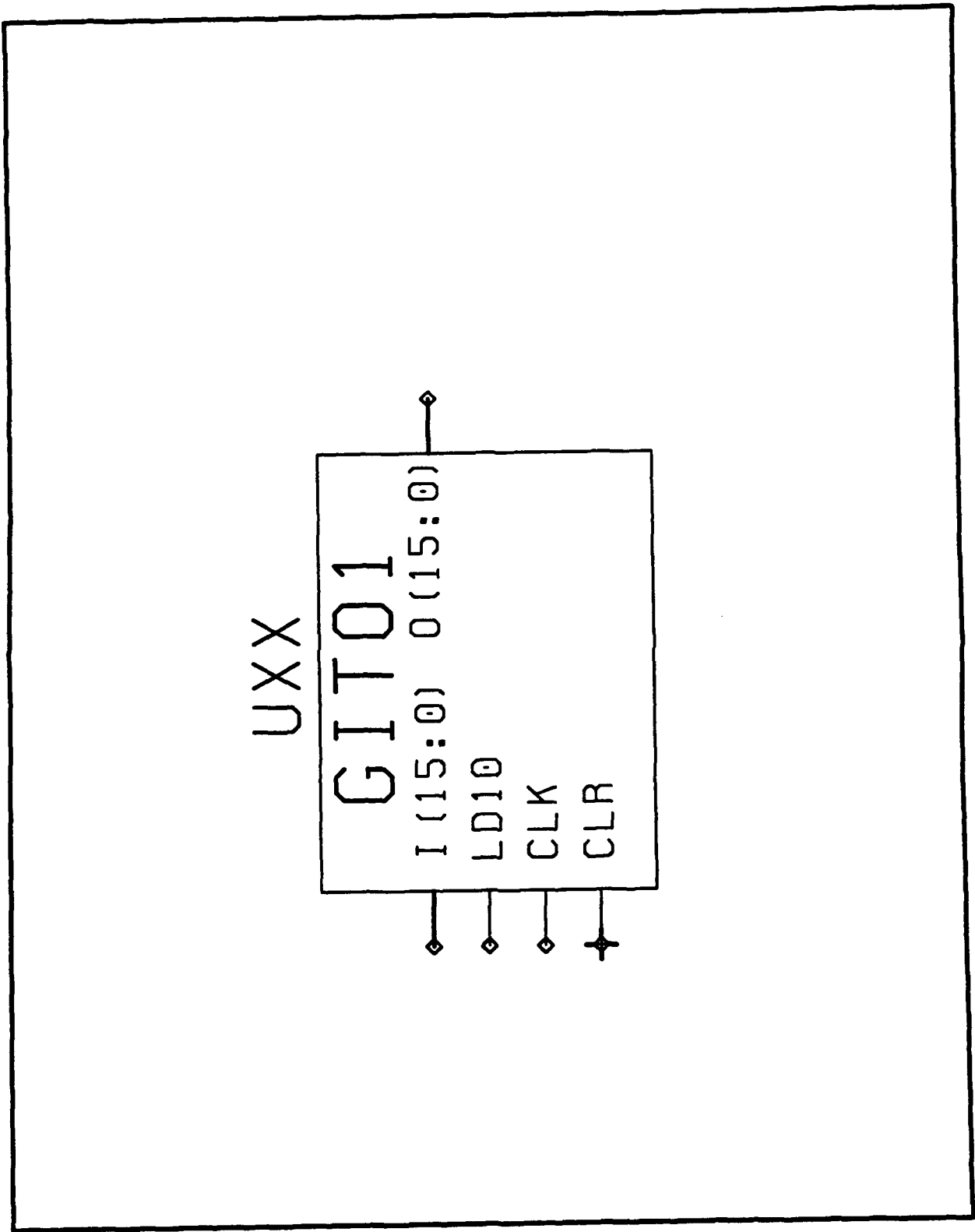




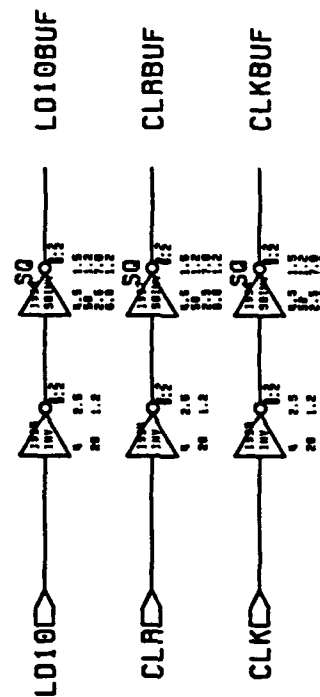
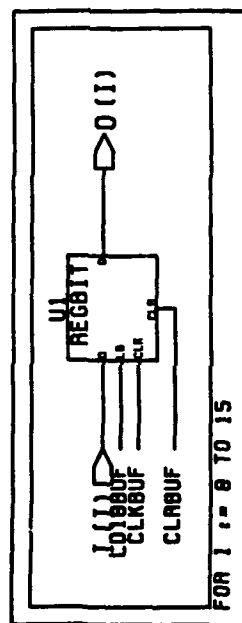


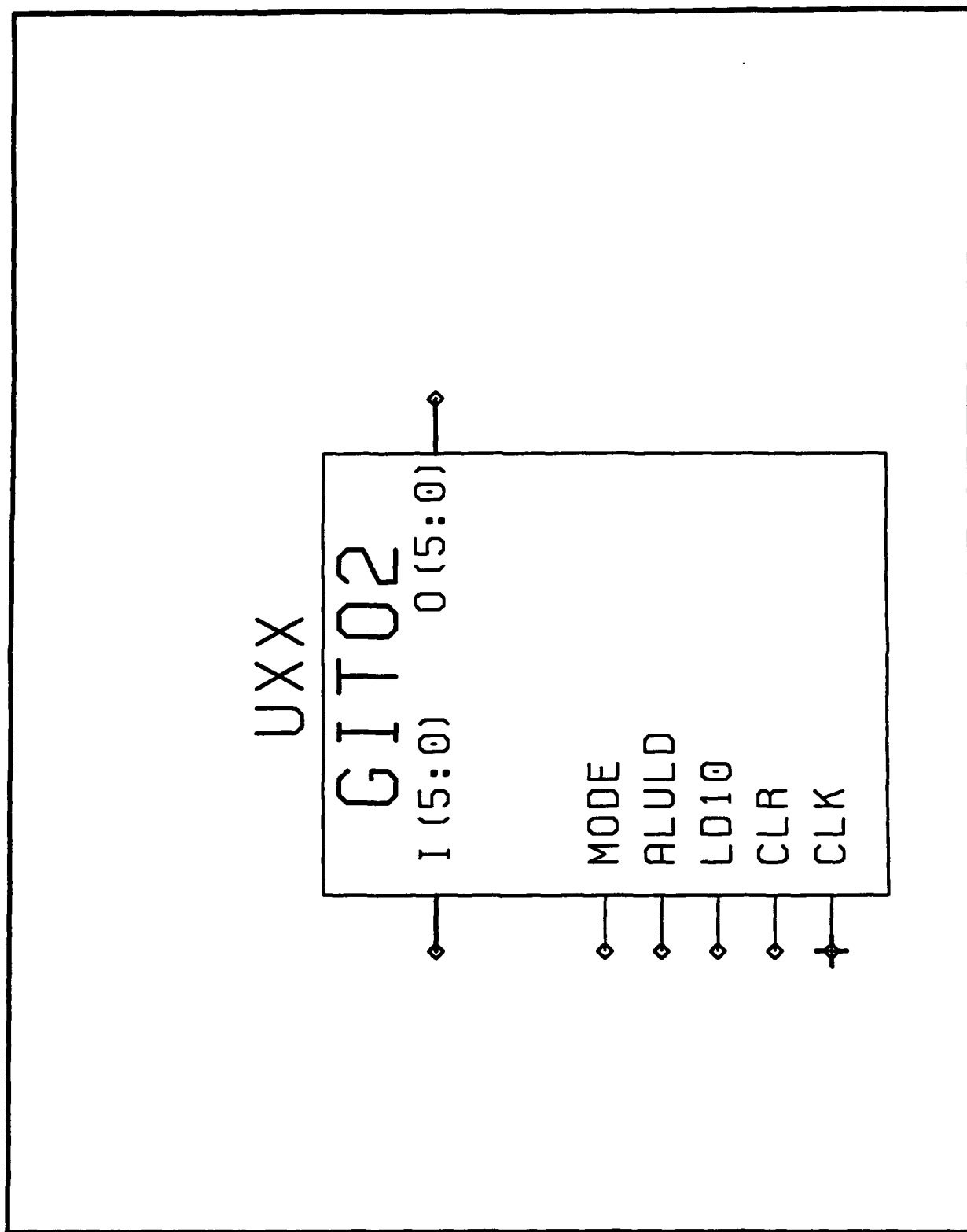


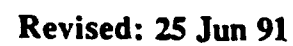


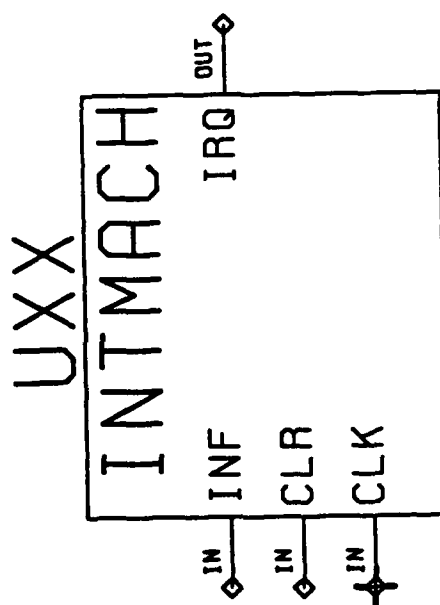


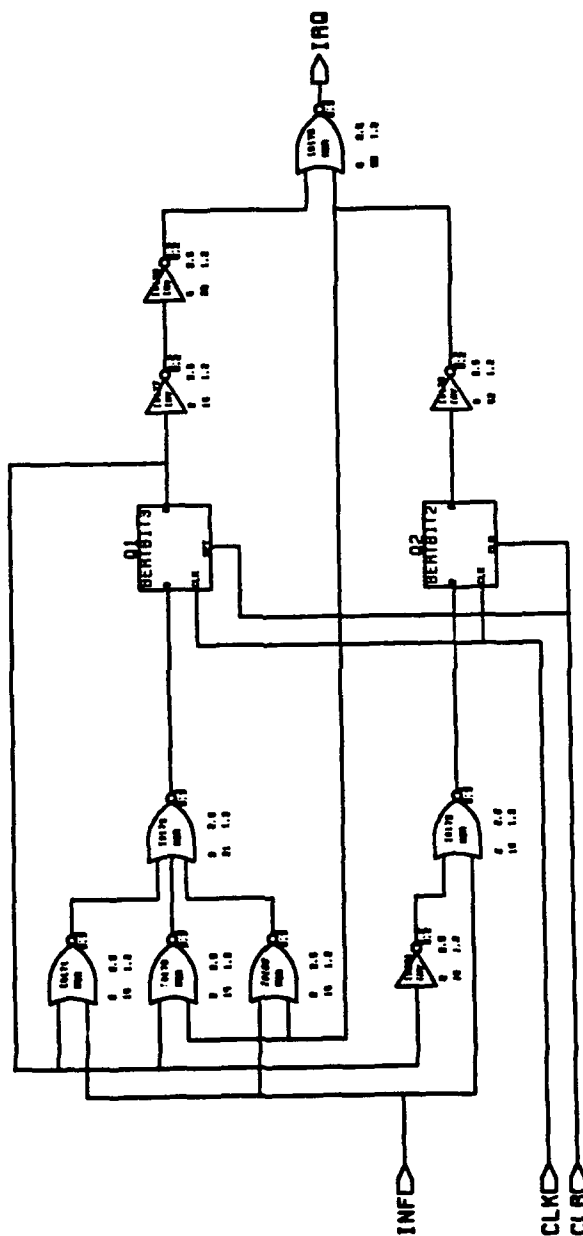
G1T01: DEST AND ADDR BUSSES





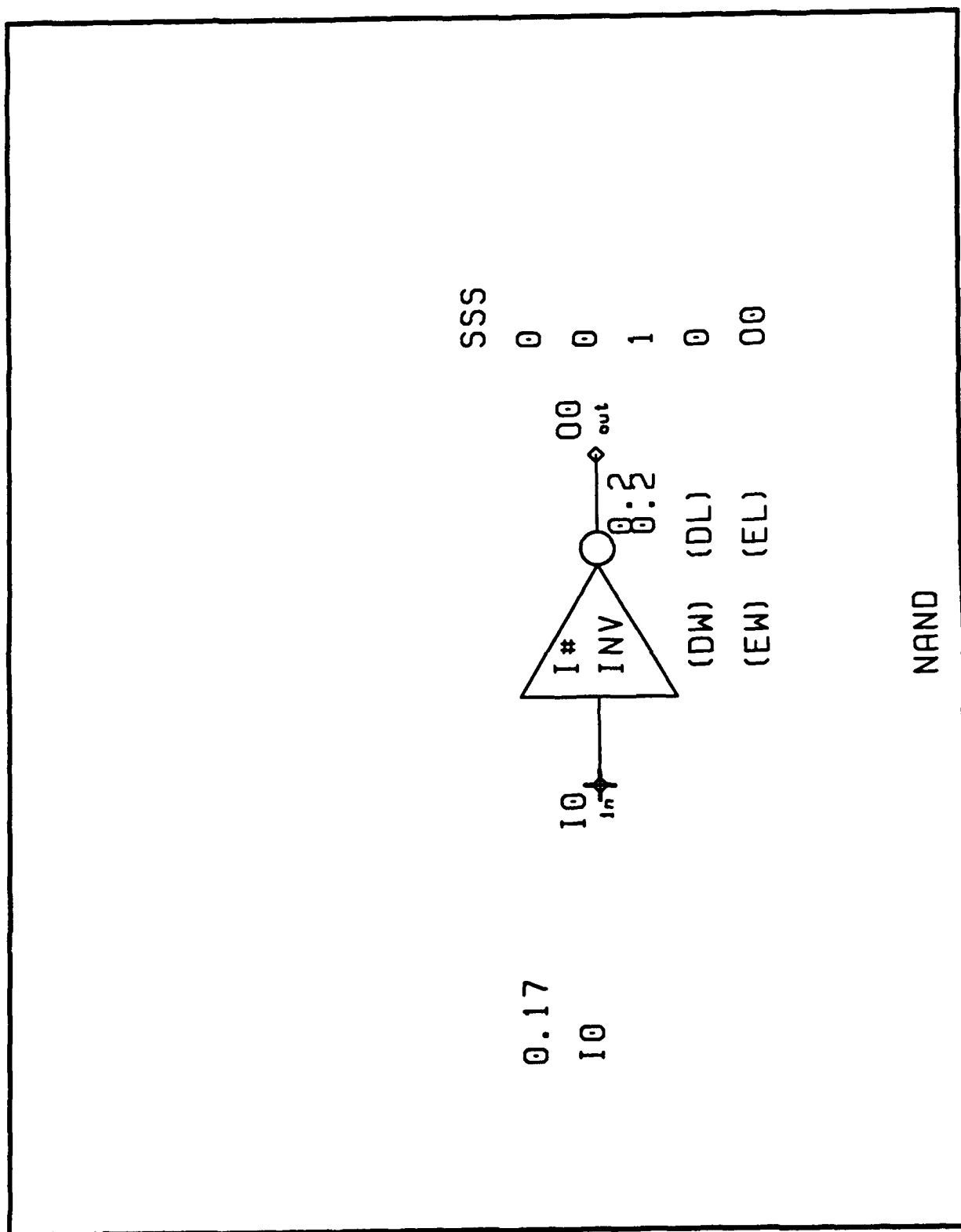




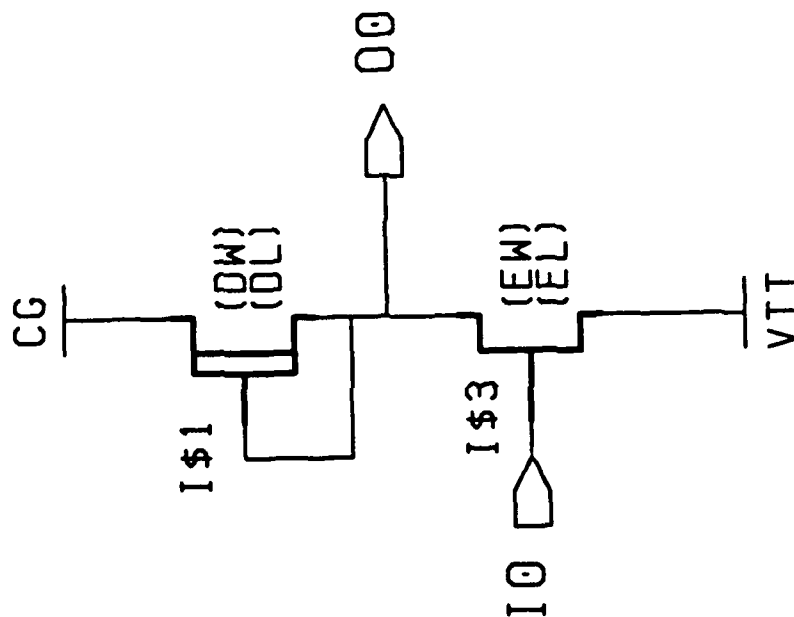


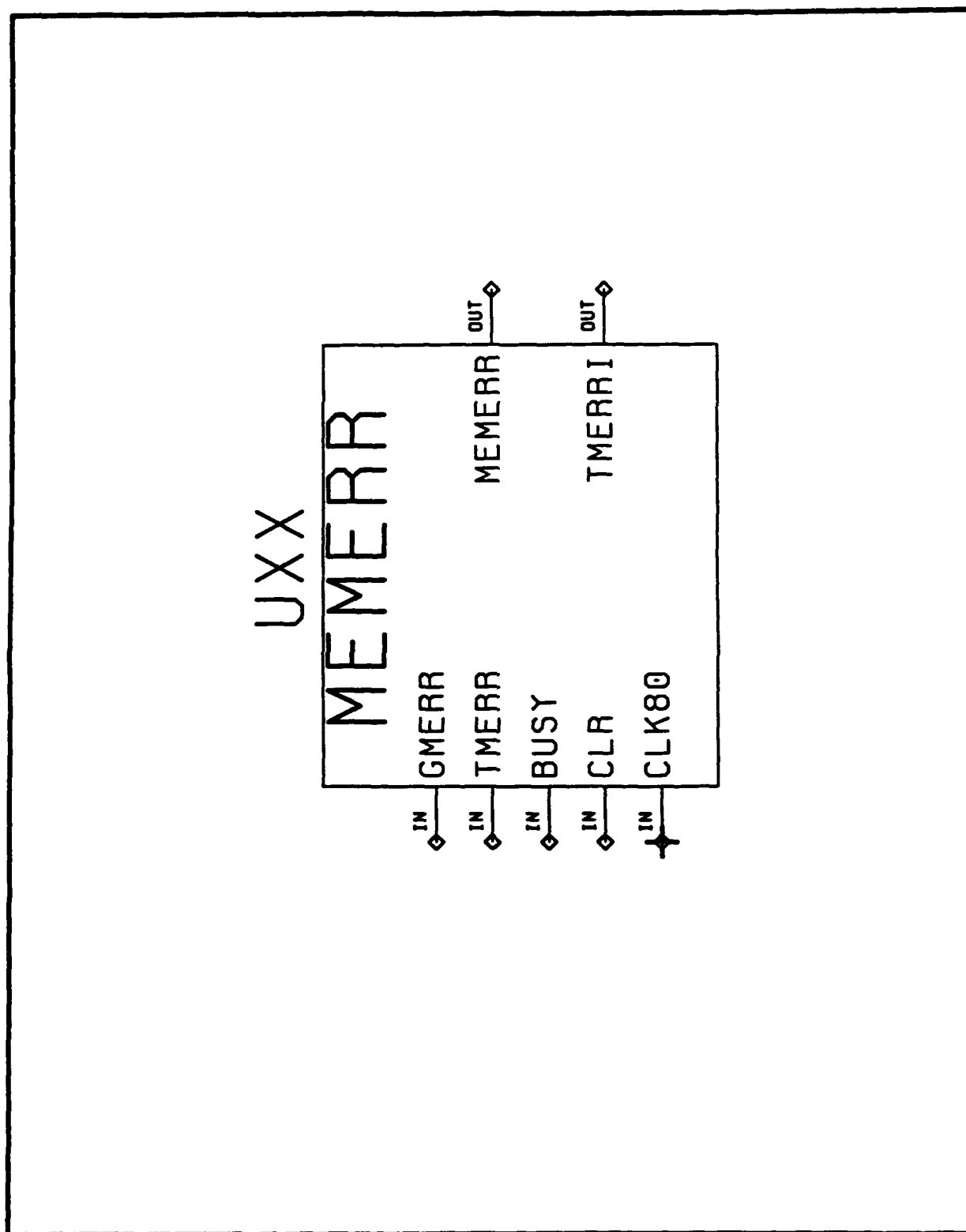
NOTE: Register 01 has a SET instead of a CLR Input

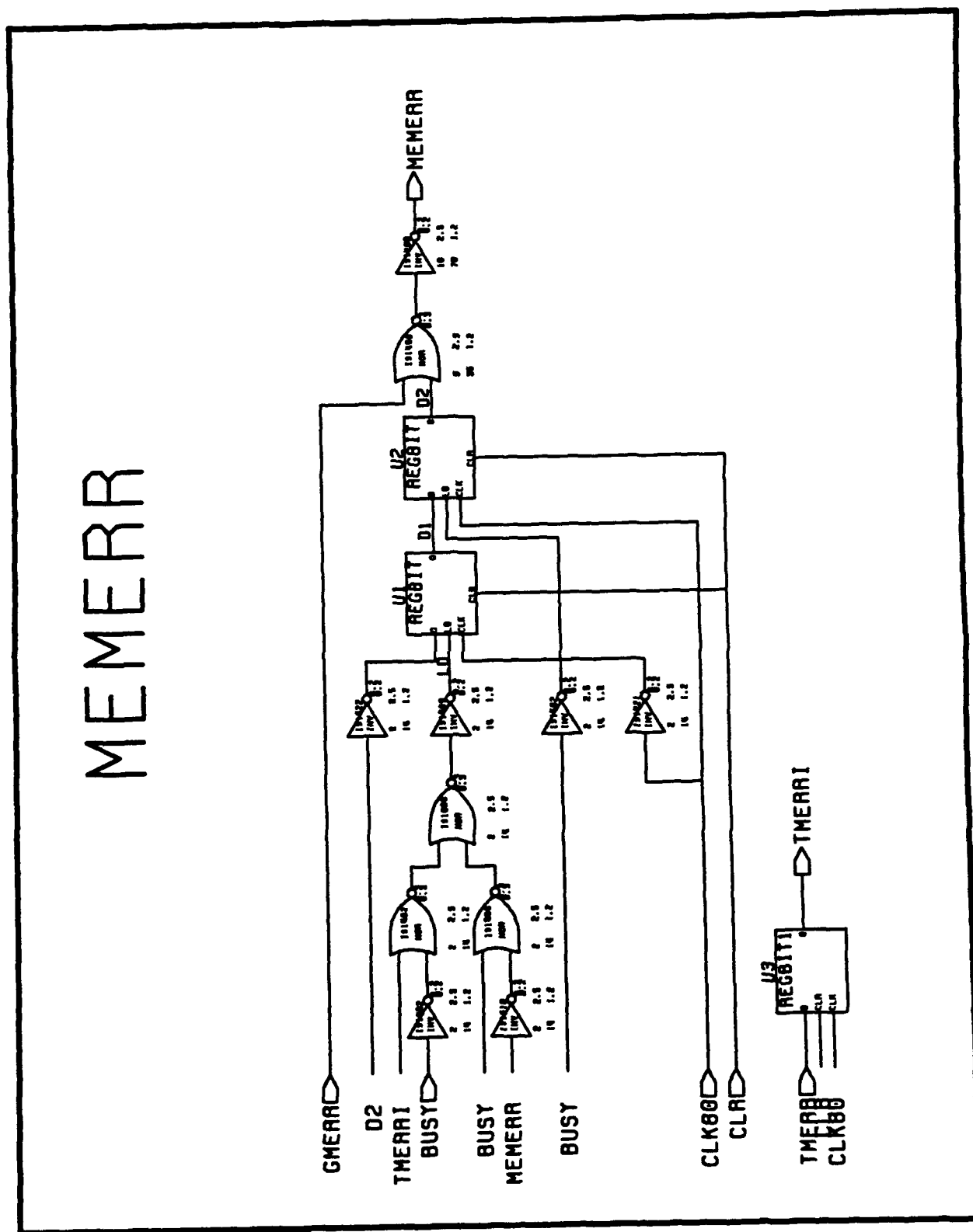
INTMACH: generation of interrupt

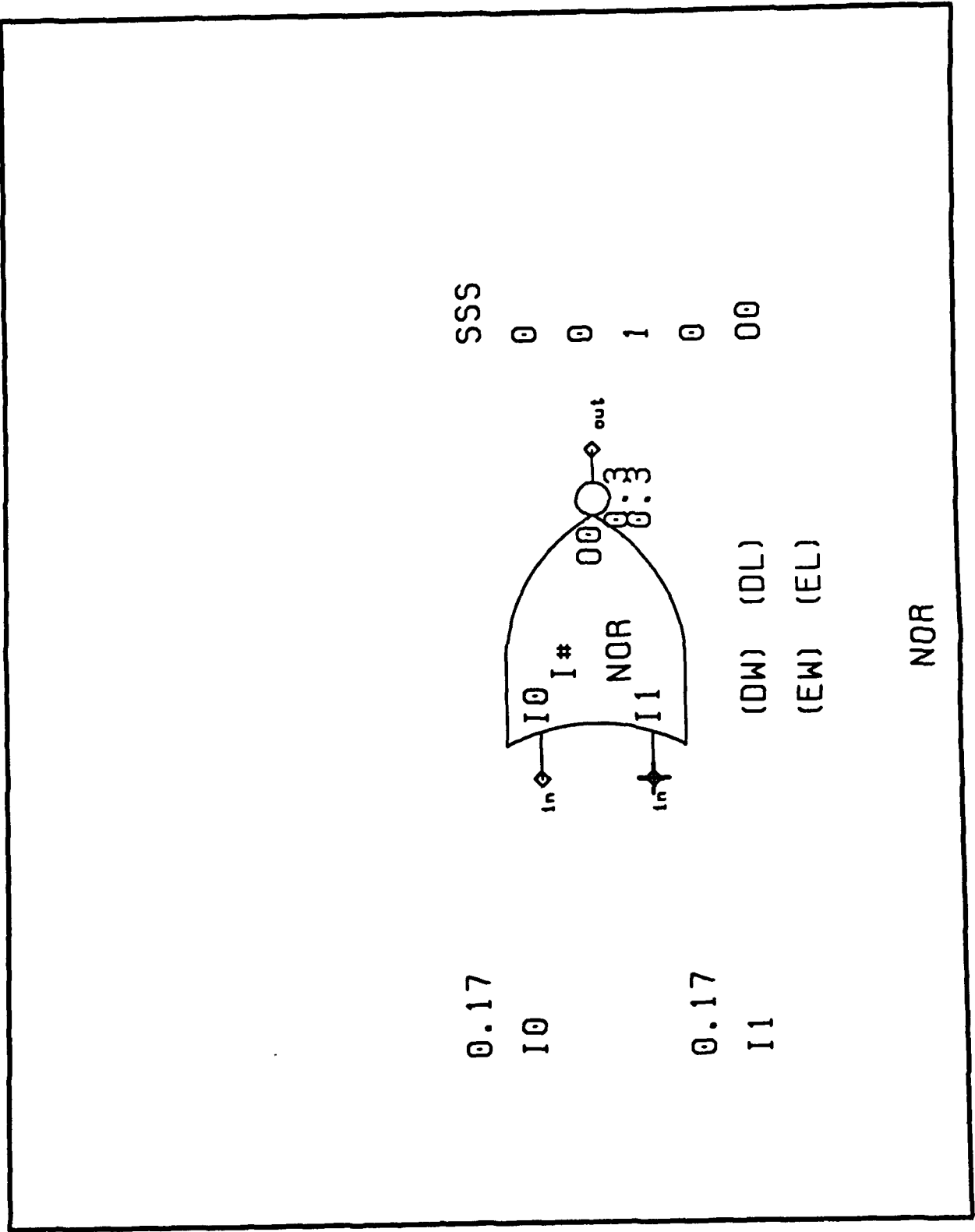


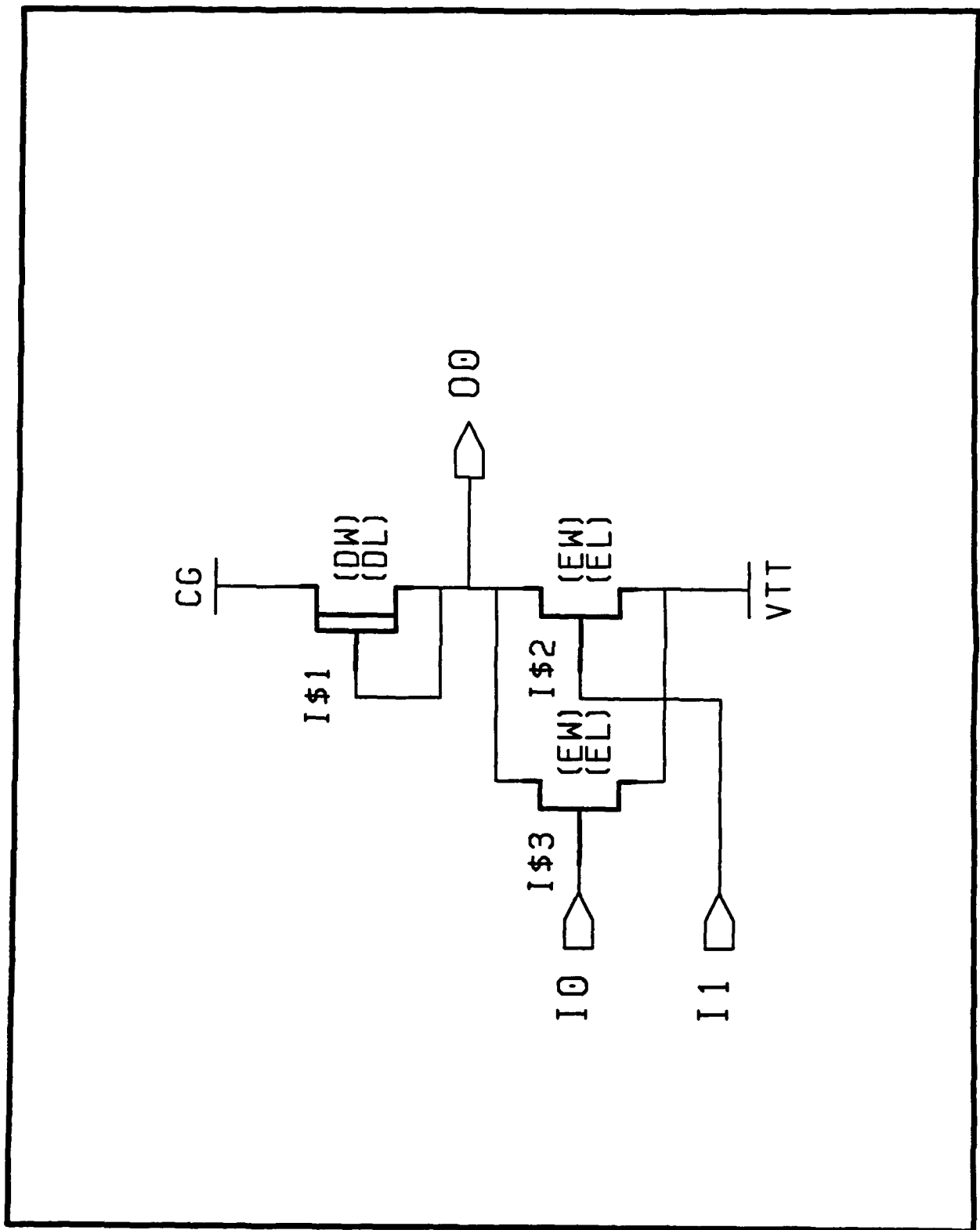


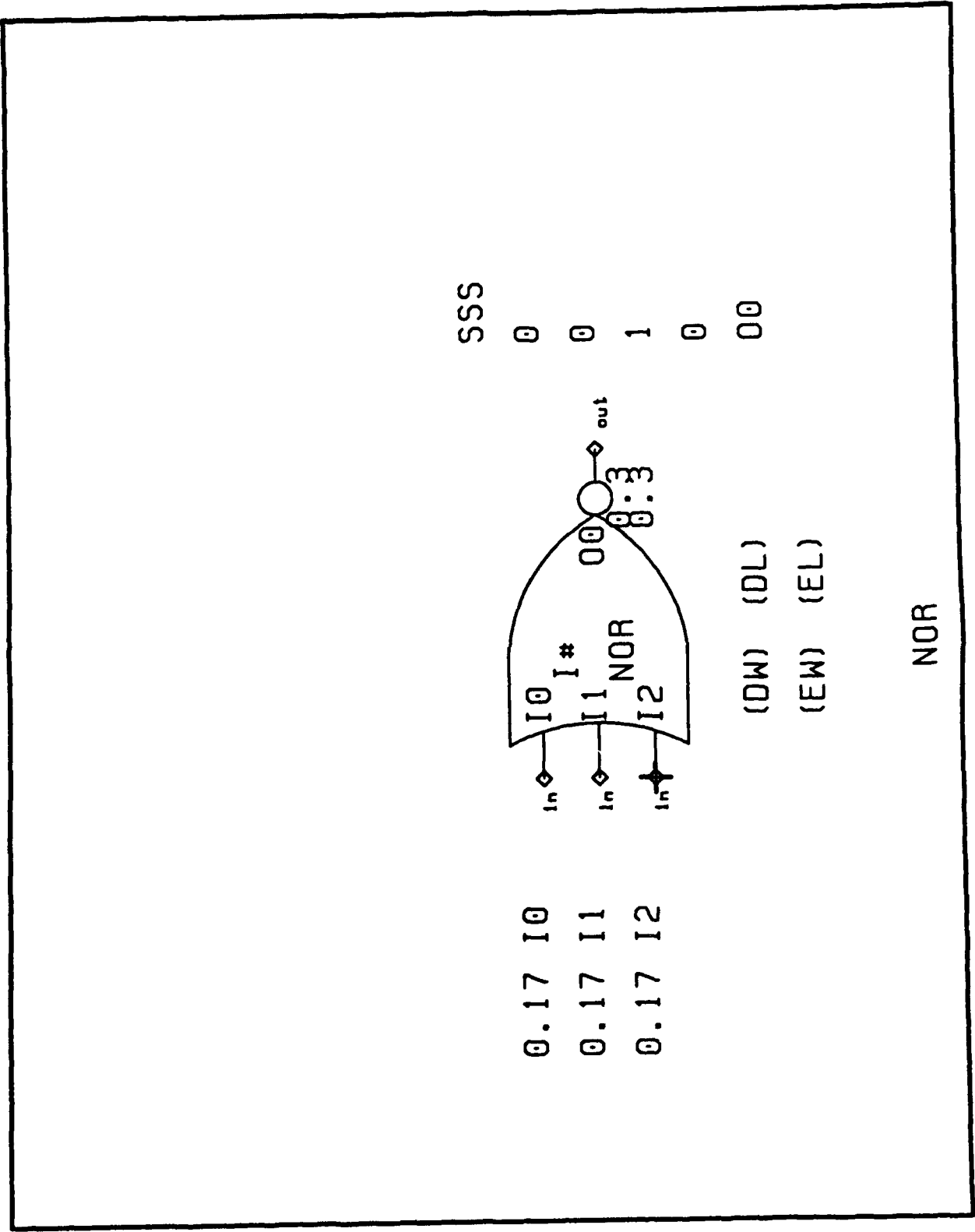


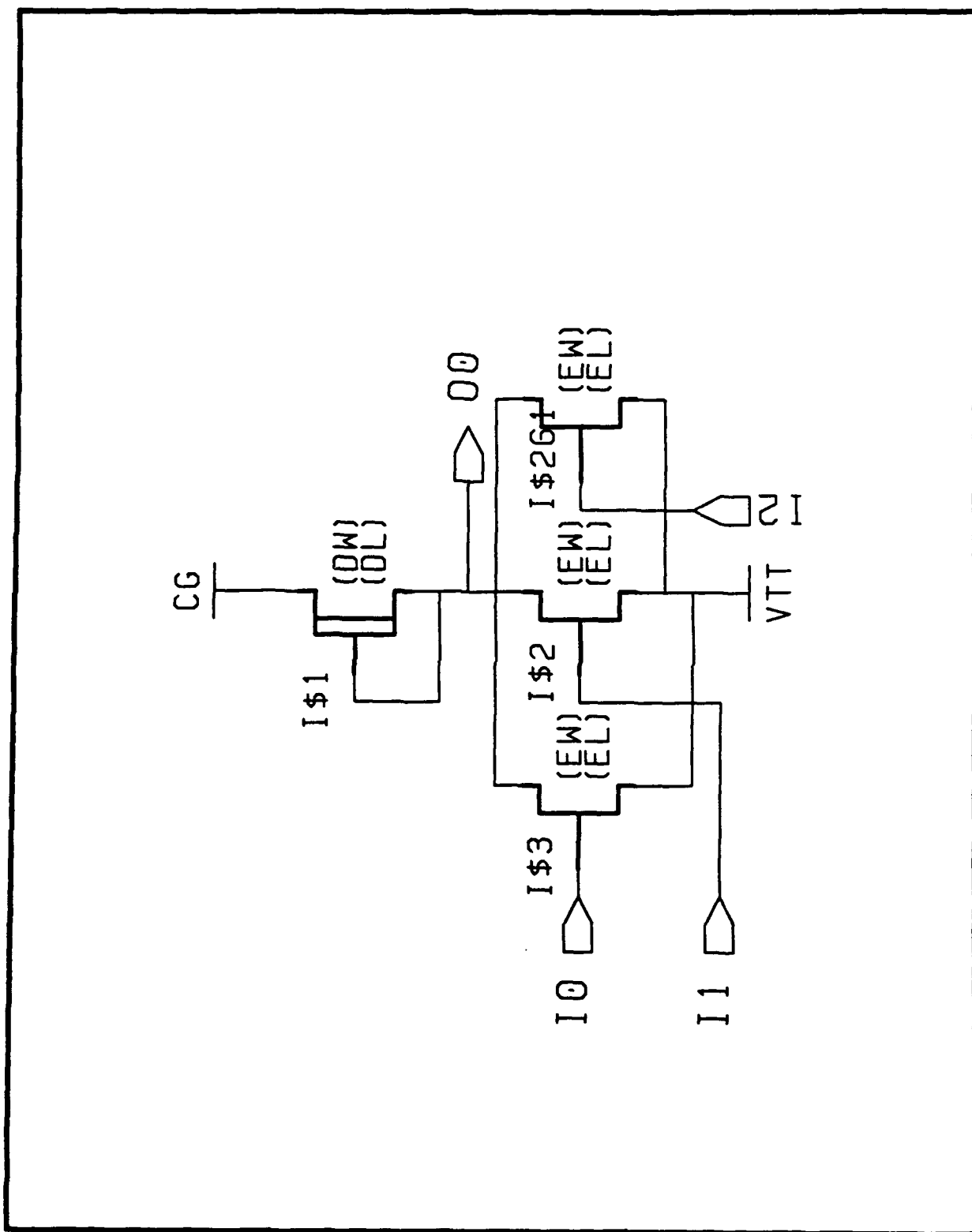


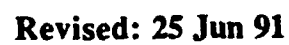




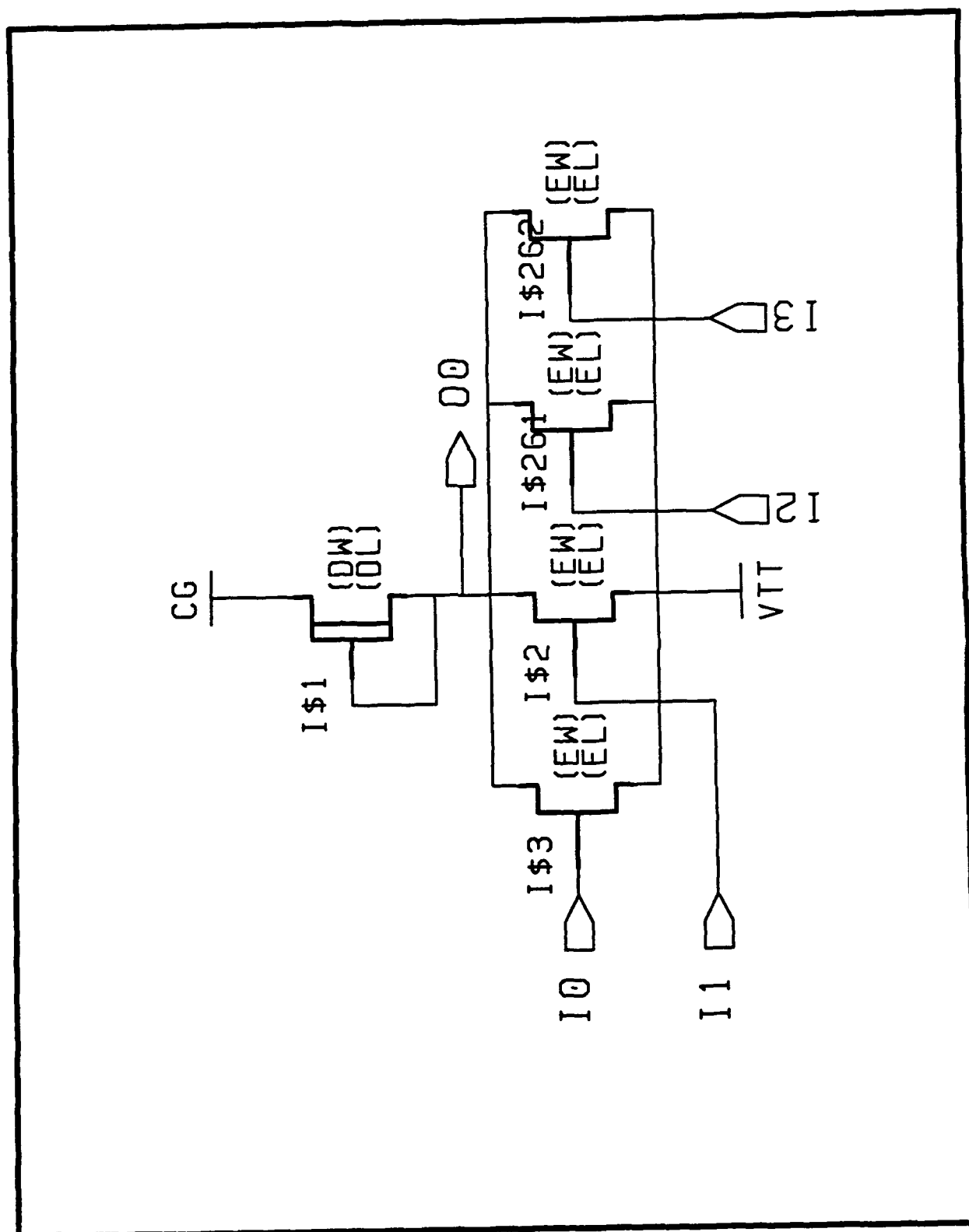


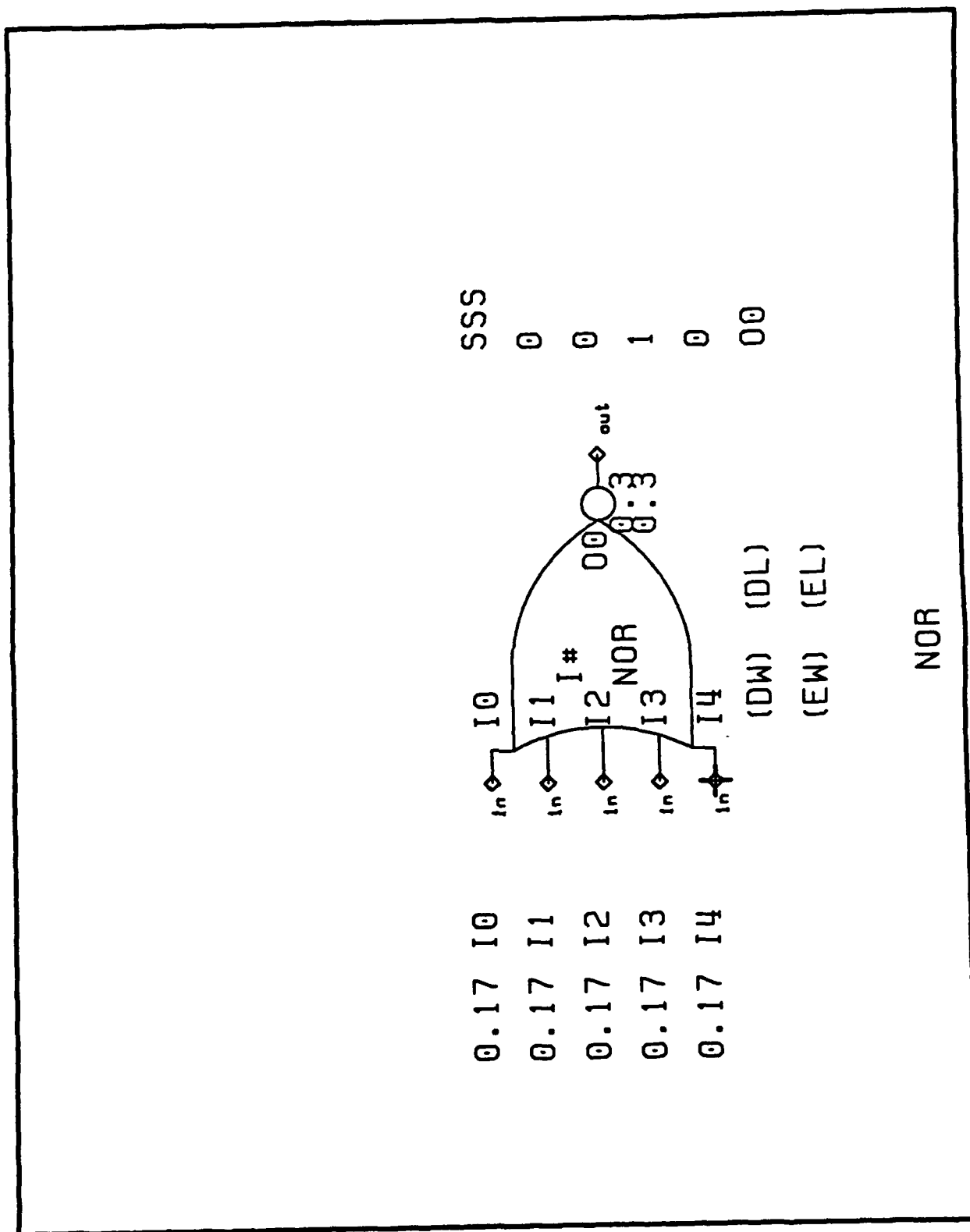




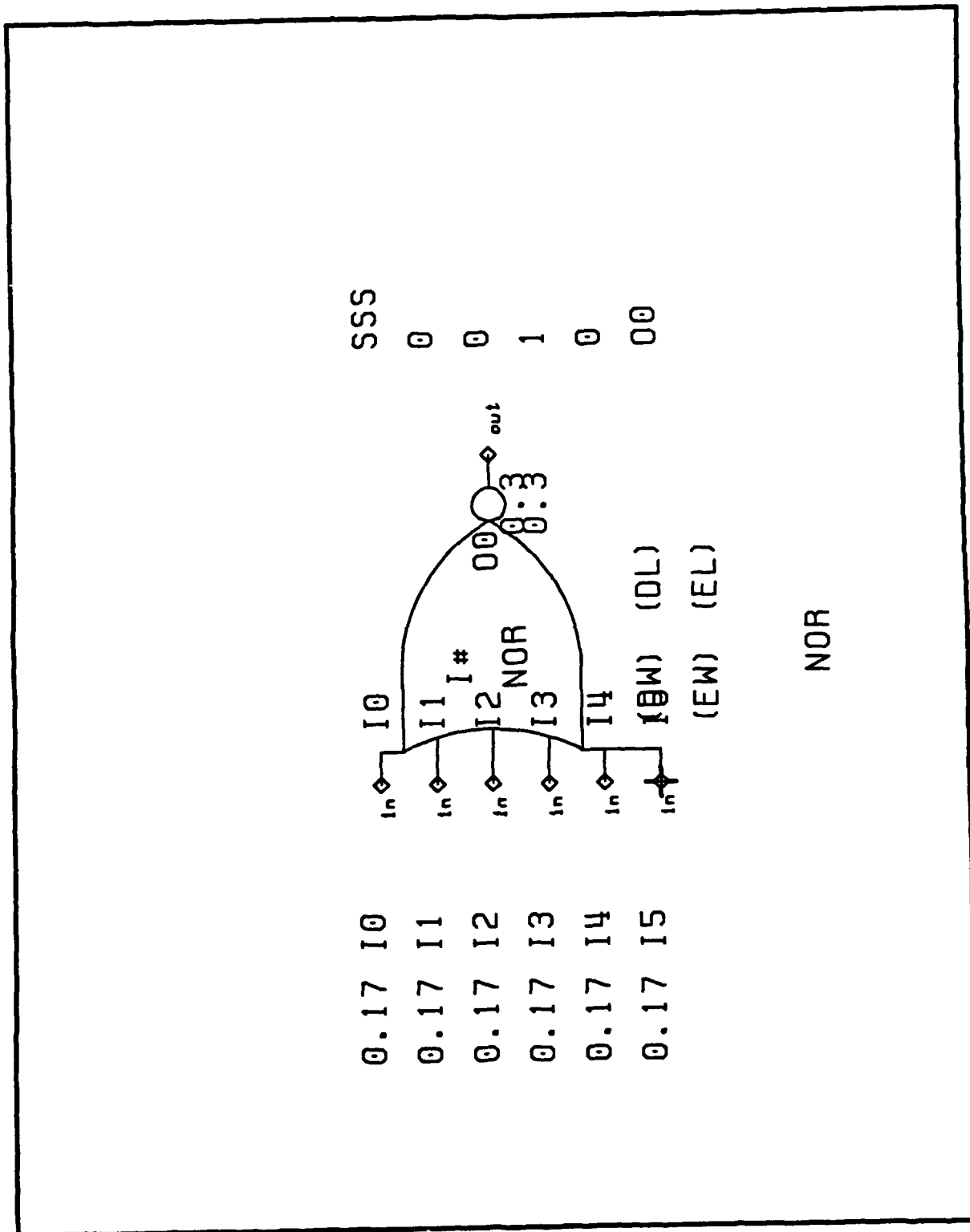


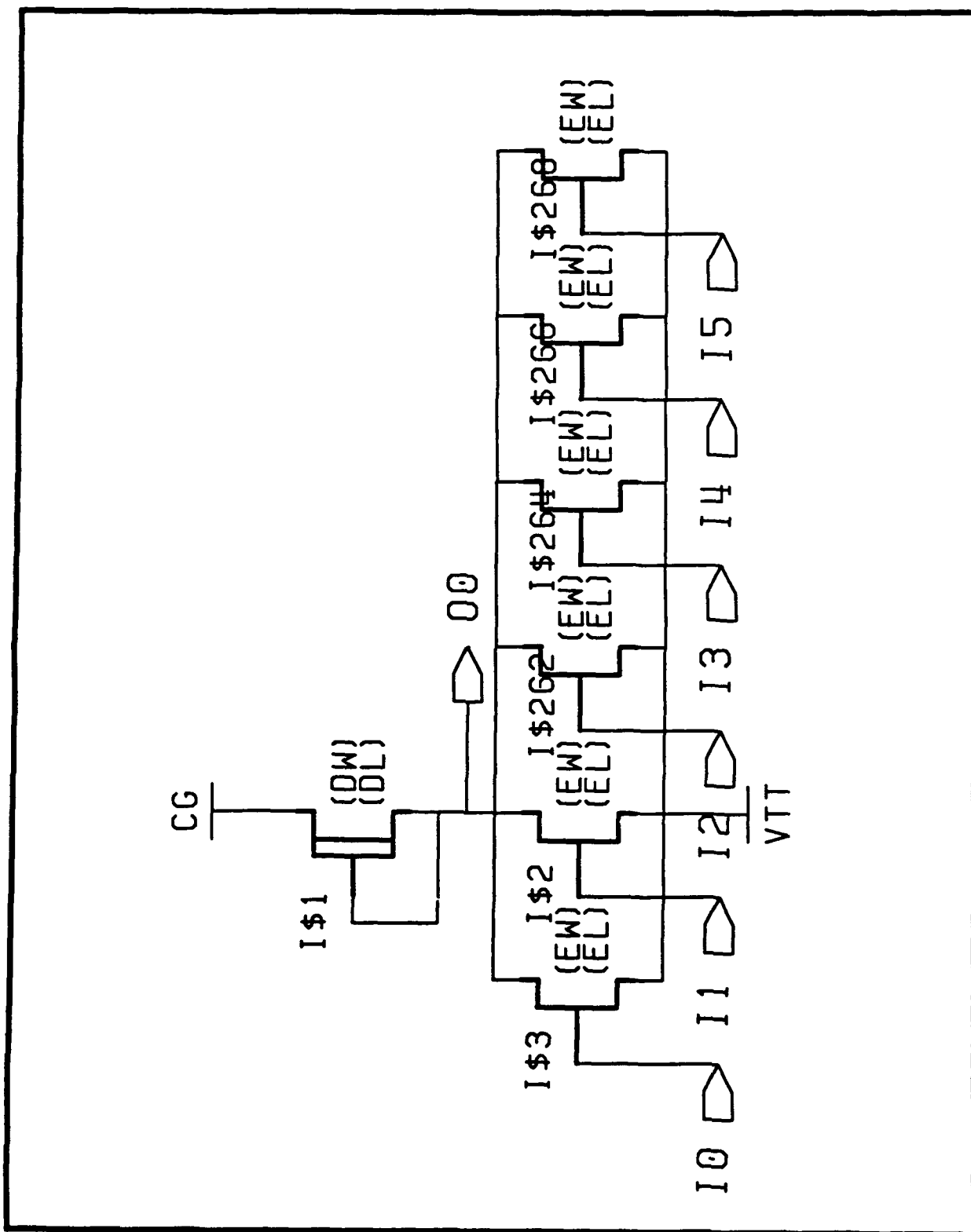


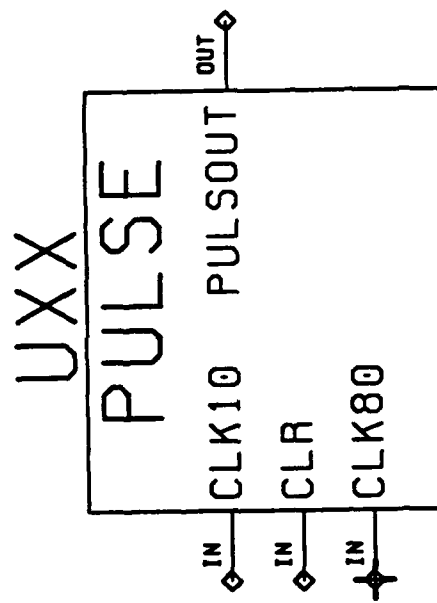


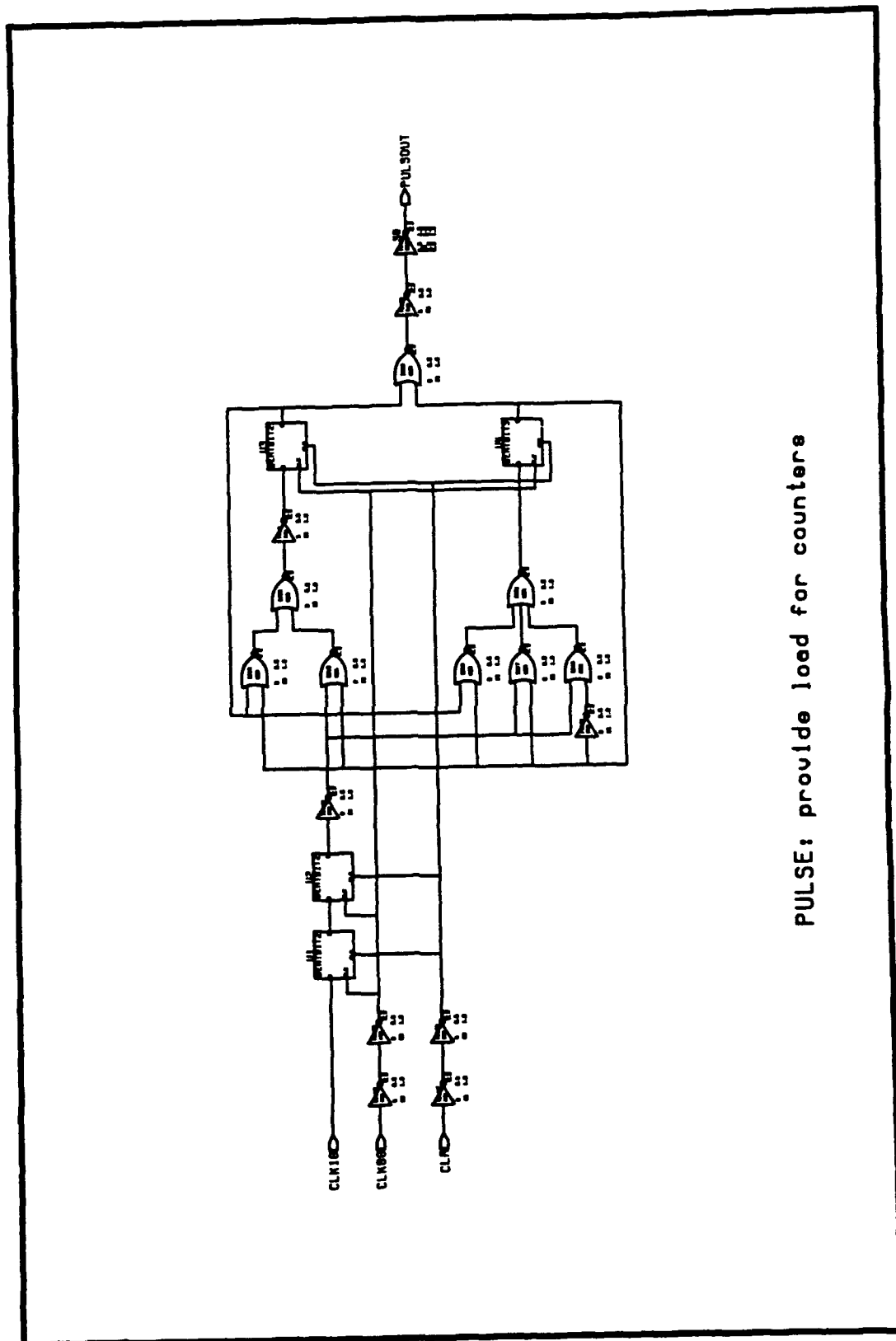












PULSE: provide load for counters

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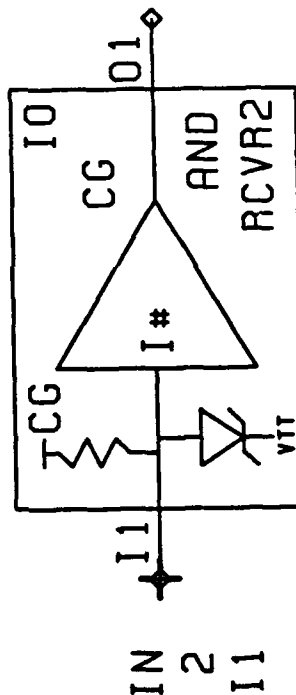
NAME:

RCVR2

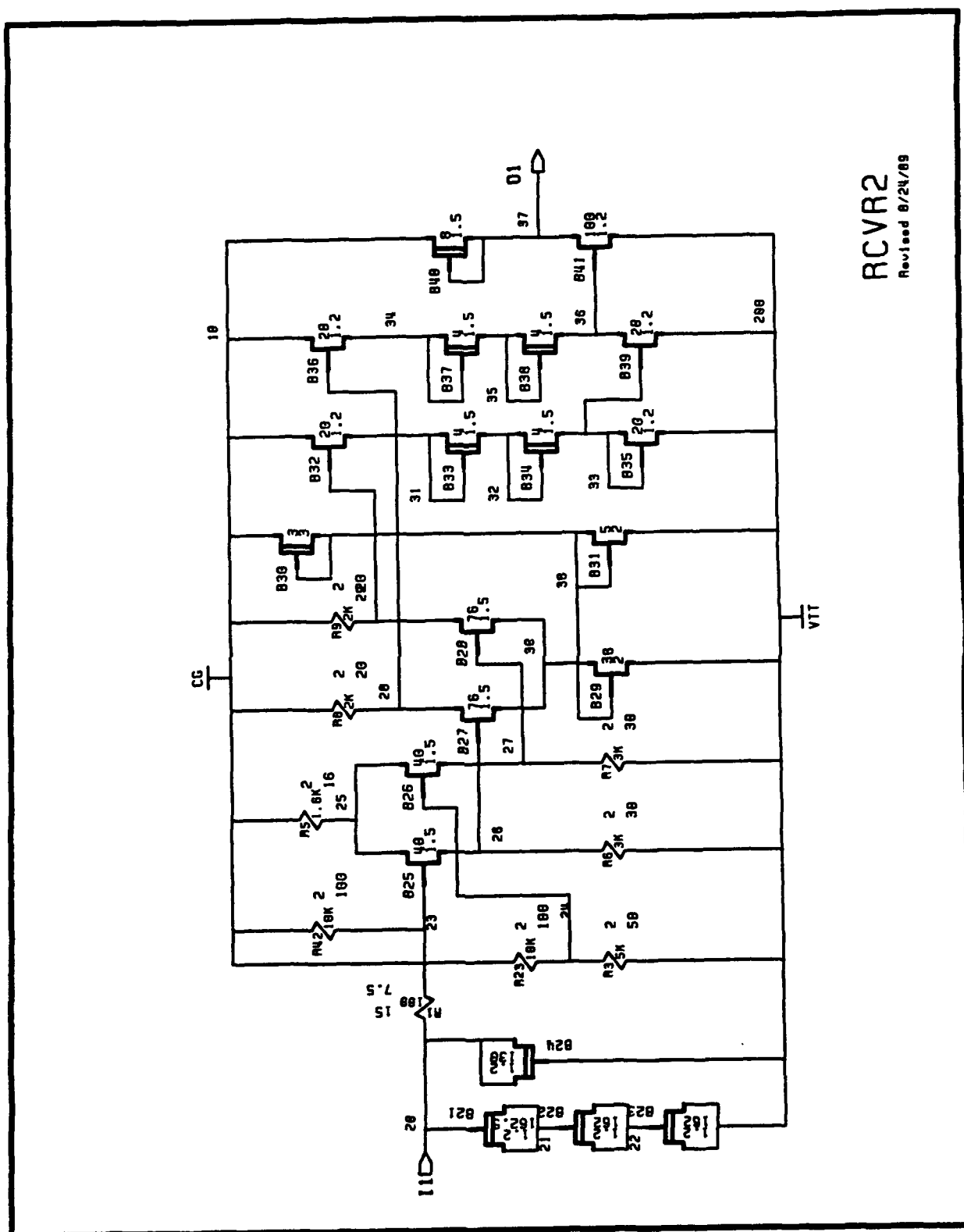
DESCRIPTION:

LOW POWER 2 VOLT RECEIVER WITH PAD

OUT  
0.5  
0.3  
1.4  
1.4  
1  
0  
SSS  
01

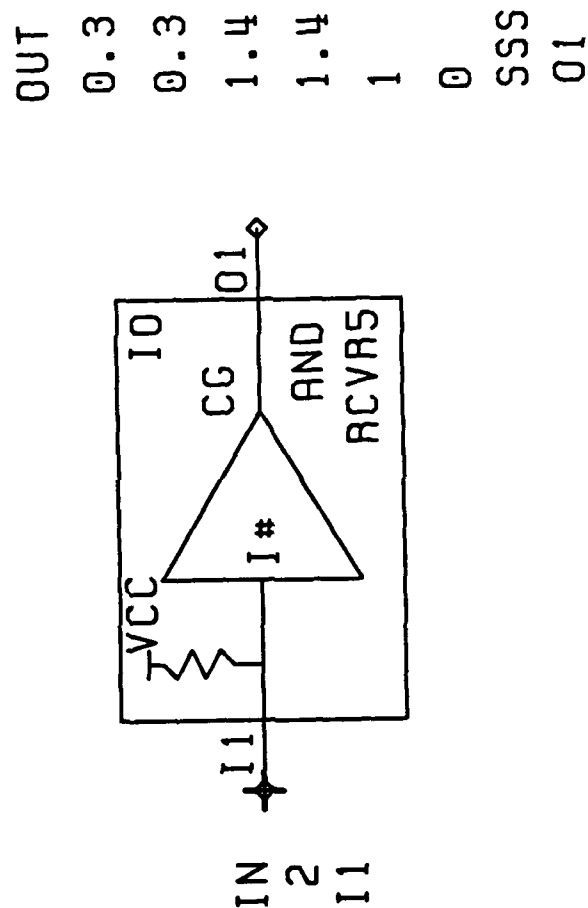


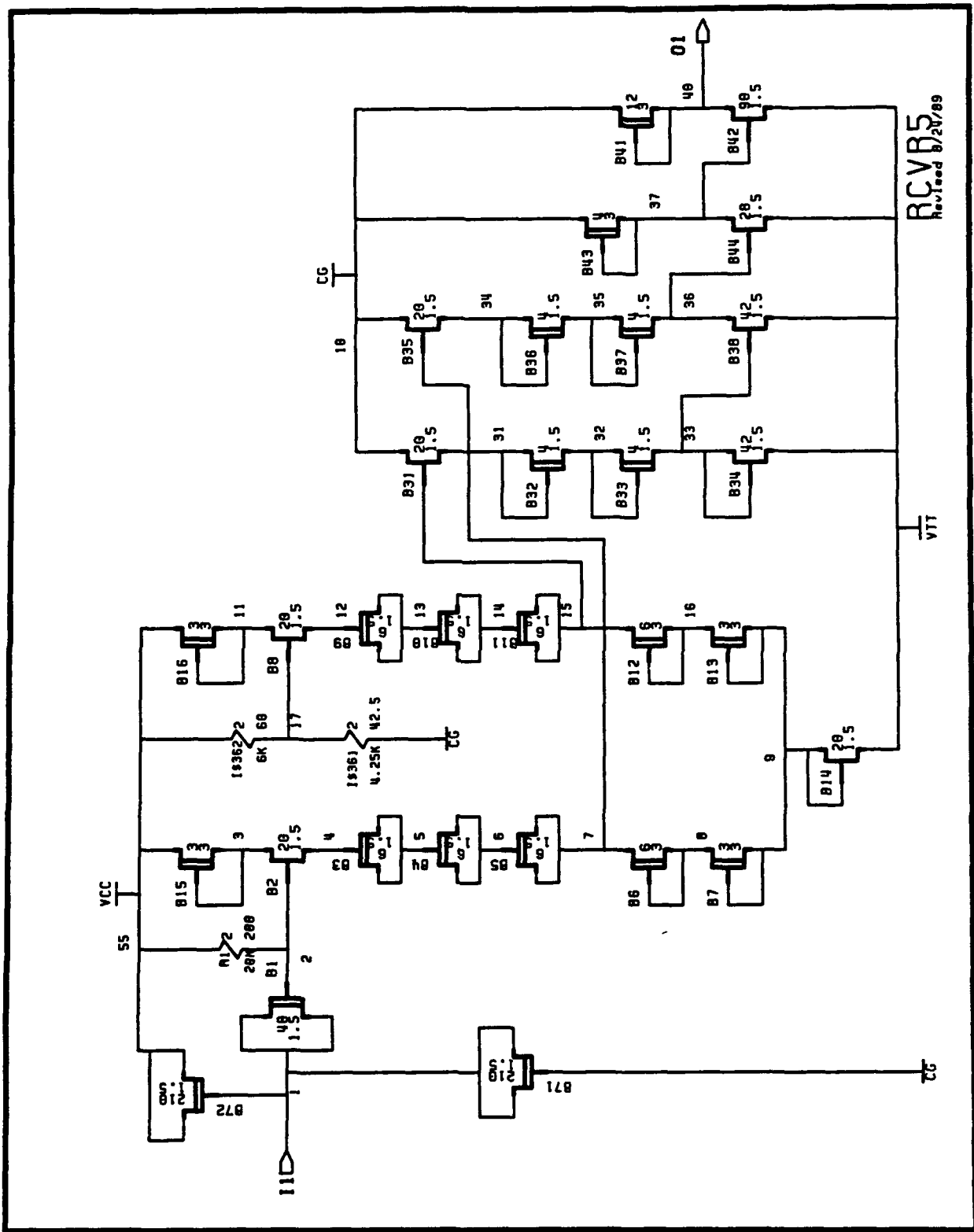


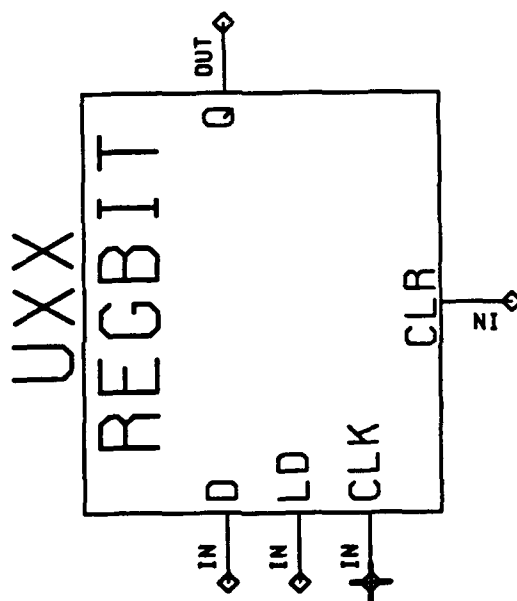


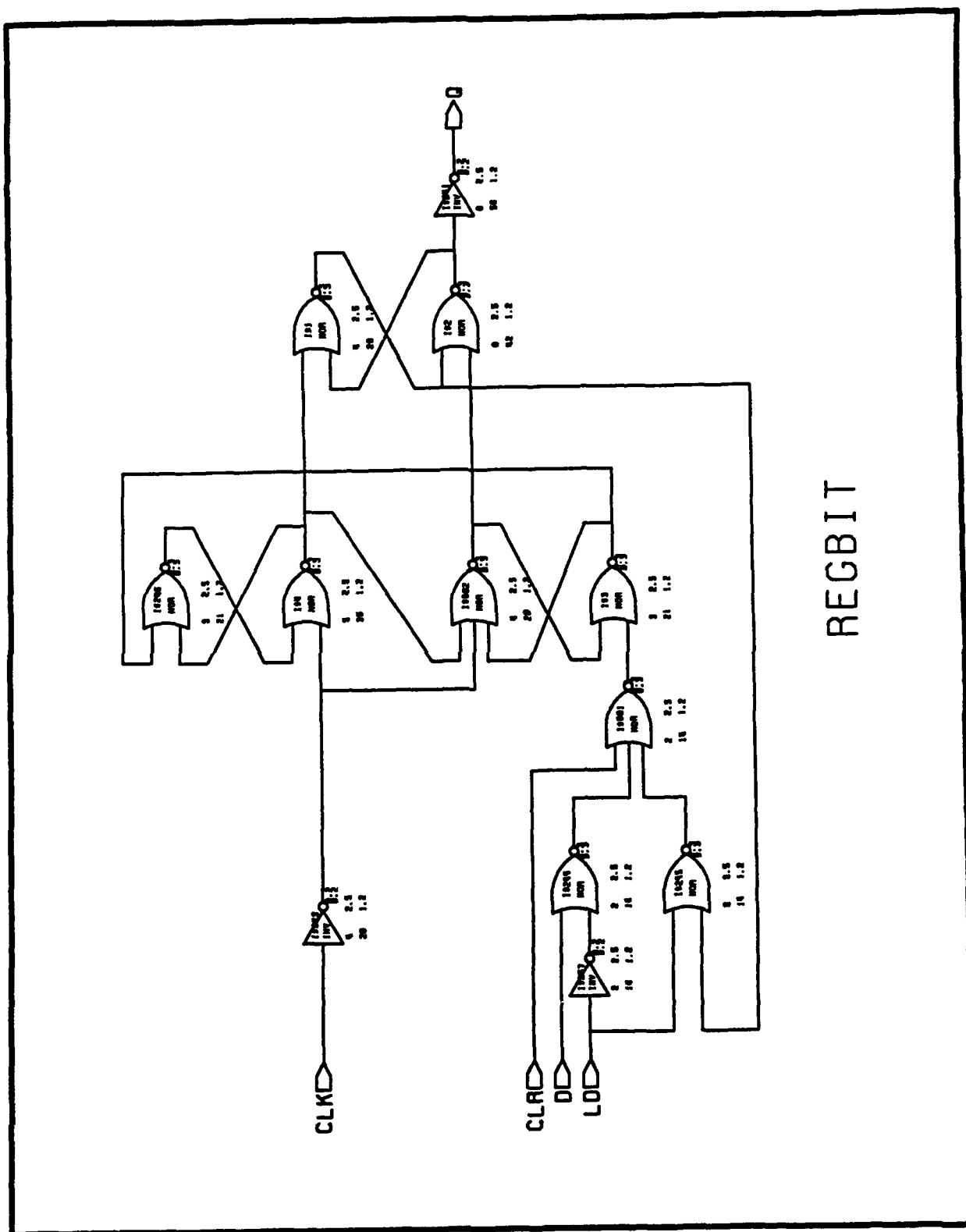
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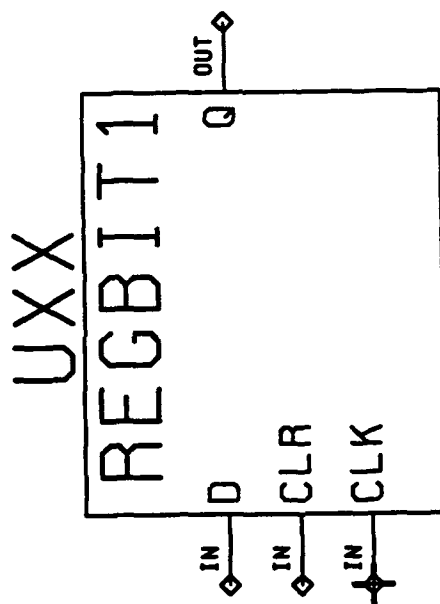
NAME: RCVR5  
DESCRIPTION: NON-INVERTING TTL RECEIVER WITH PAD

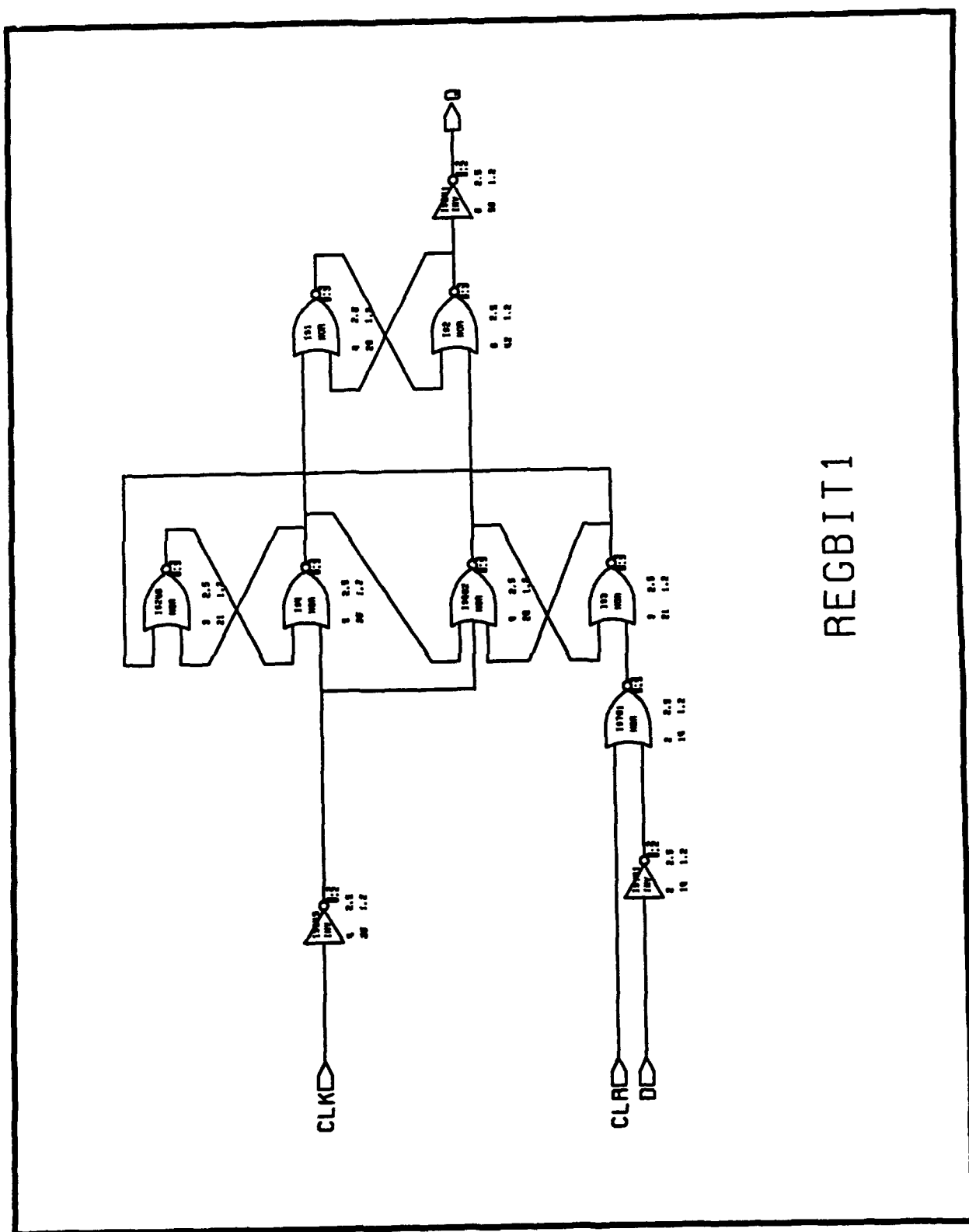


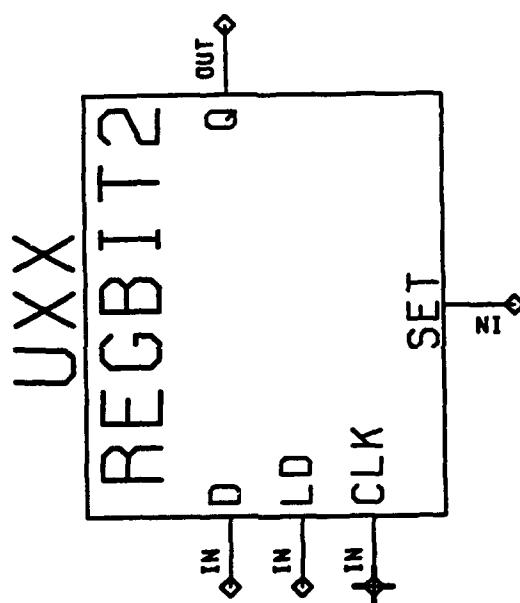




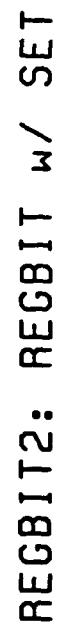


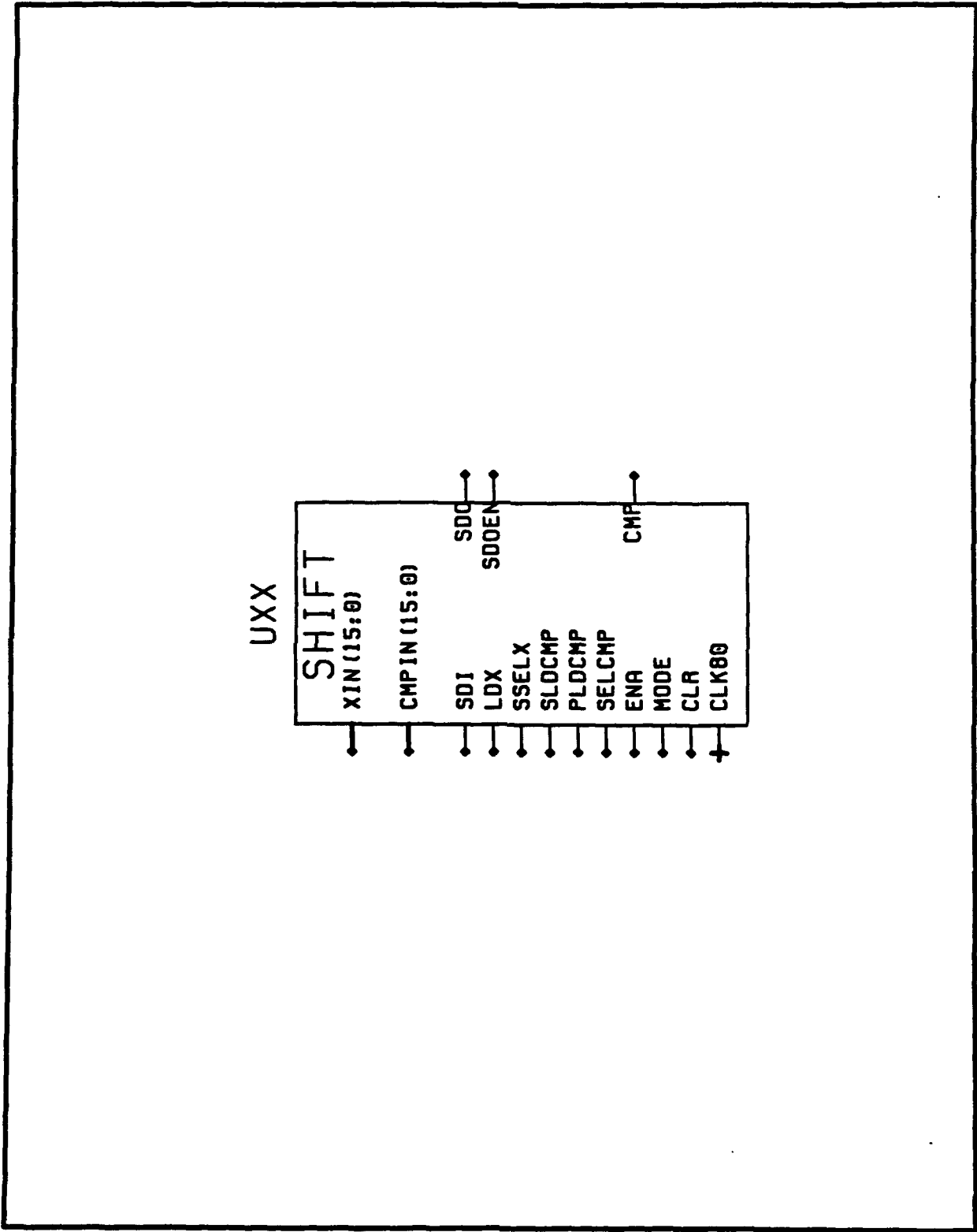


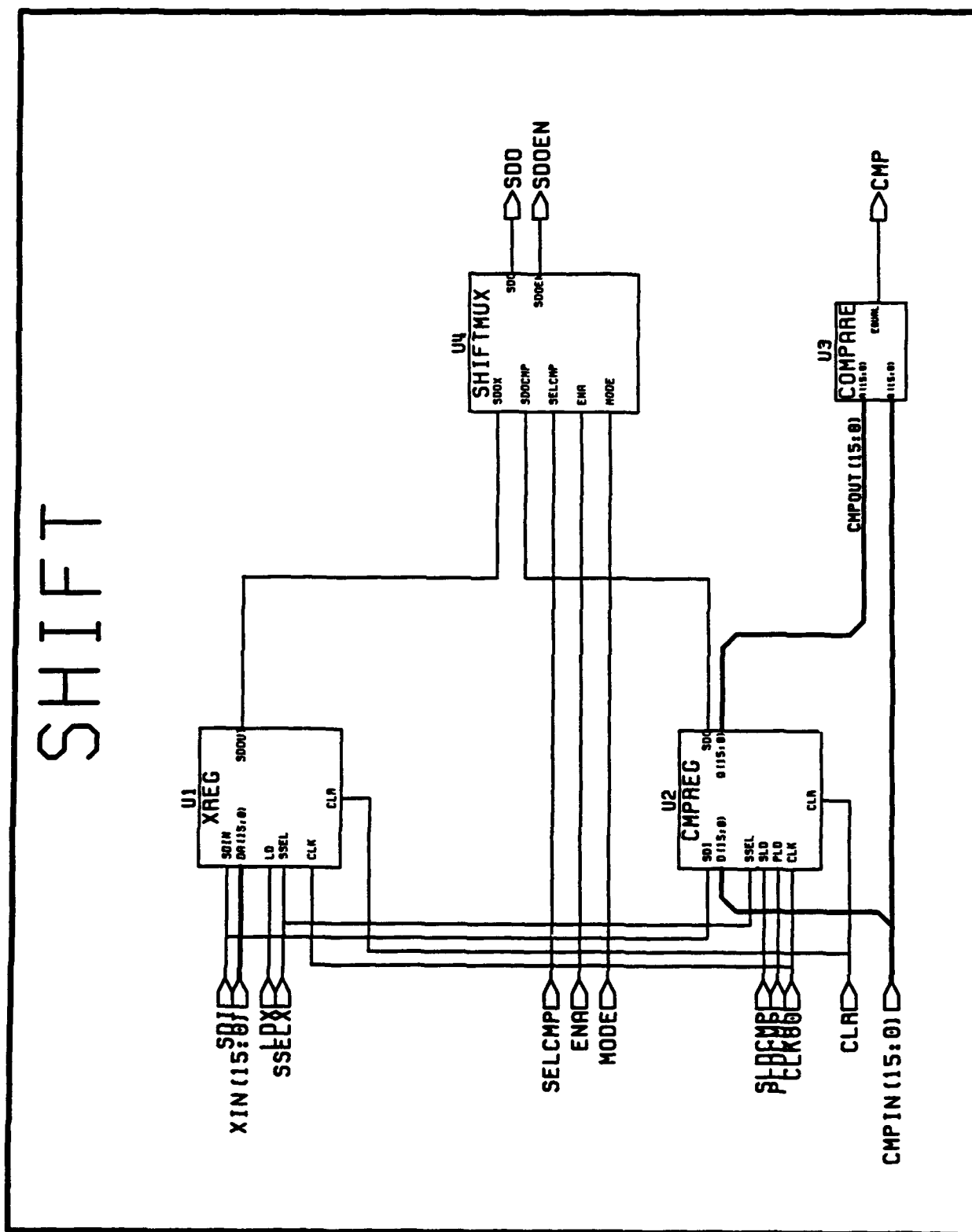


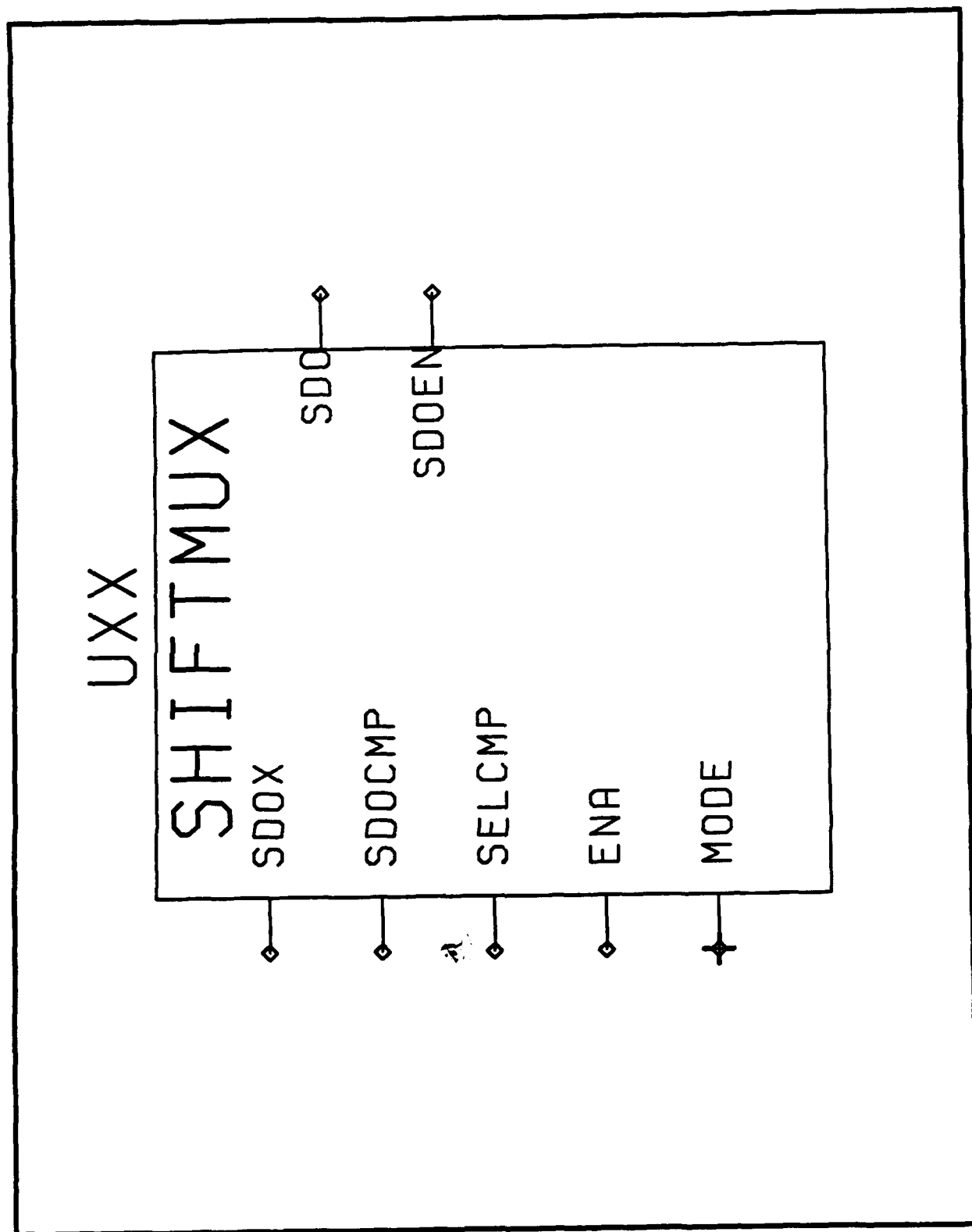


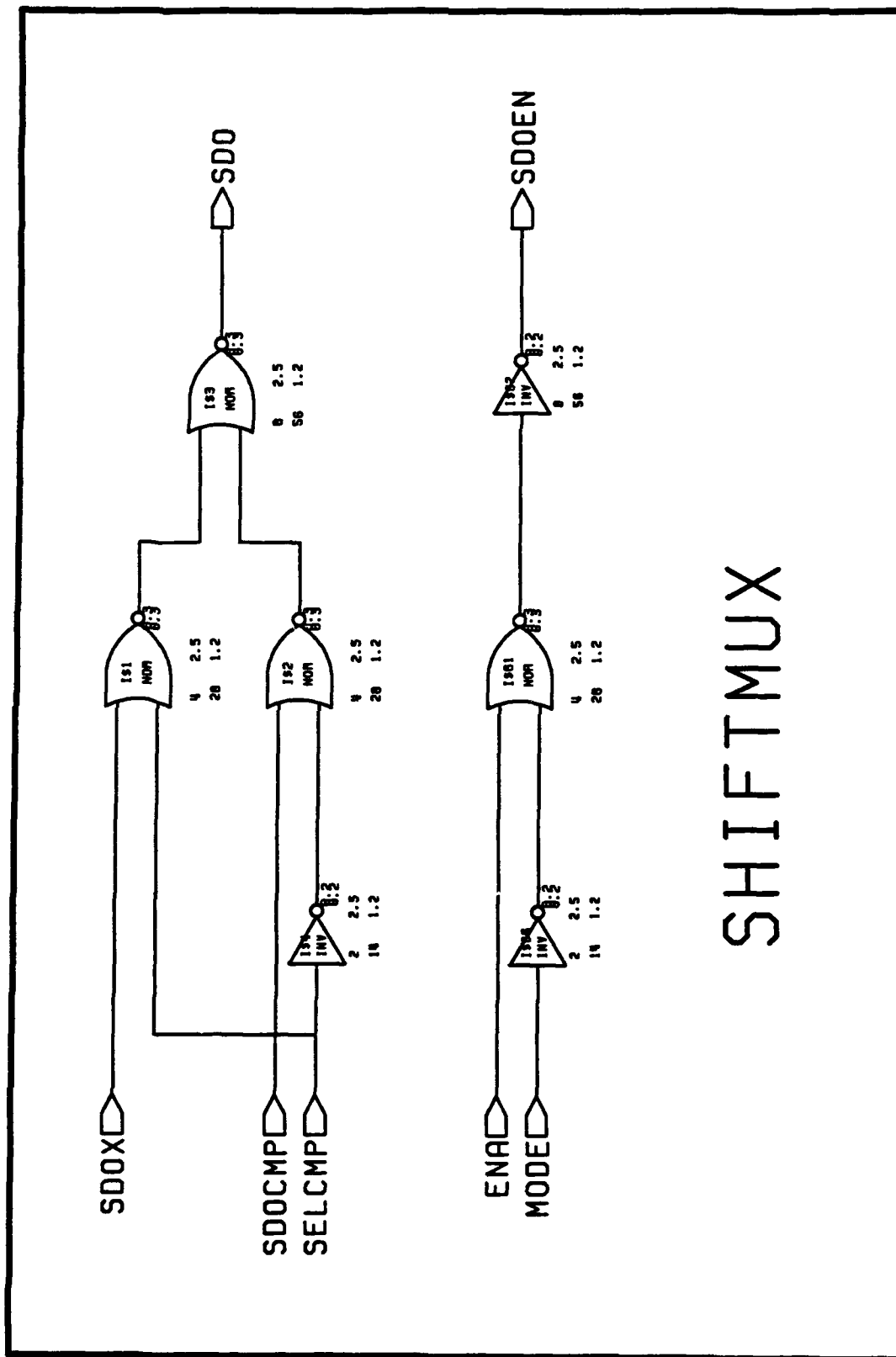


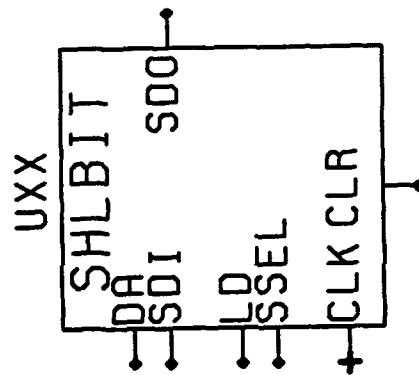


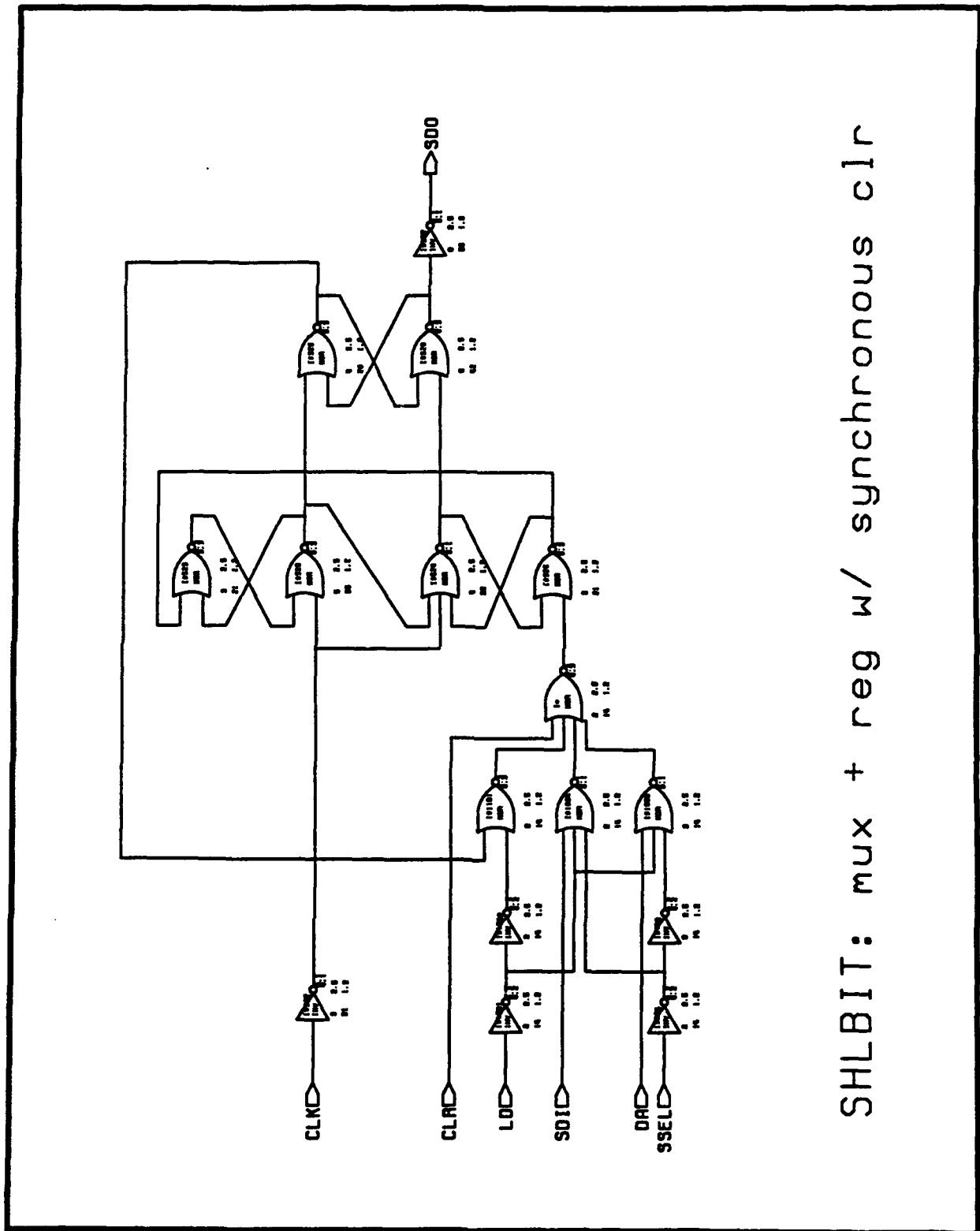




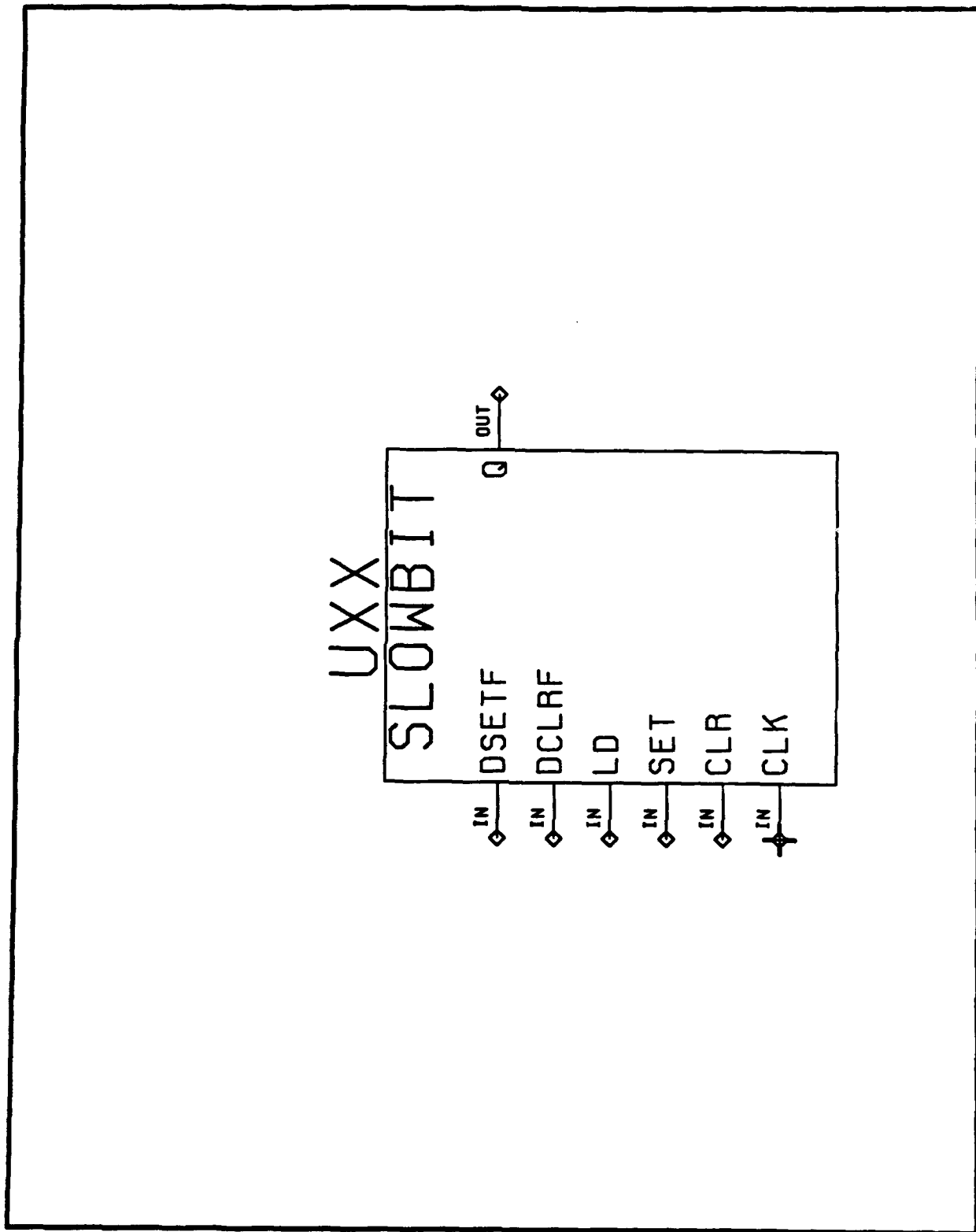




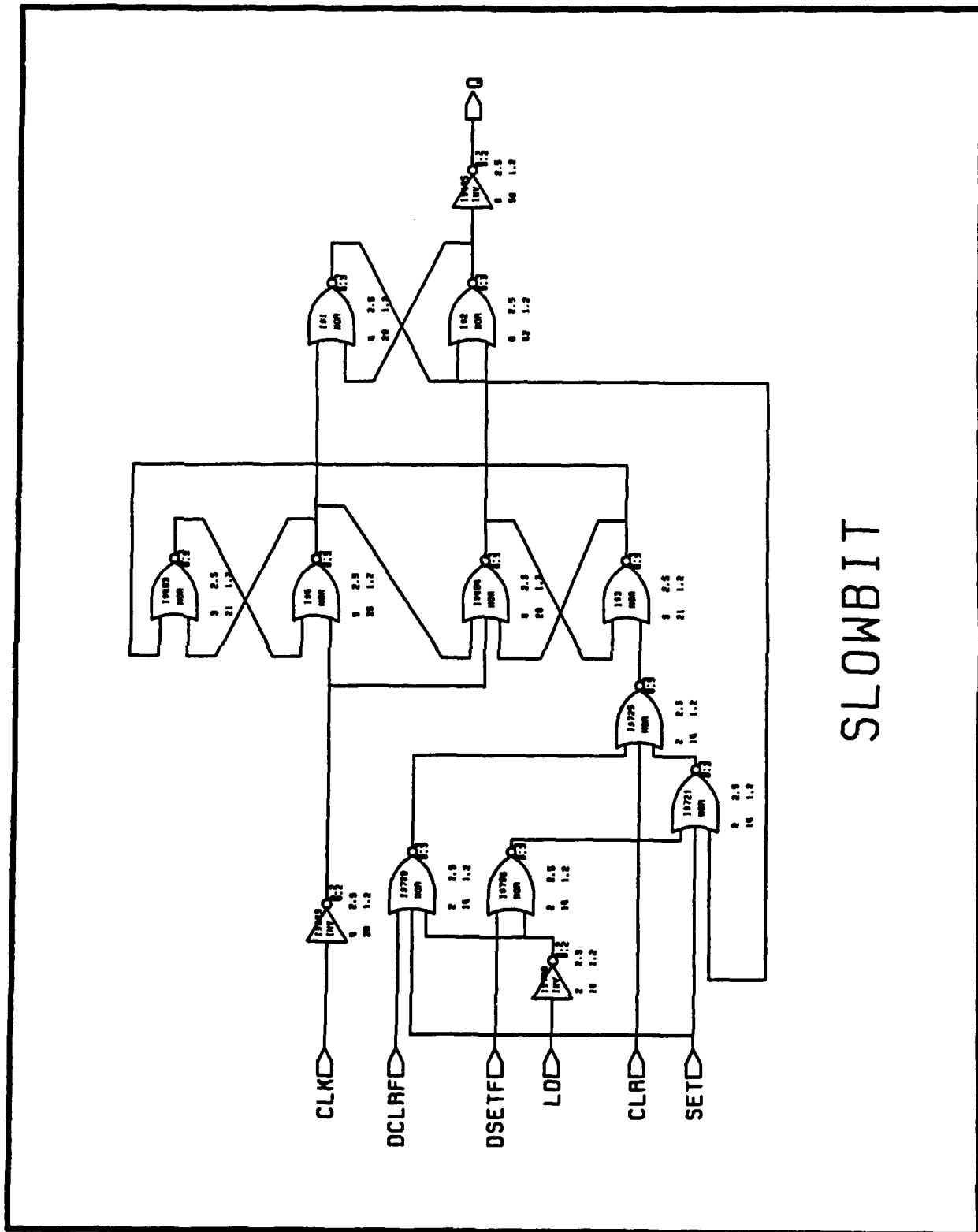


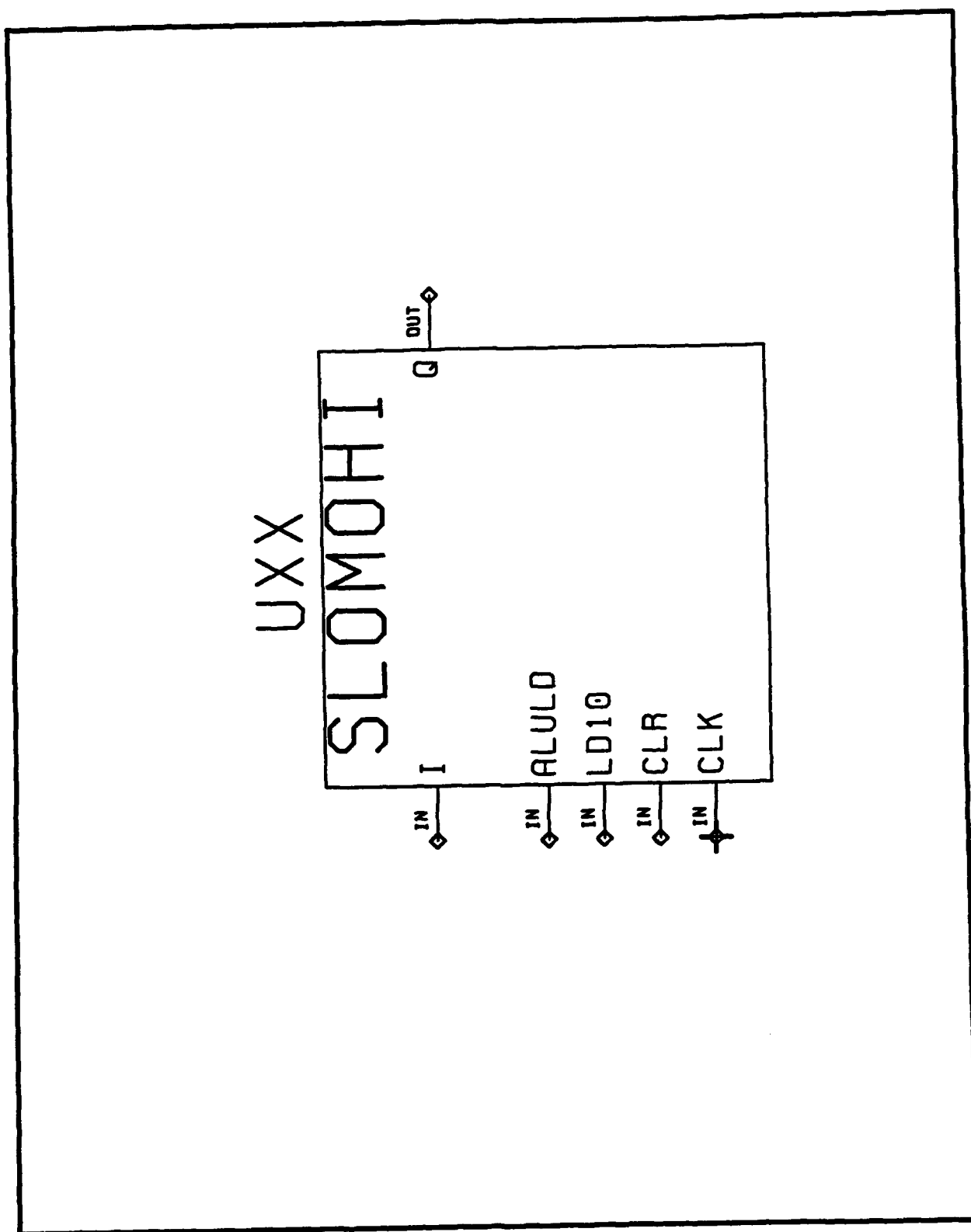


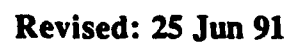
SHLBIT: mux + reg + reg w/ synchronous clr

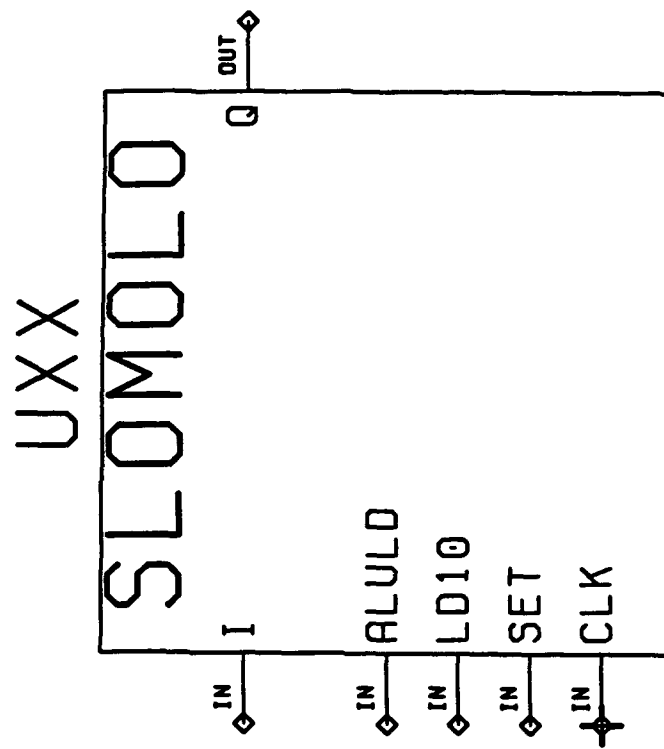


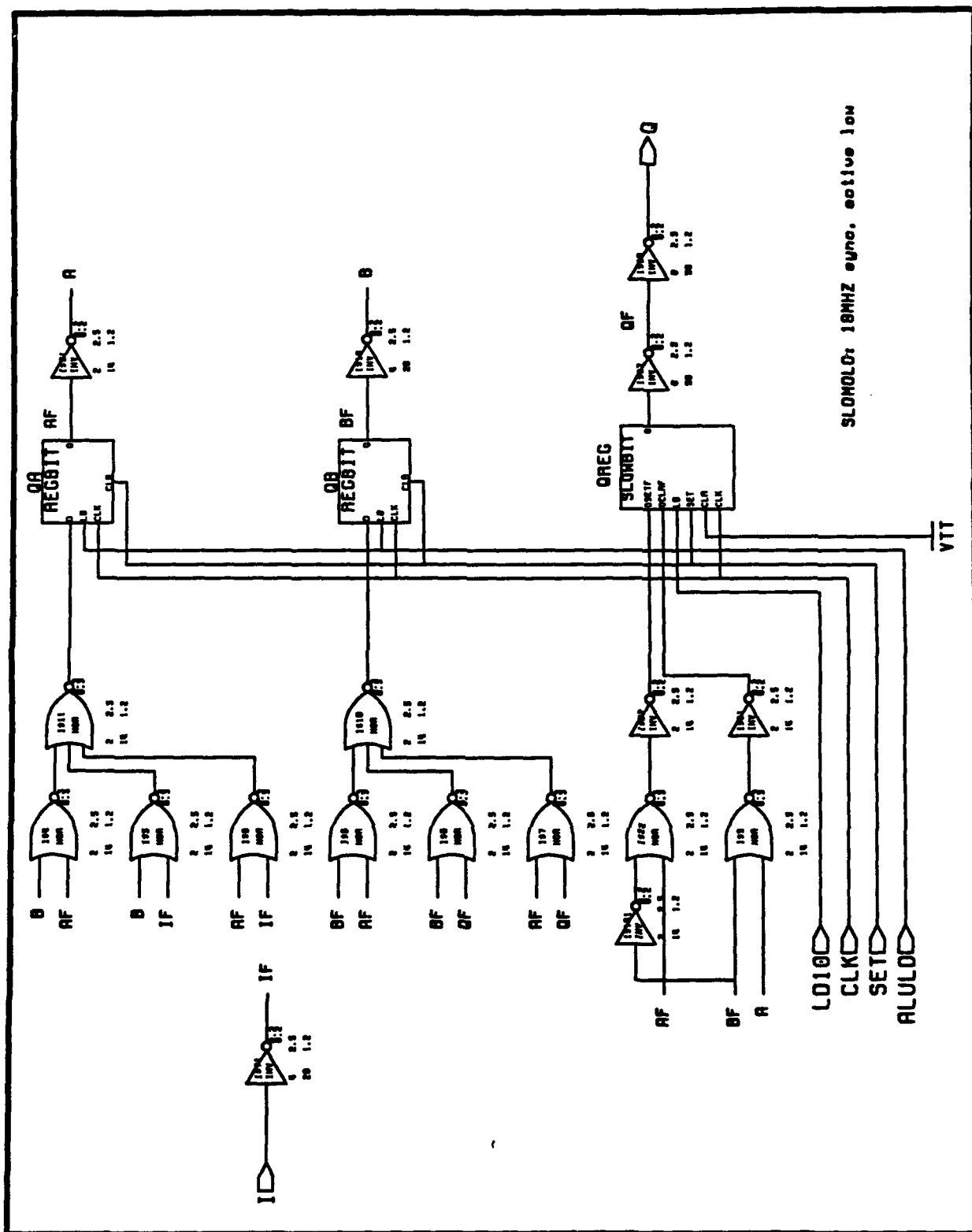




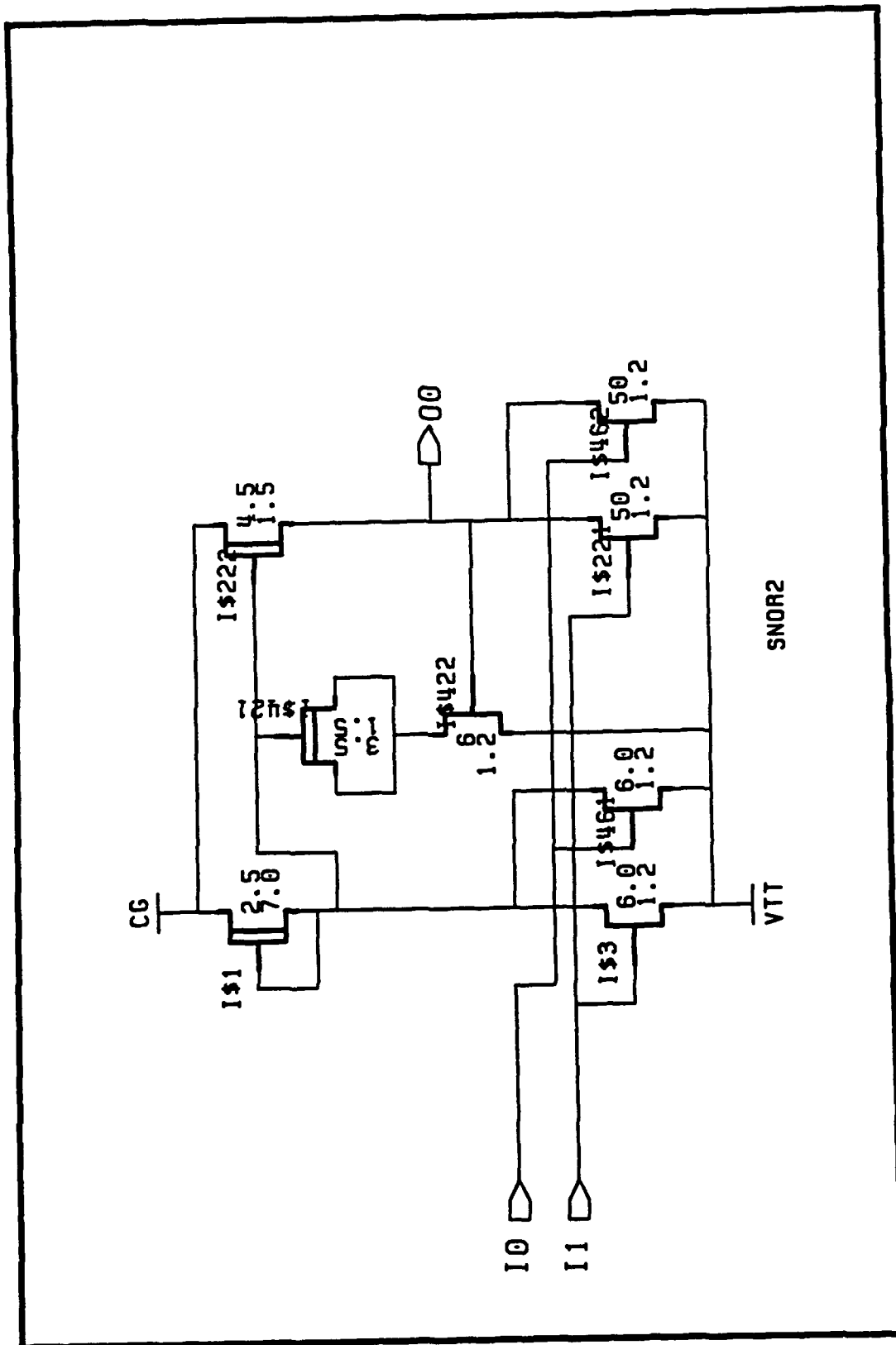


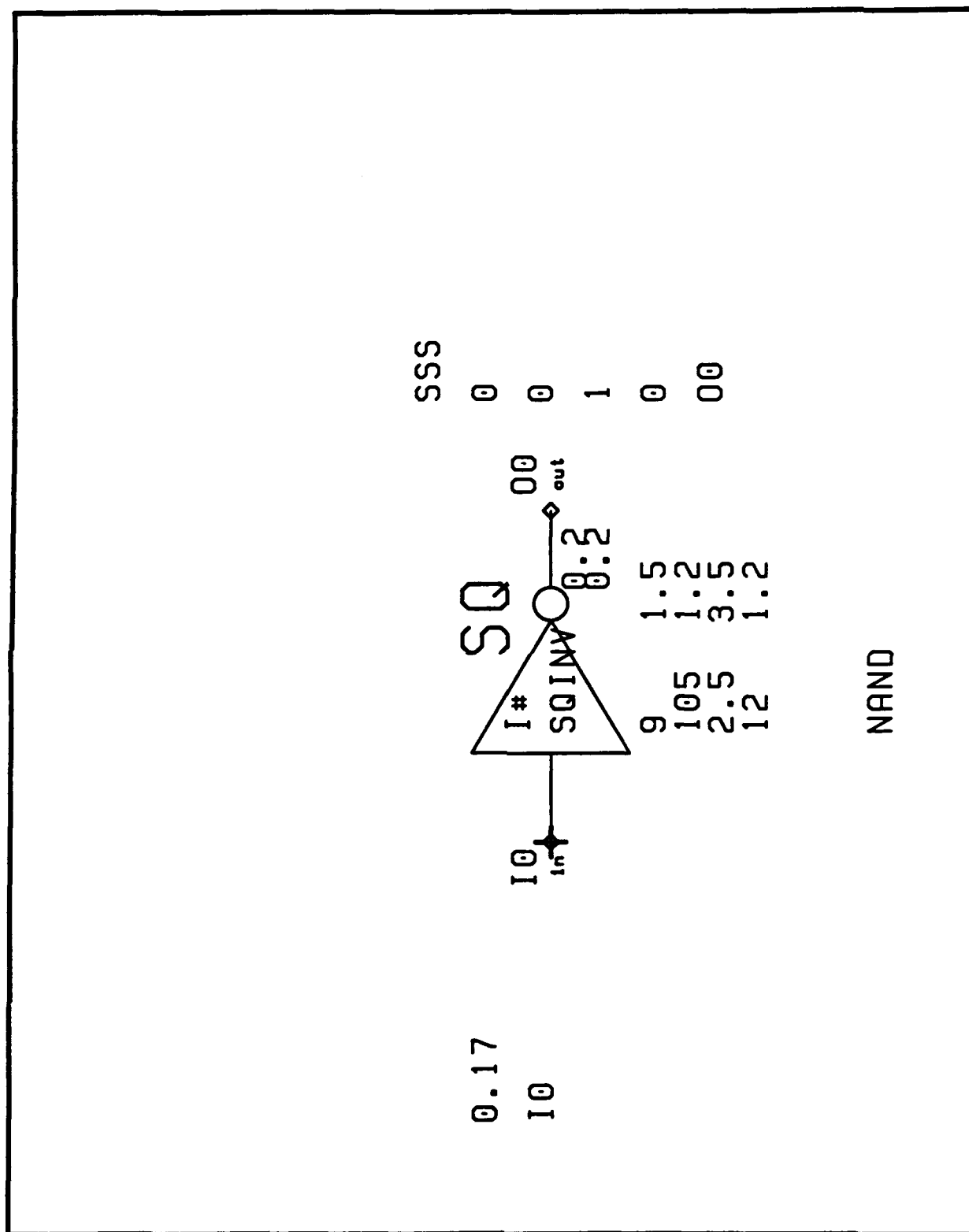




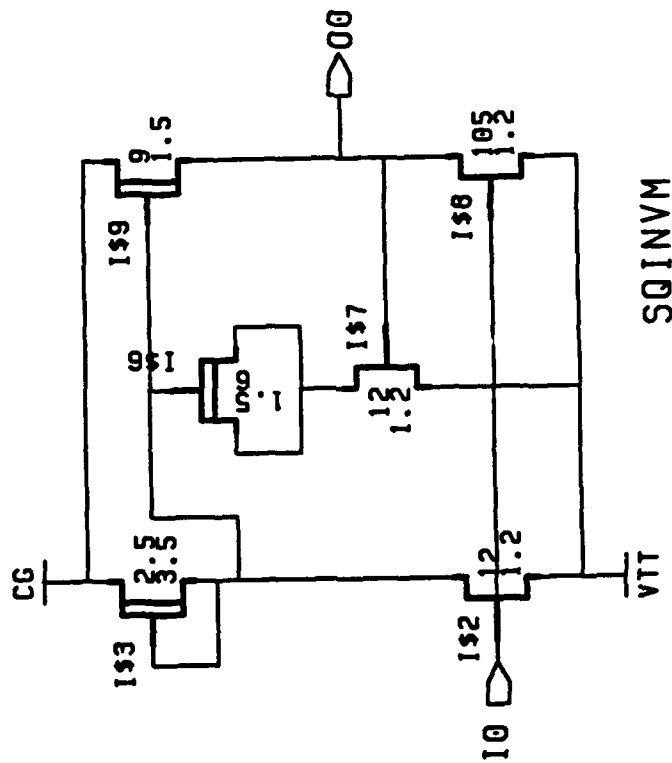


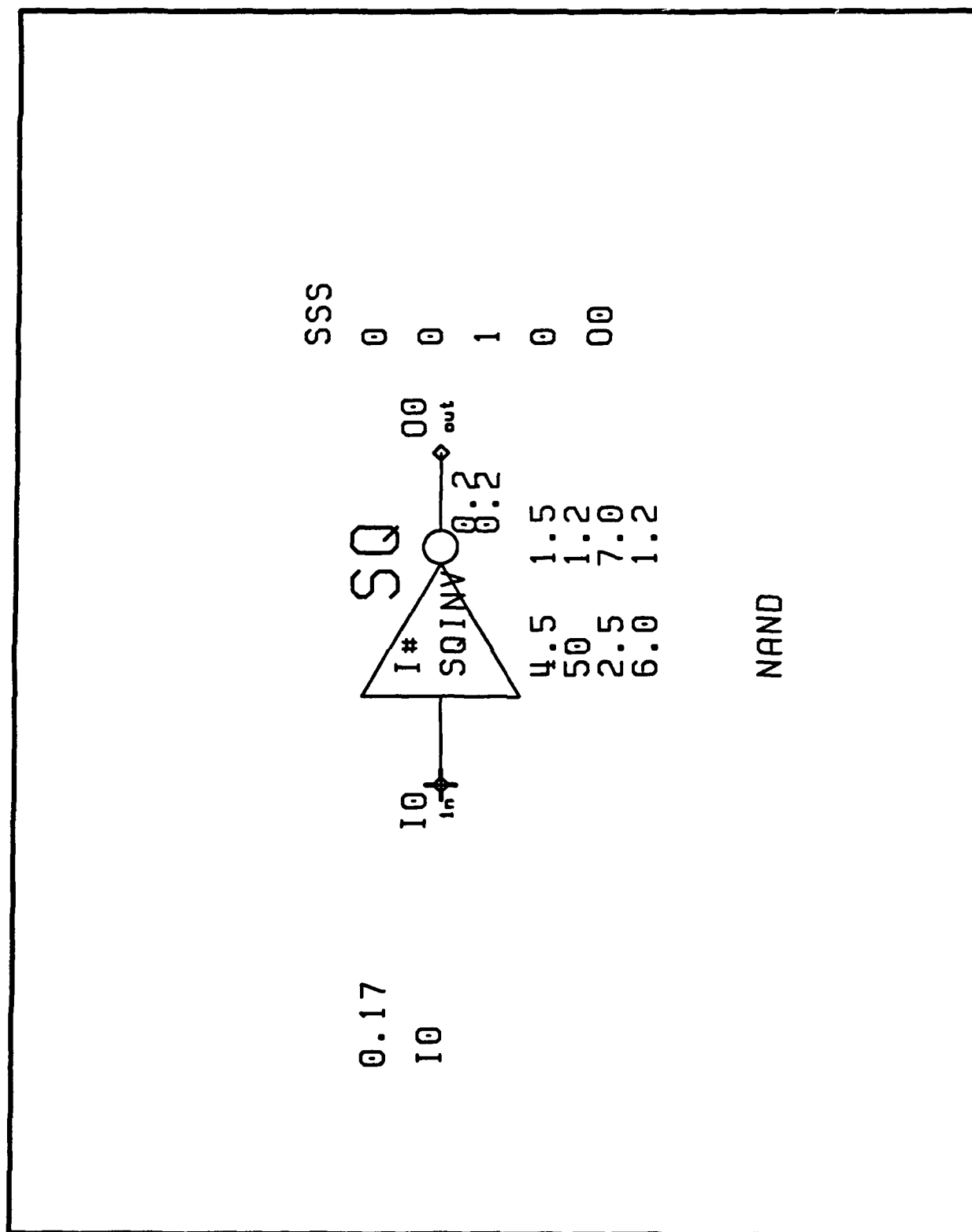


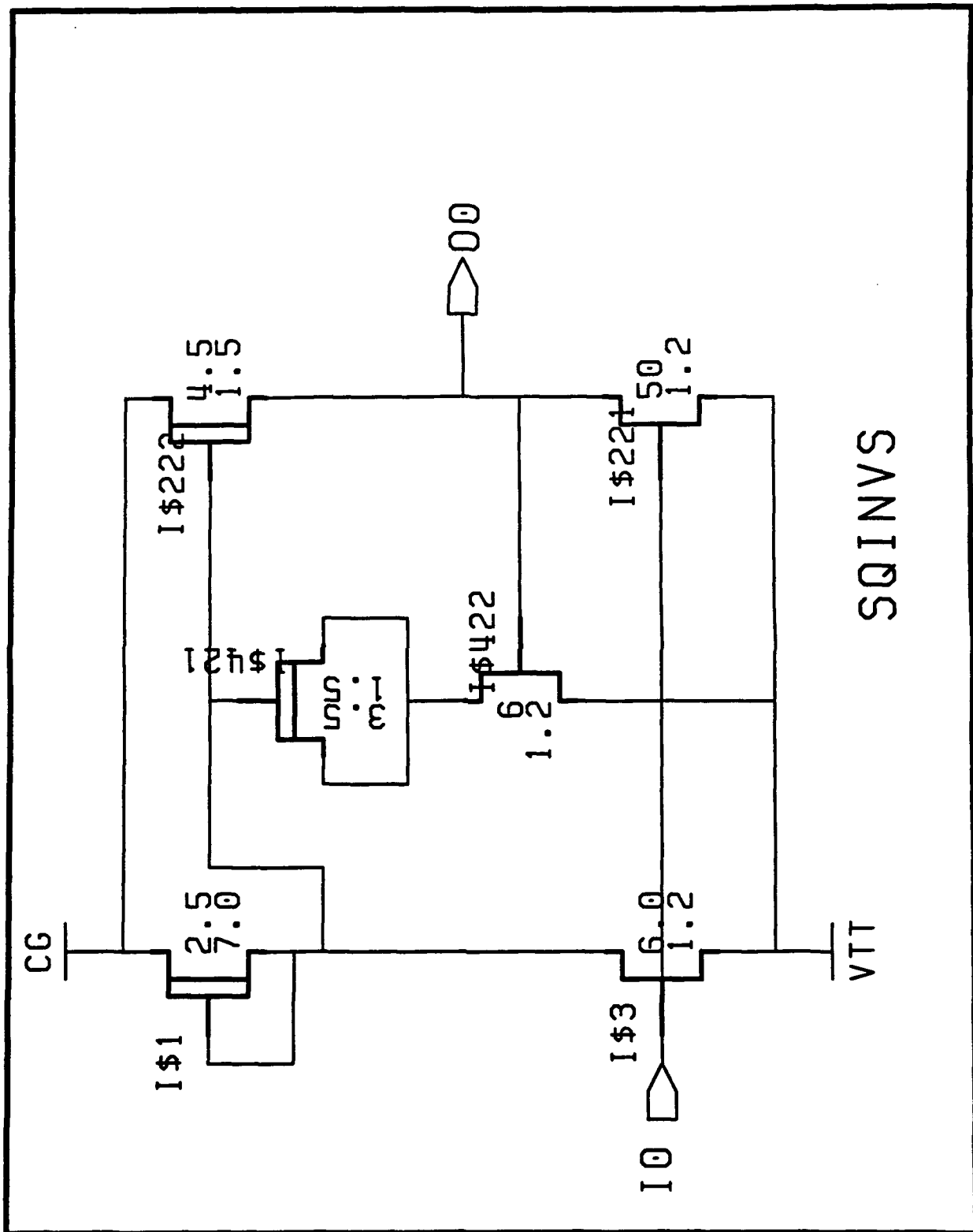


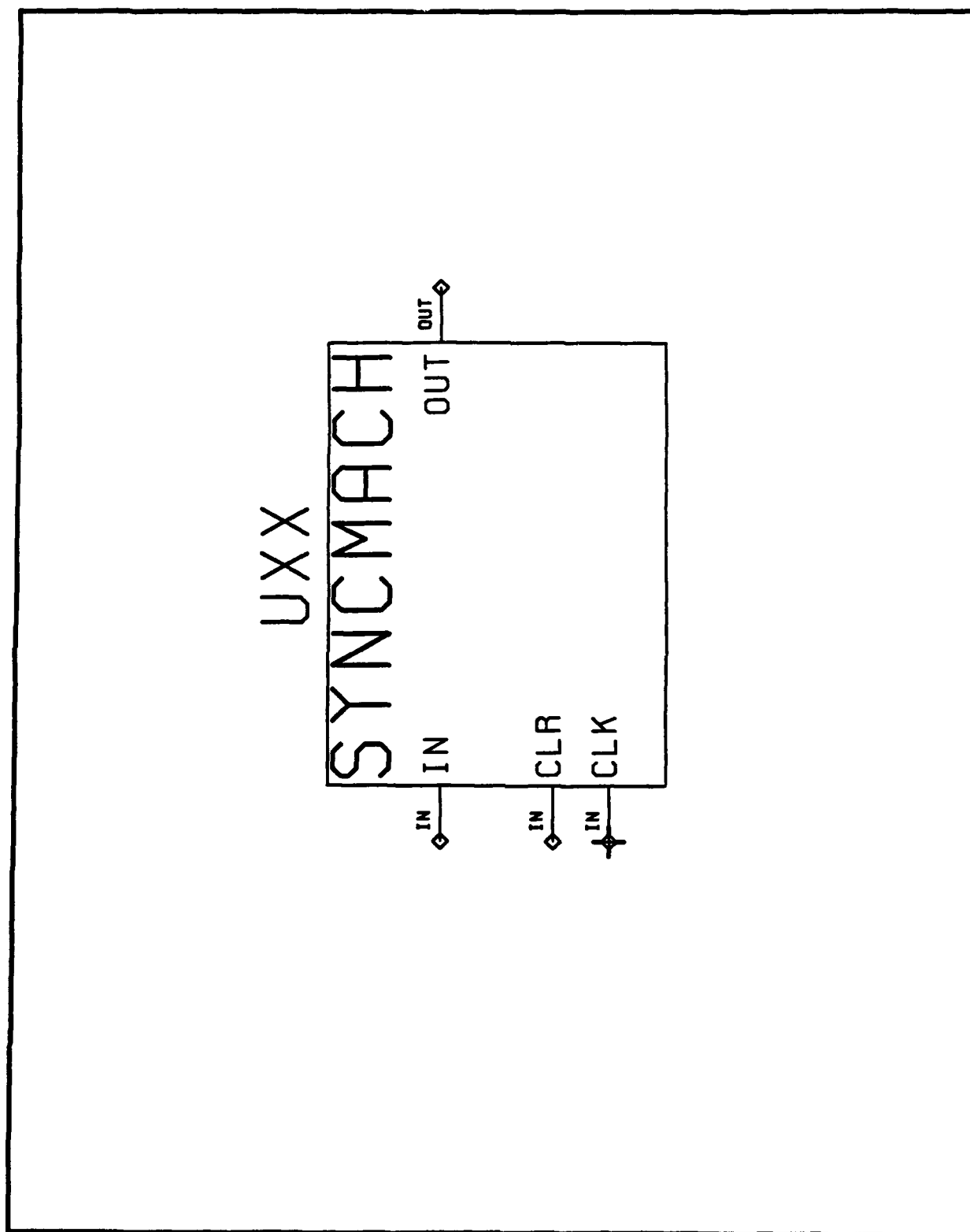


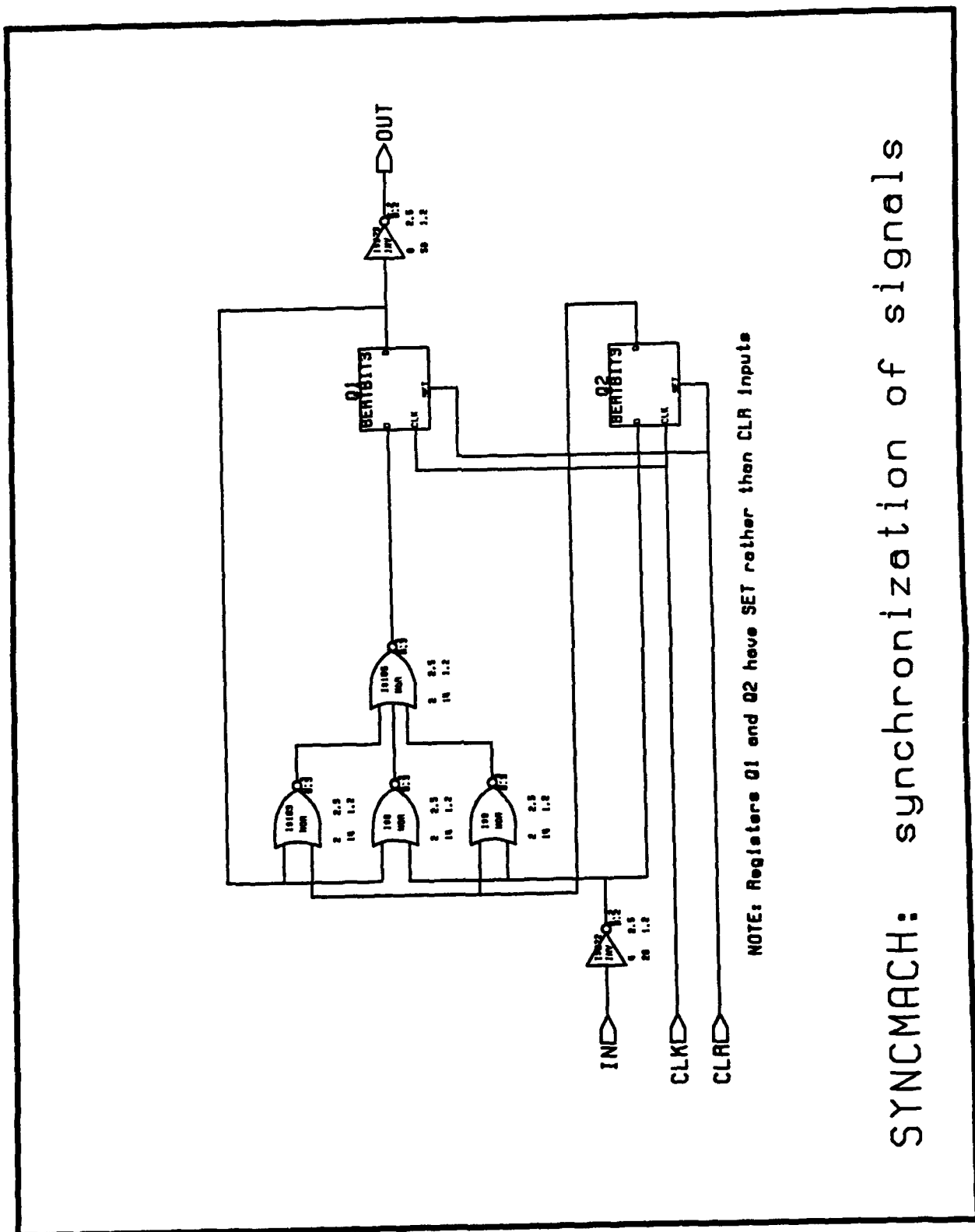


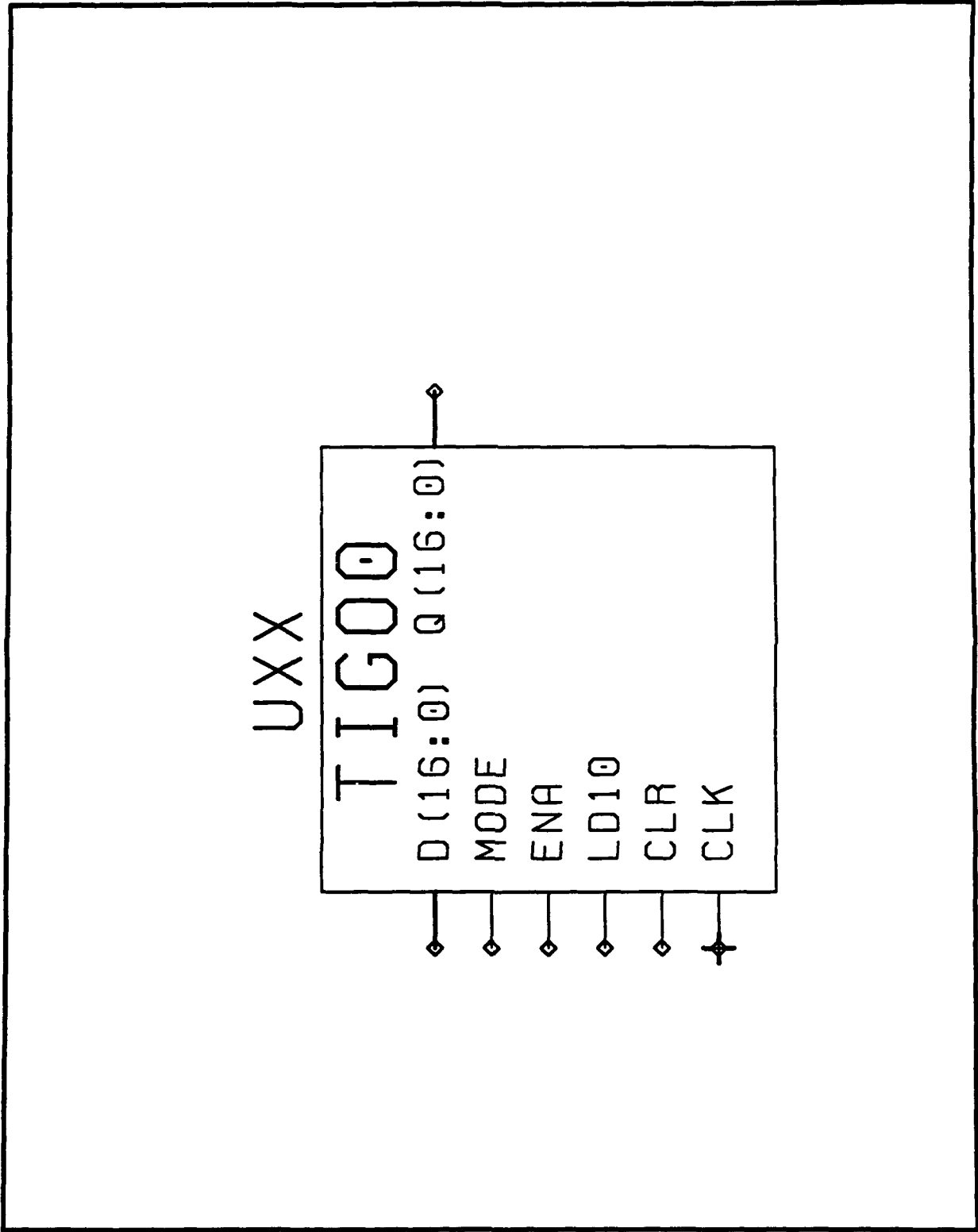


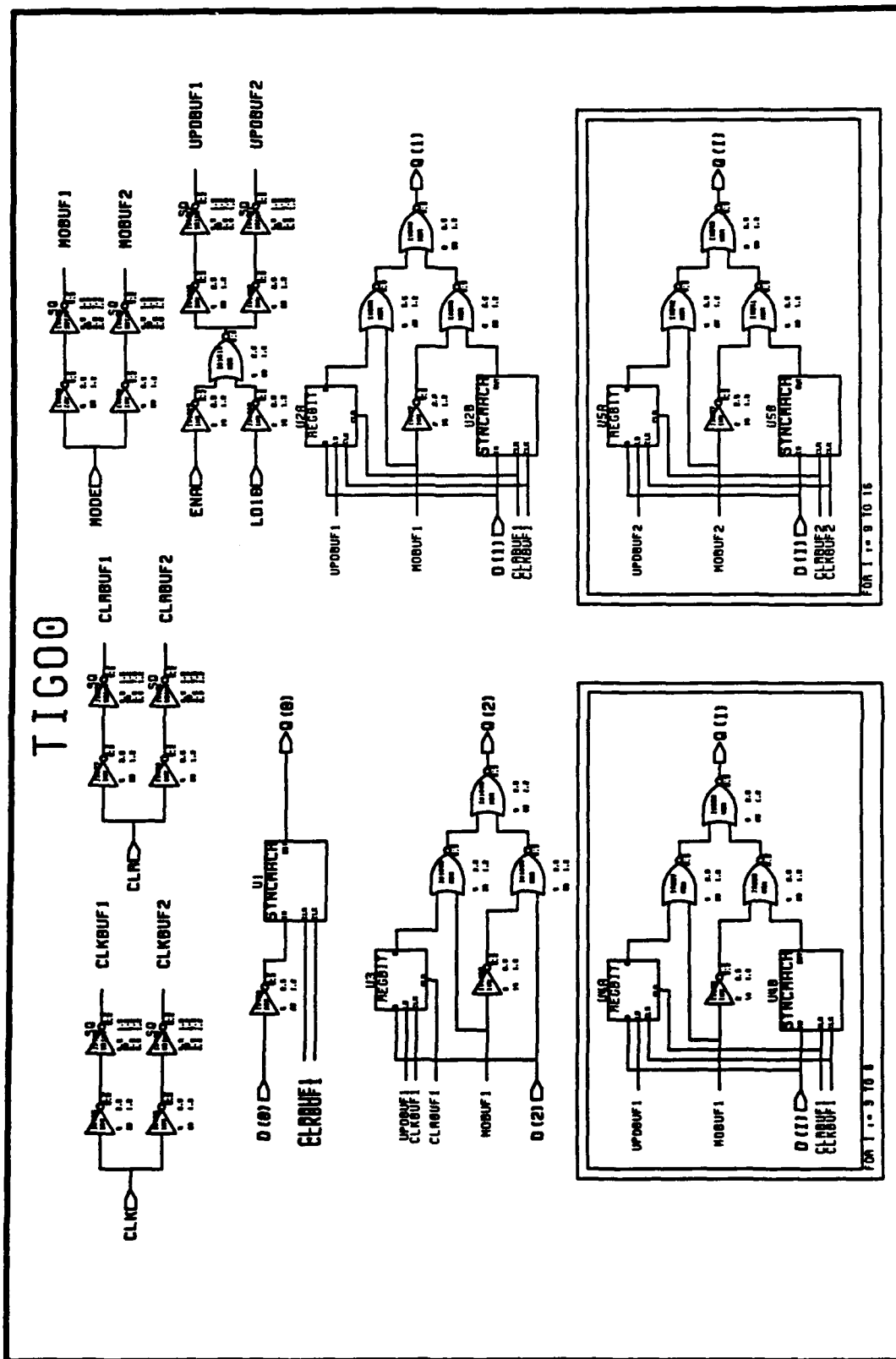


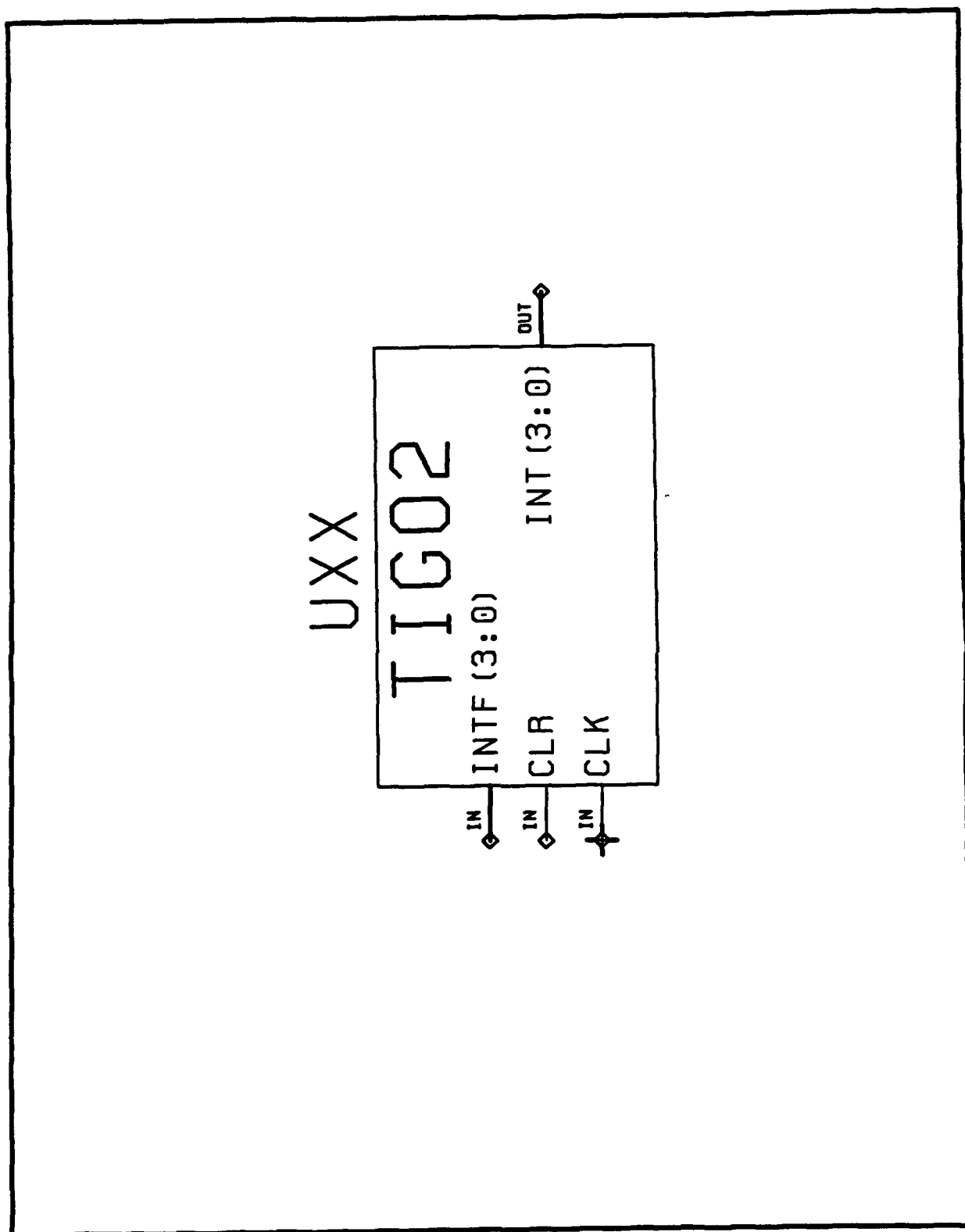




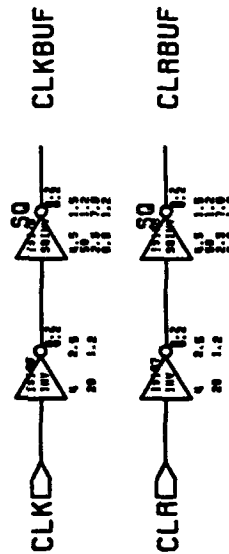
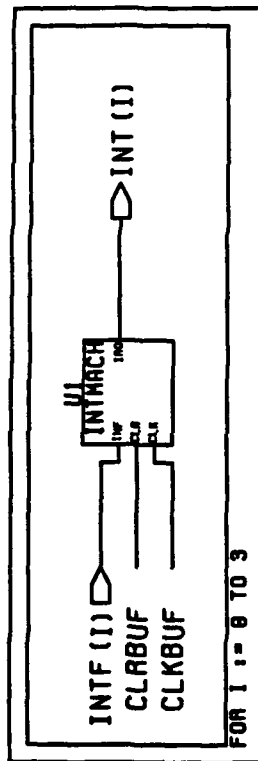




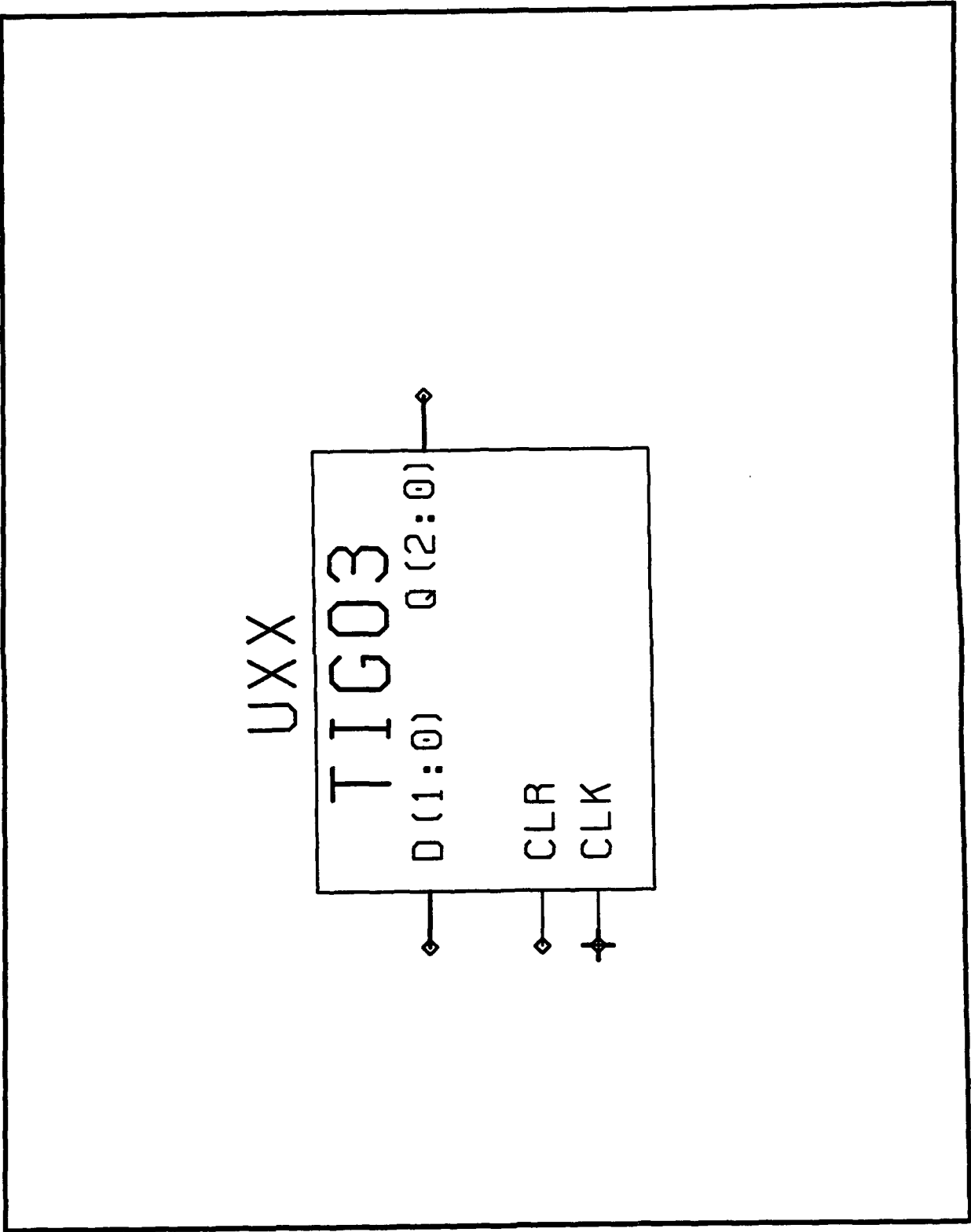


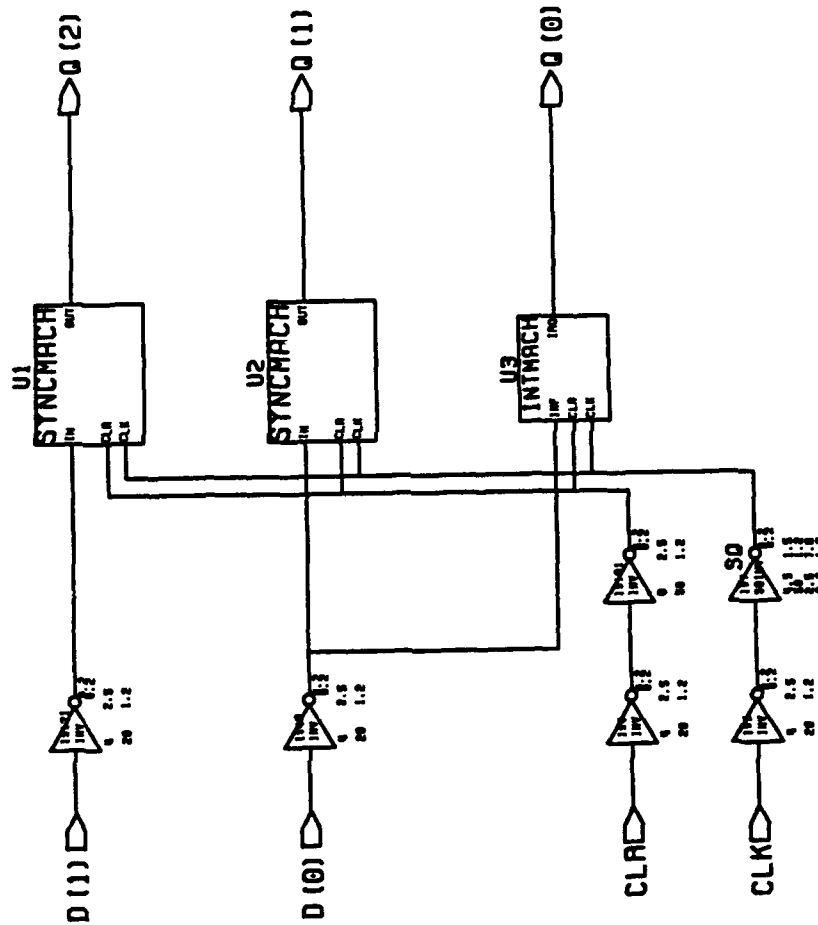




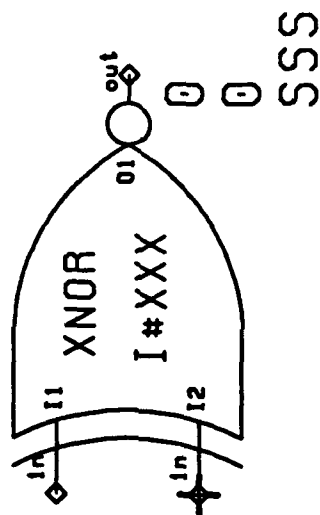


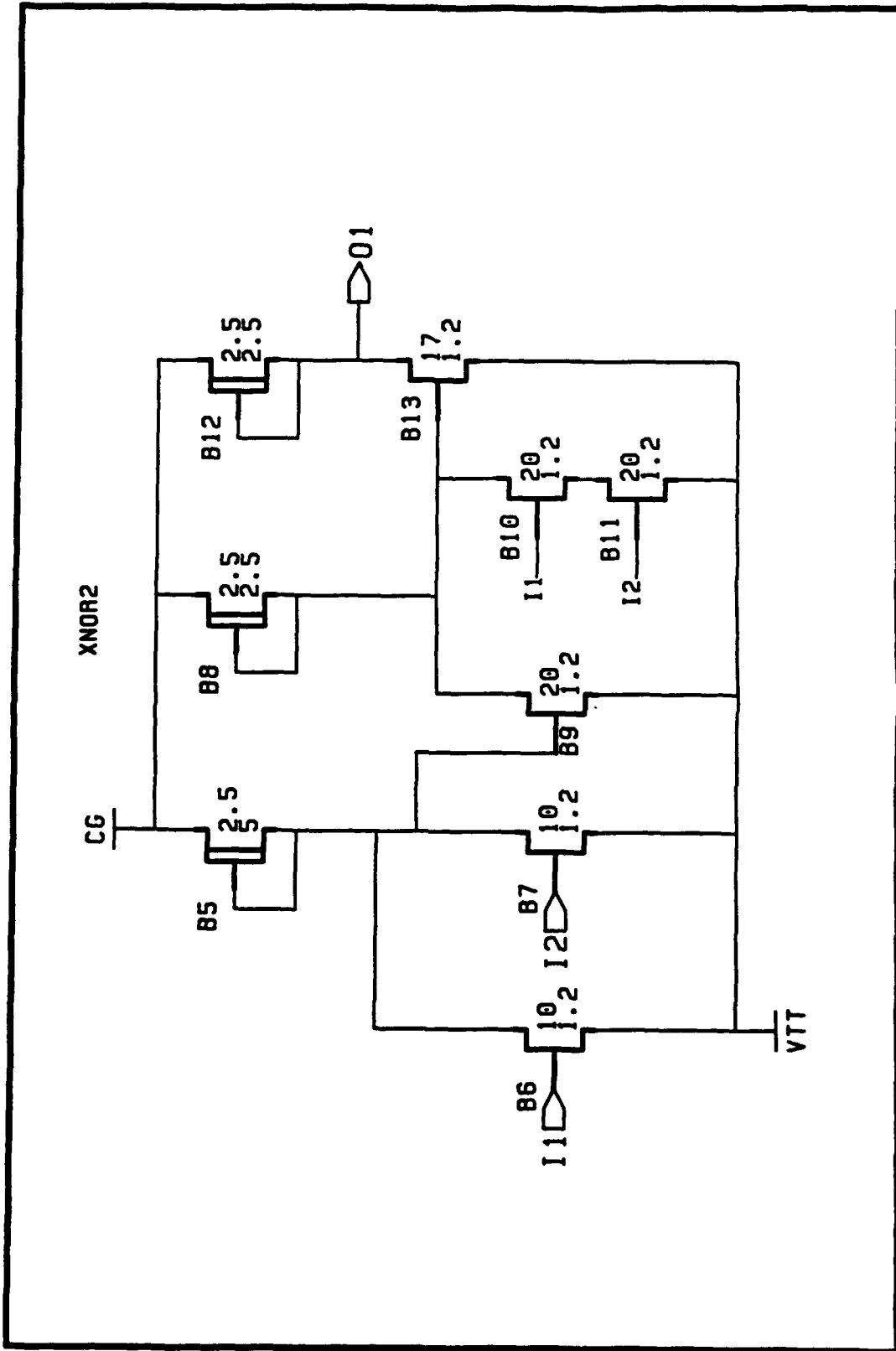
TIG02: Interrupt pulse generation

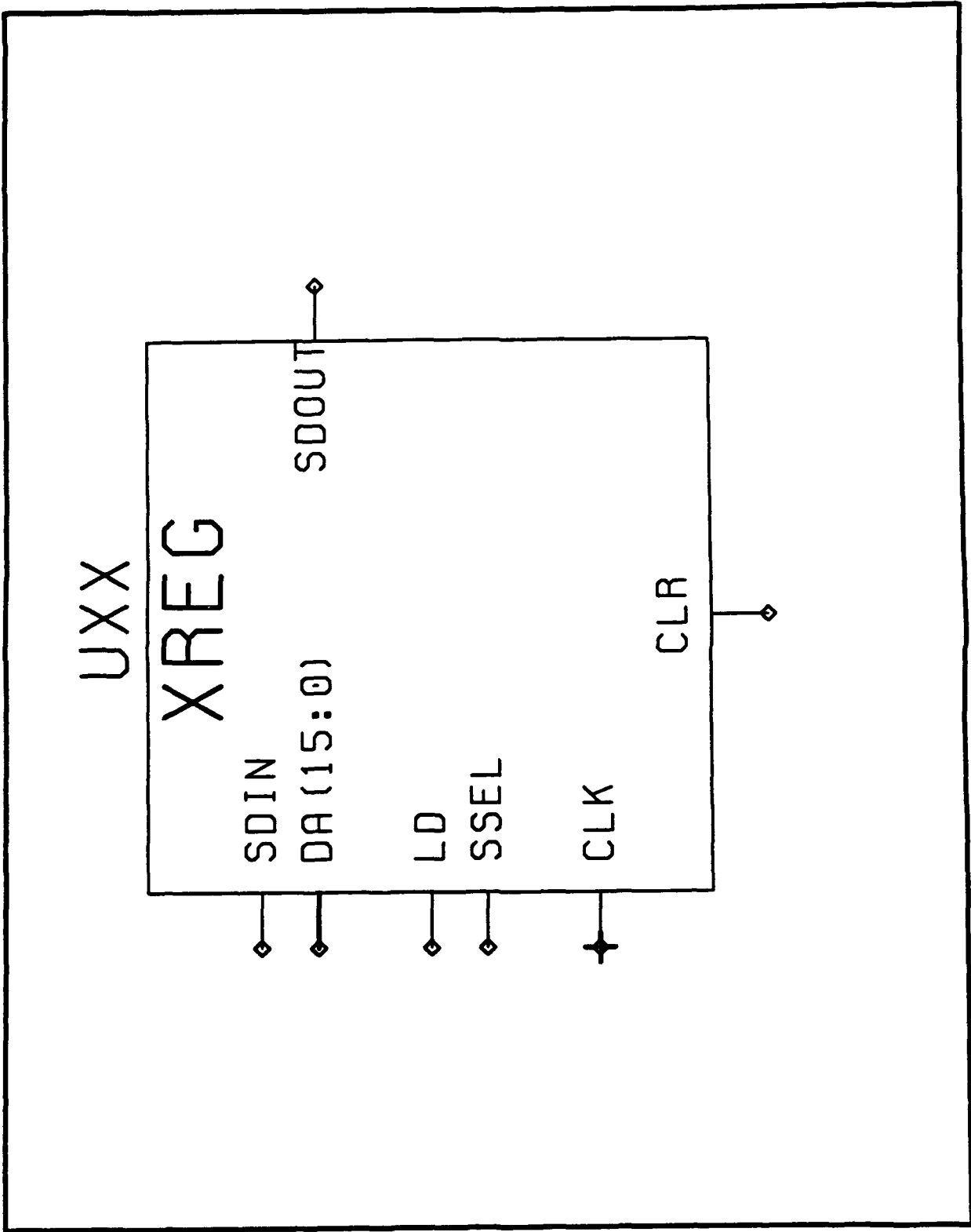


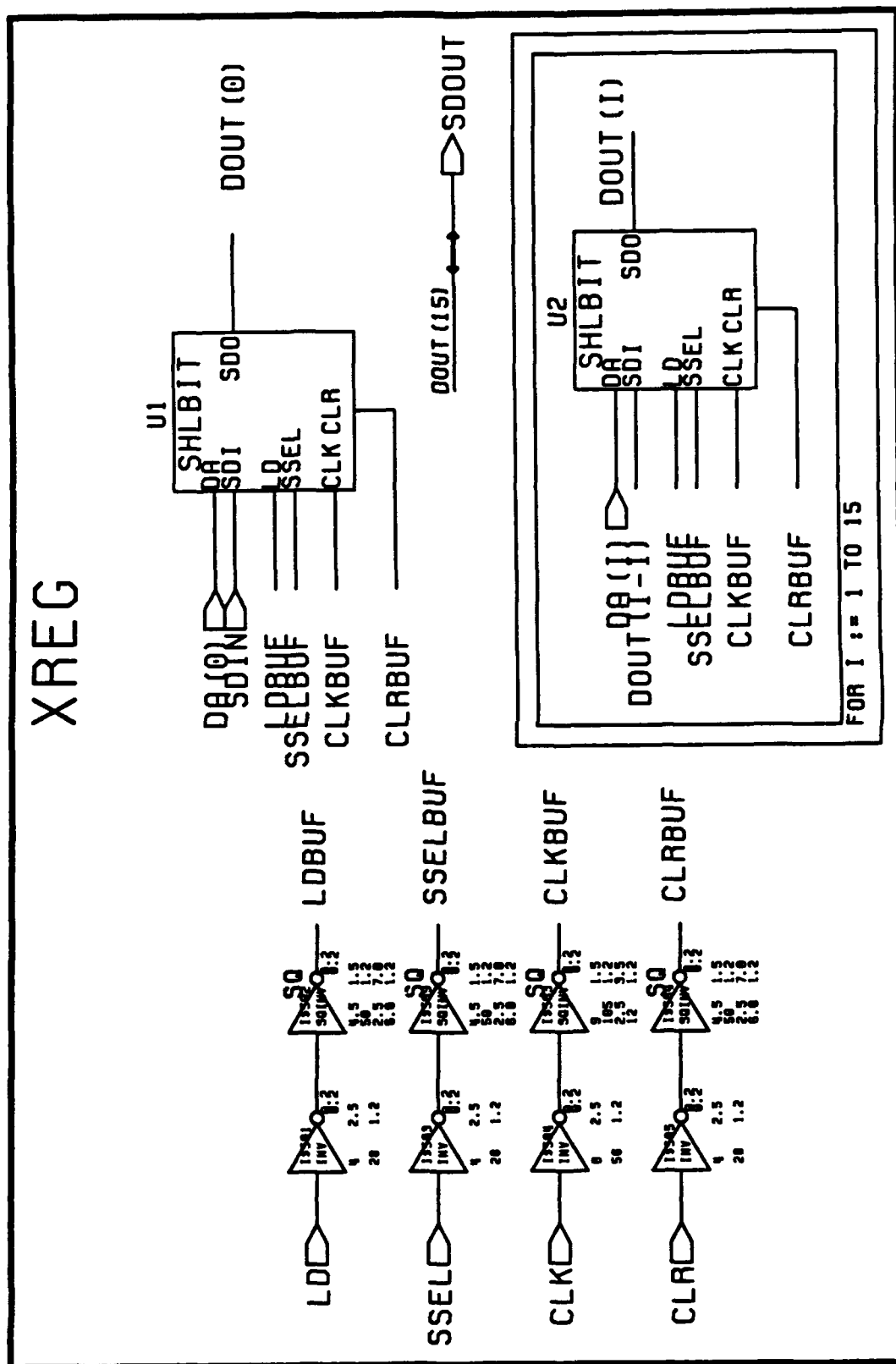


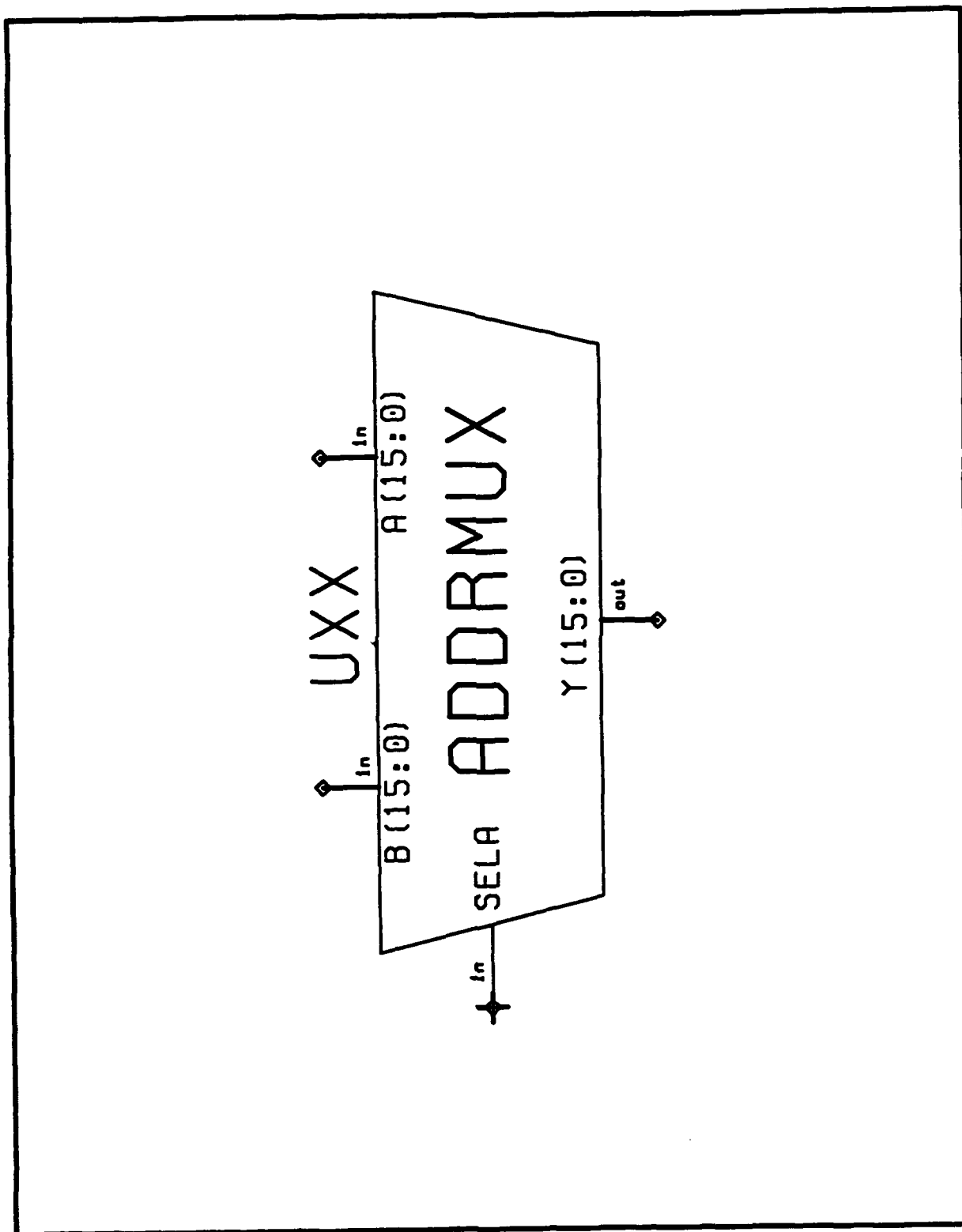
TIG03: interrupts and condition codes



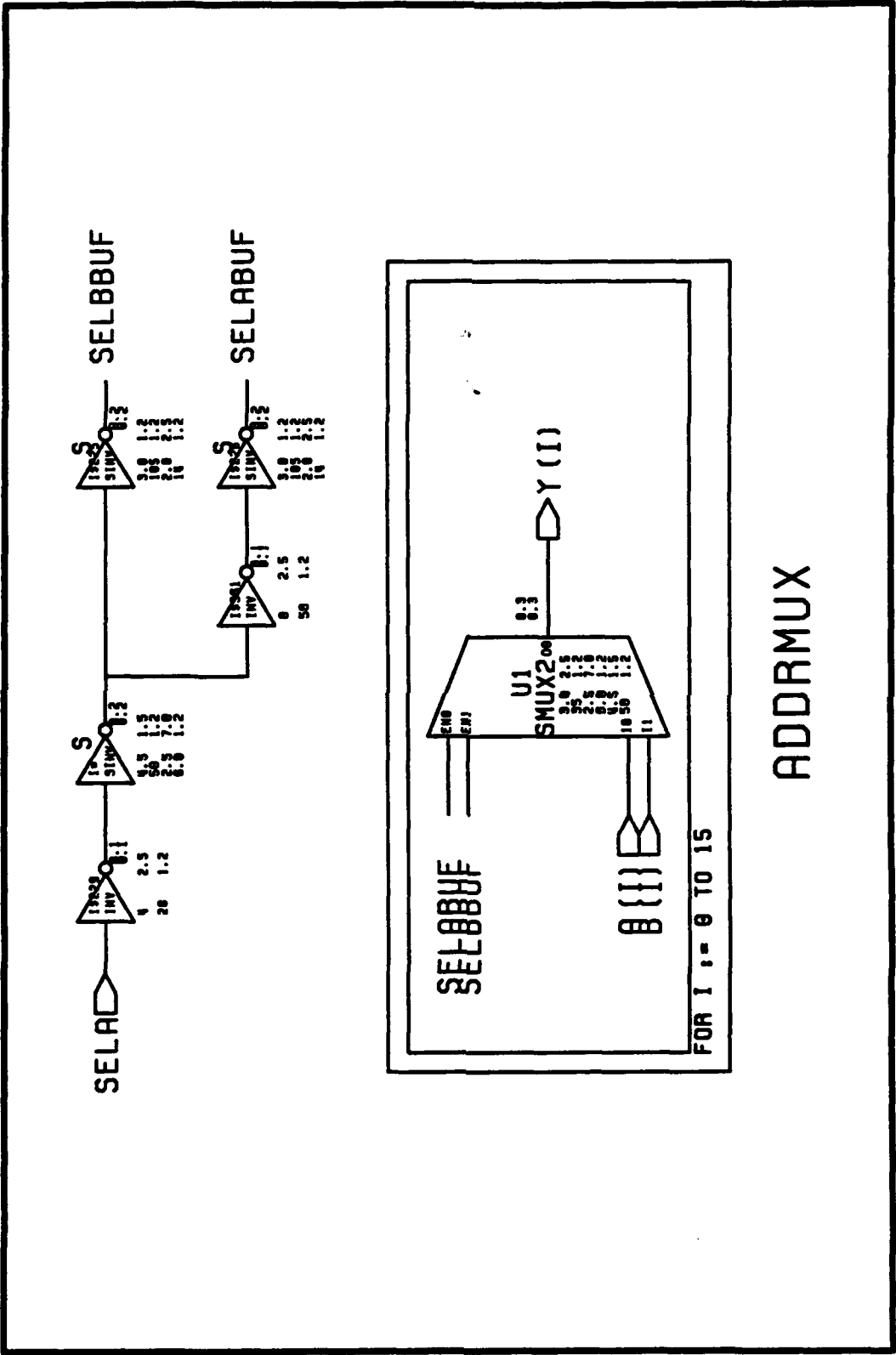


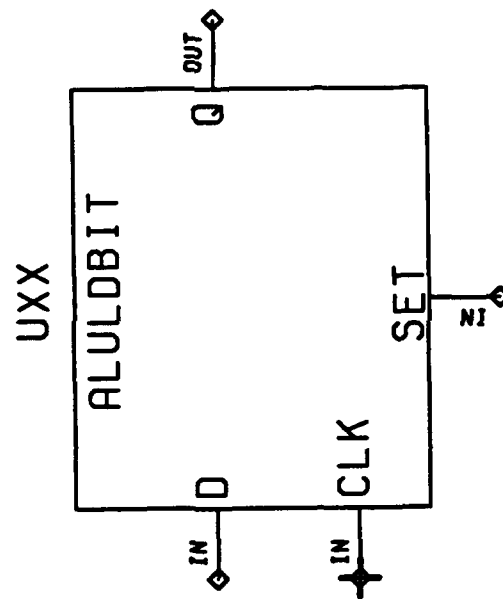


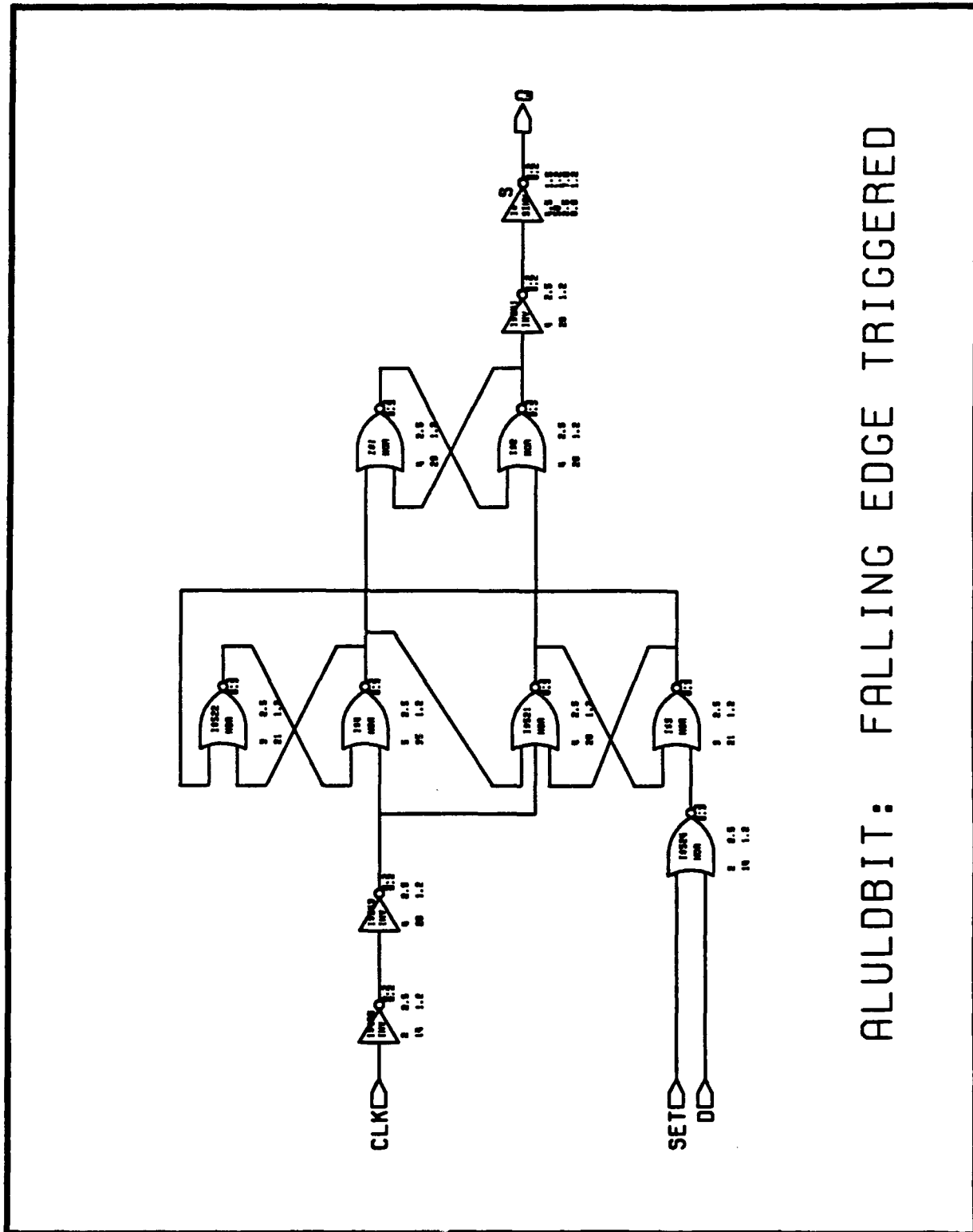


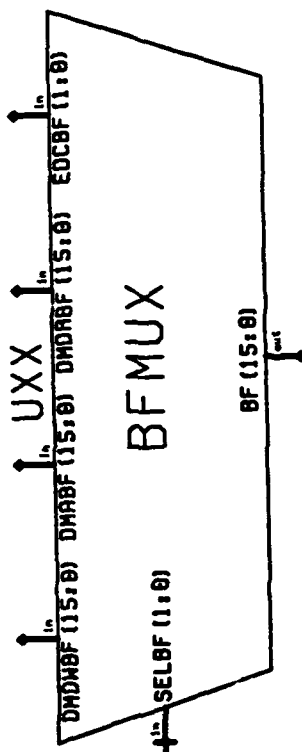


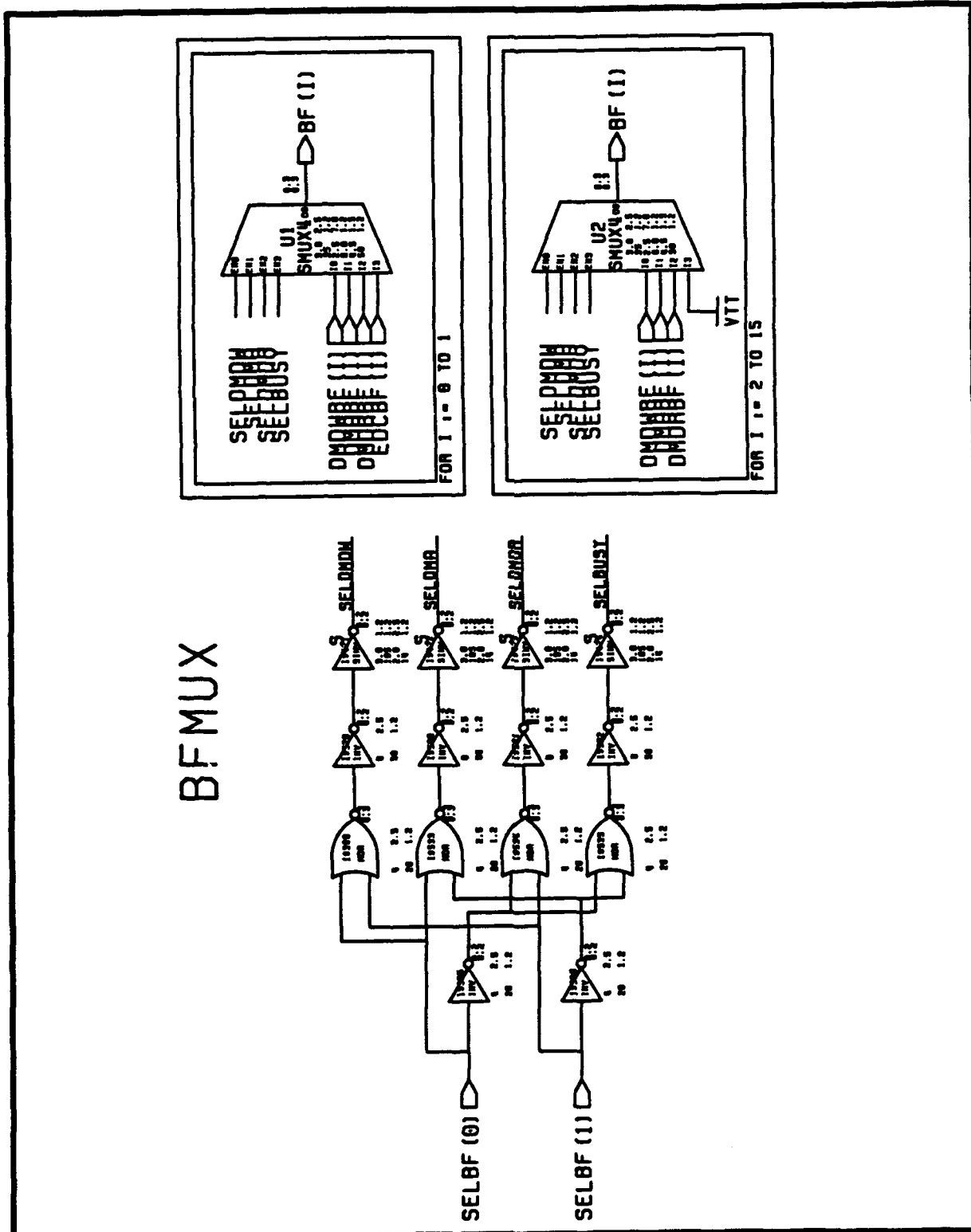






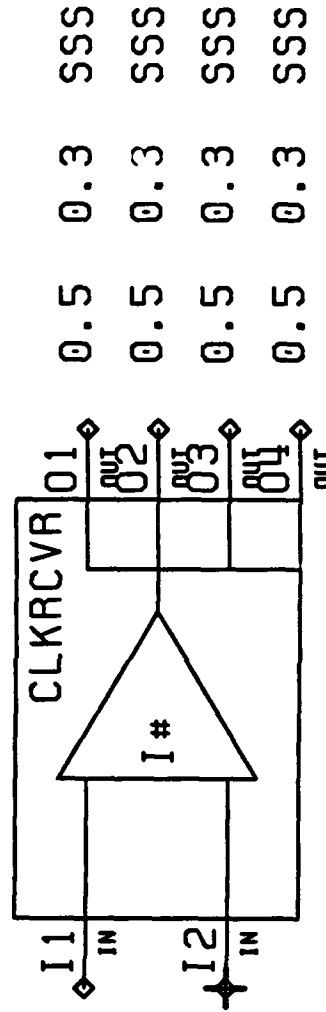






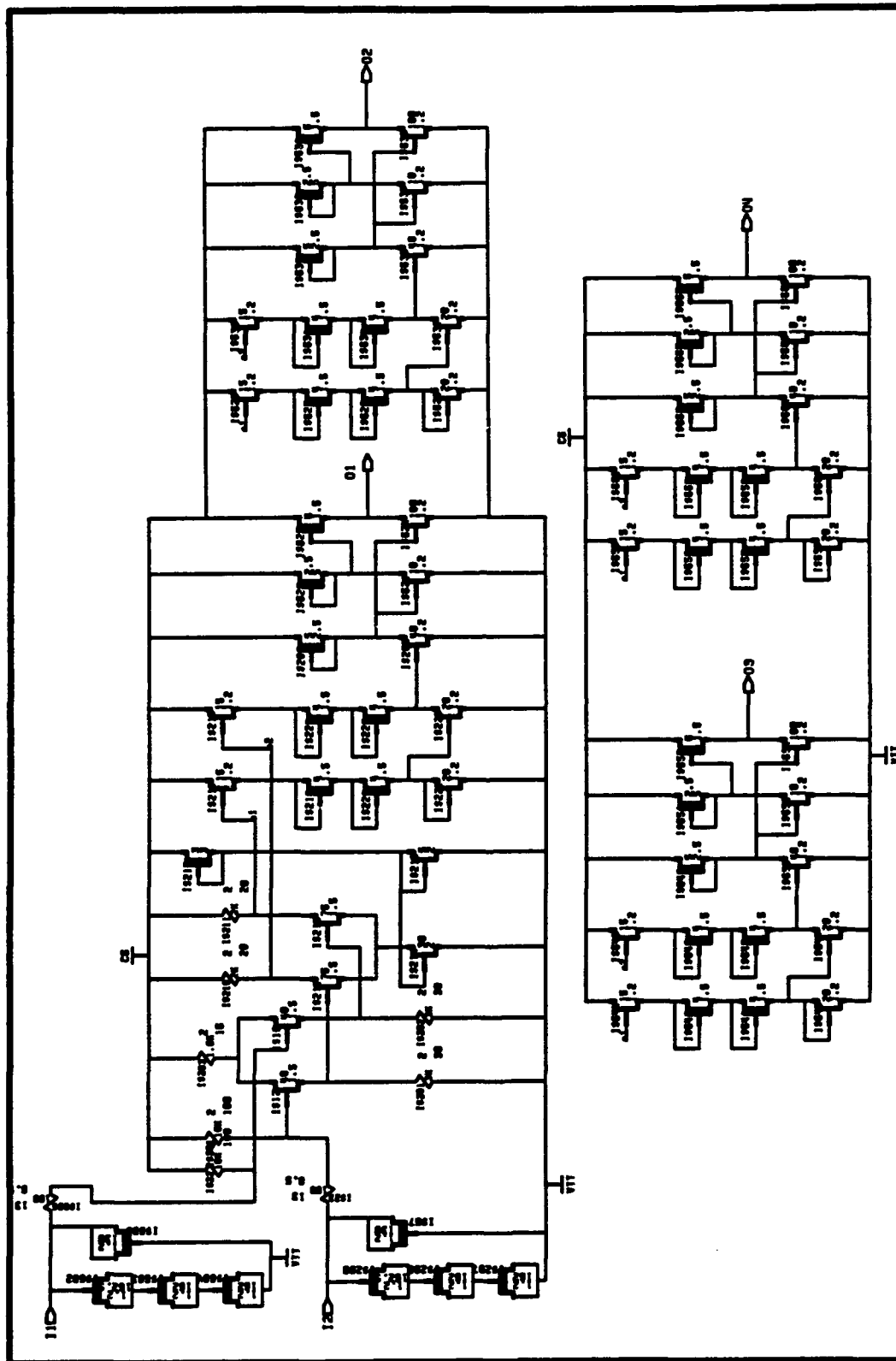
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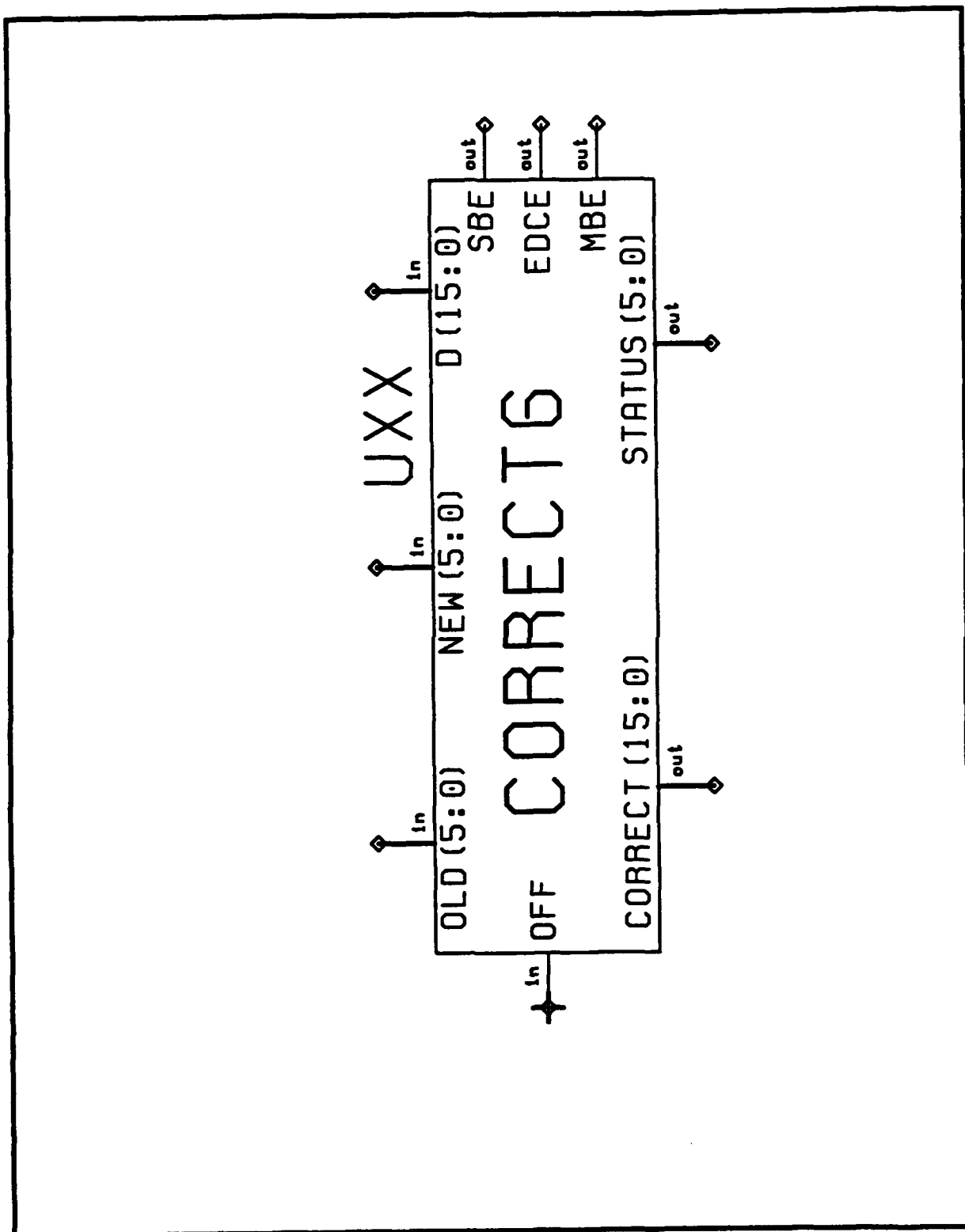
NAME: CLKRCVR  
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER



0.5	0.3	SSS
0.5	0.3	SSS
0.5	0.3	SSS
0.5	0.3	SSS

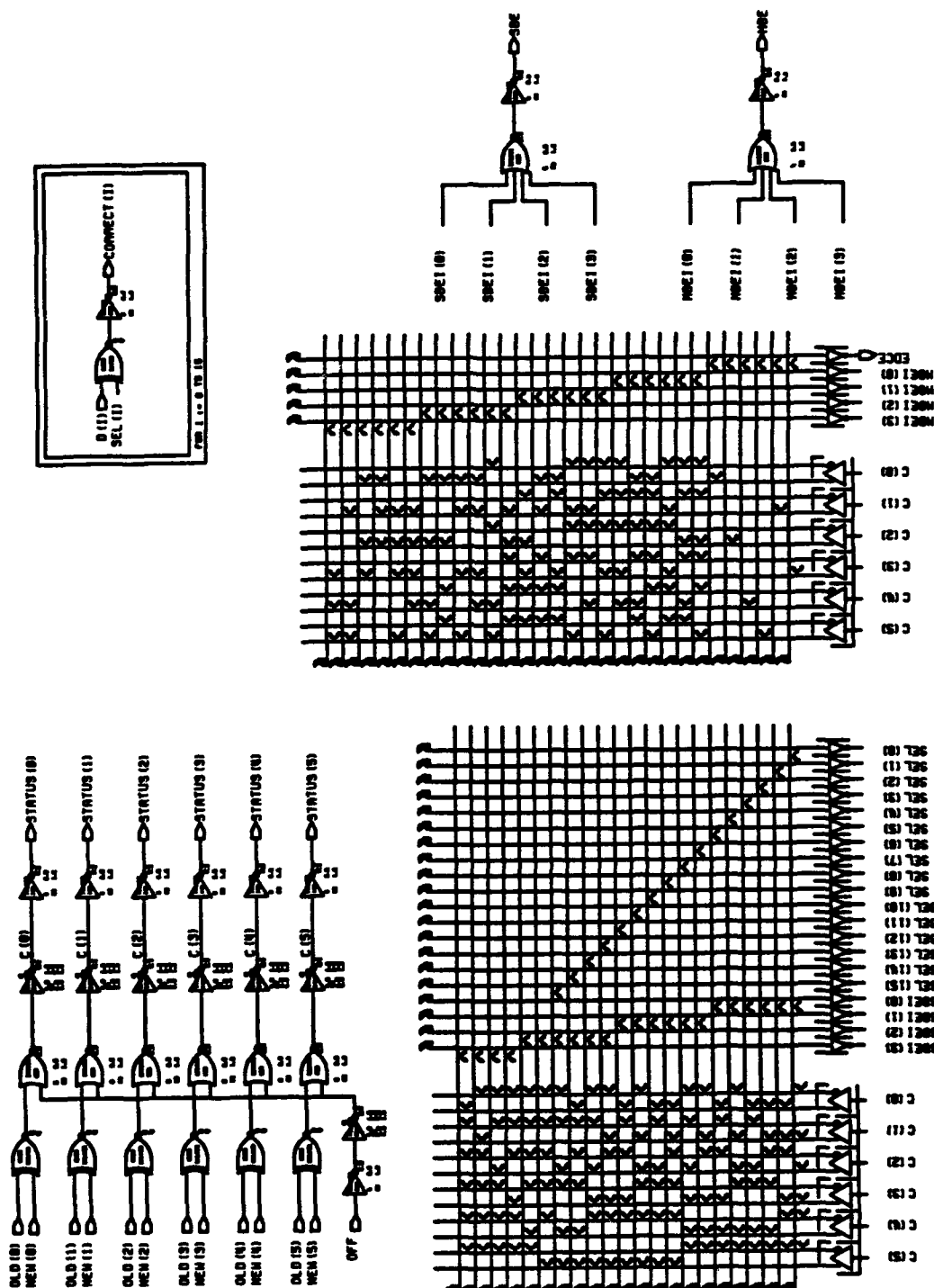
CLKRCVR  
clkrcvr.bin

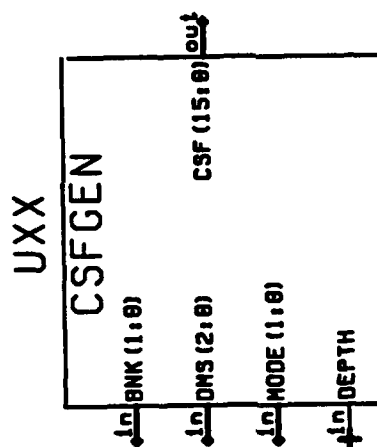


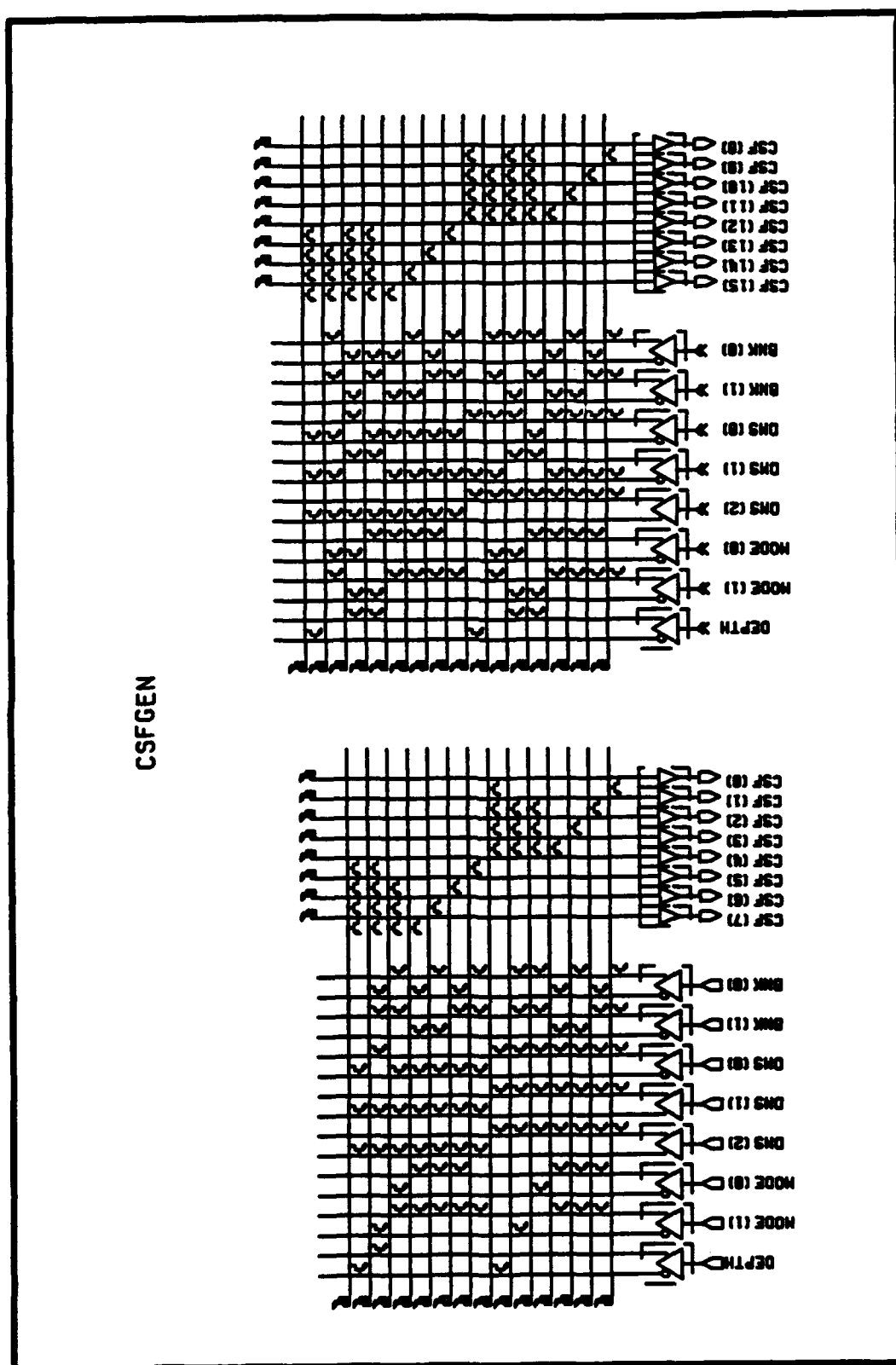


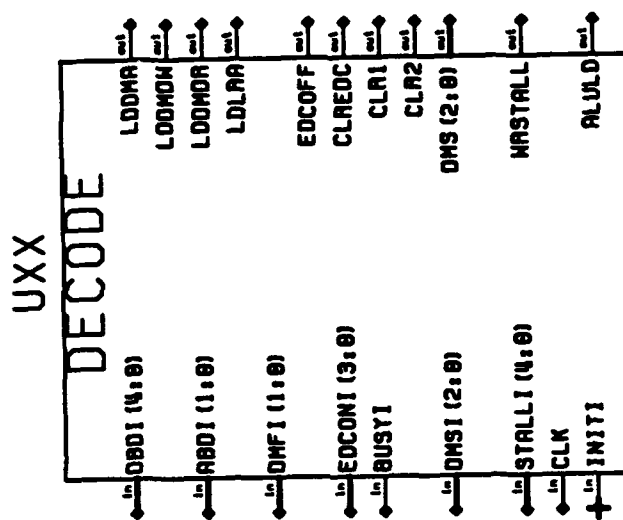


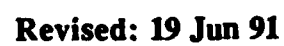
CORRECT6: 6-BIT EDC with STATUS

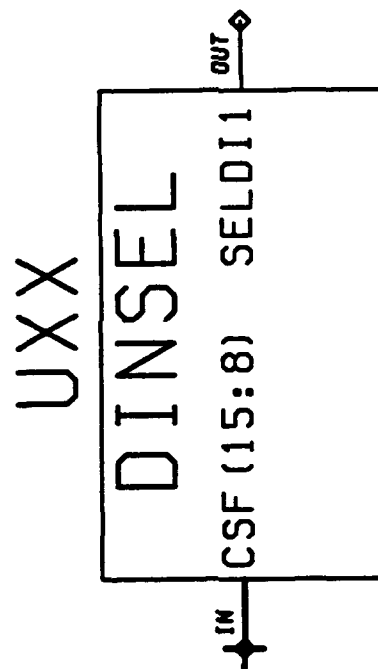


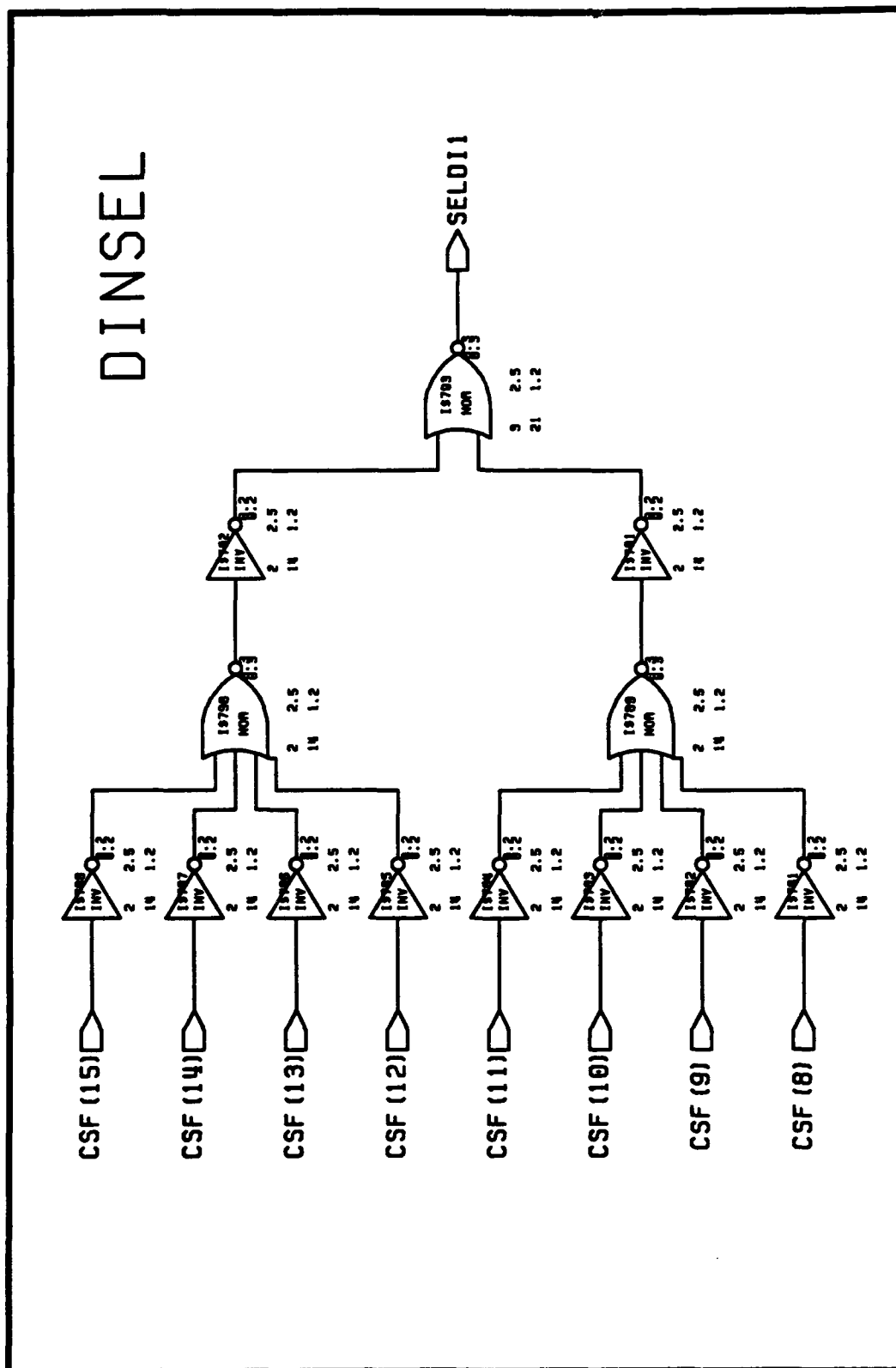


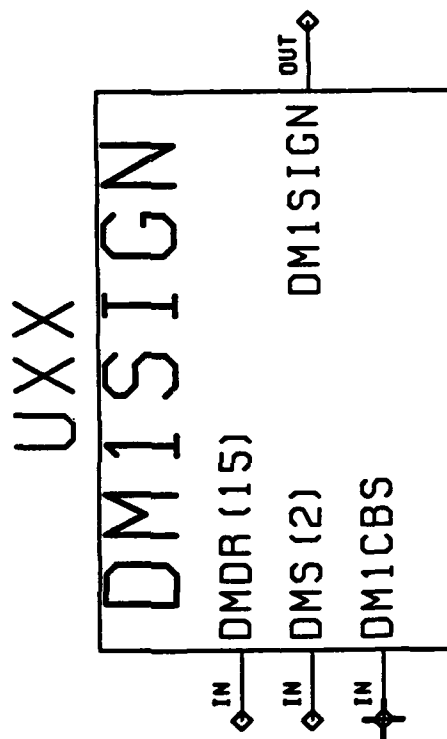




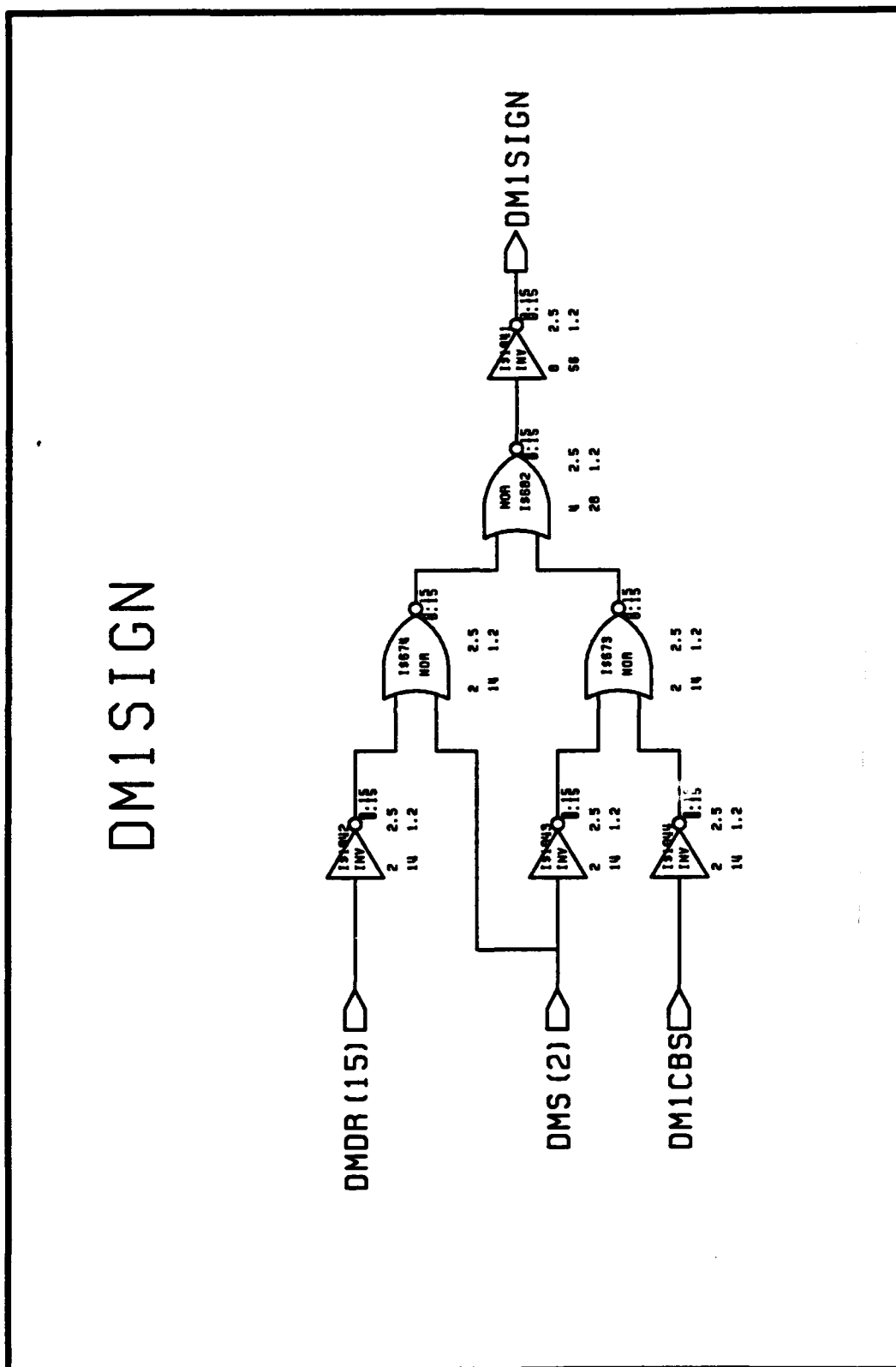










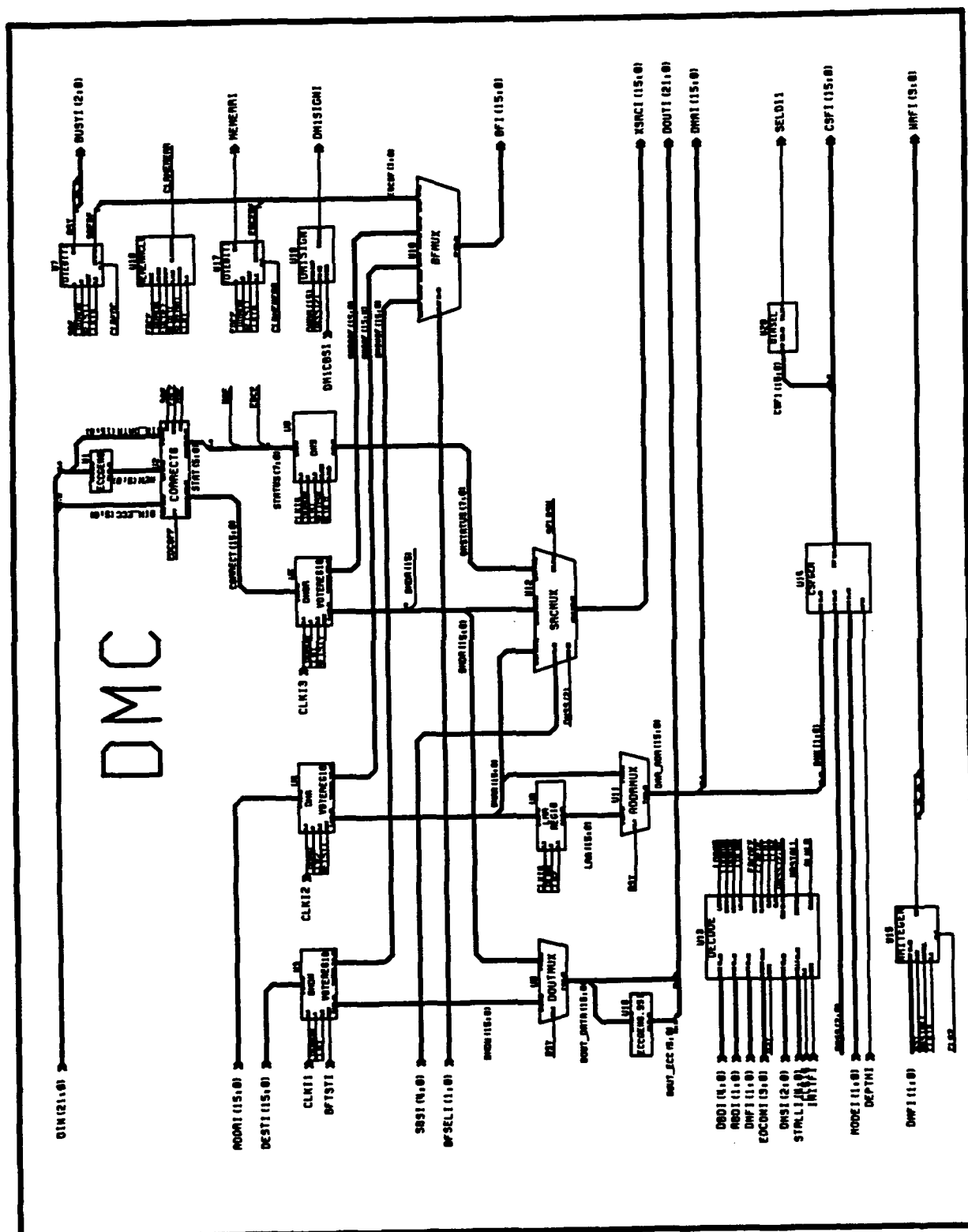


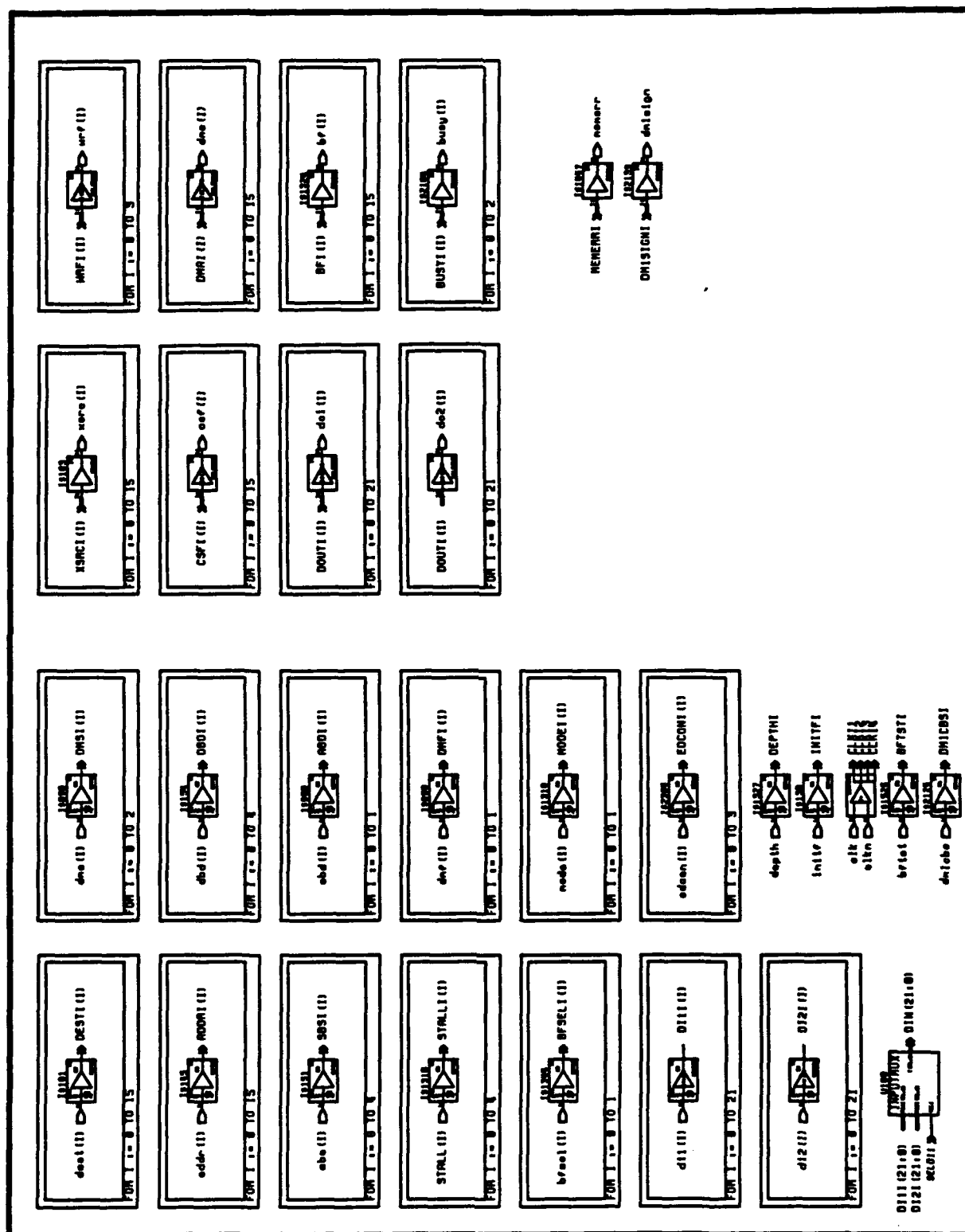
UXX

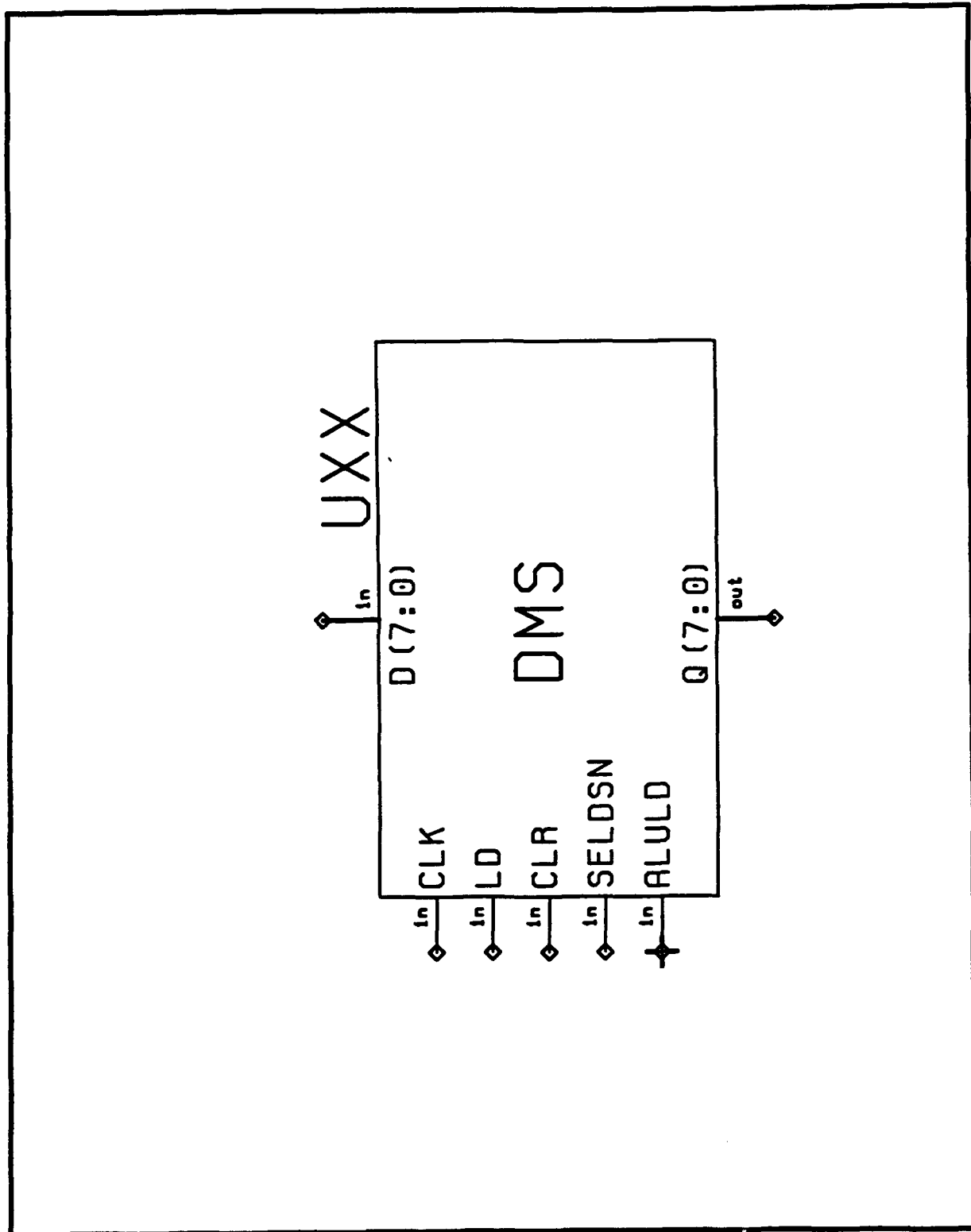
in	dest (15:0)	out	xerc (15:0)
in	addr (15:0)		
in	d11 (21:0)	out	do1 (21:0)
in	d12 (21:0)	out	do2 (21:0)
in	sbs (4:0)	out	dms (15:0)
in	dbd (4:0)	out	csf (15:0)
in	abd (1:0)	out	wrf (3:0)
in	dms (1:0)		
in	dms (2:0)		
in	edcon (3:0)		
in	dmlcbs	out	dmlcgn
in	depth		
in	mode (1:0)		
in	bfael (1:0)	out	bf (15:0)
in	bftst		
in	lnl1f	out	buey (2:0)
in	stall (4:0)	out	memerr
in	clk		
in	clkn		

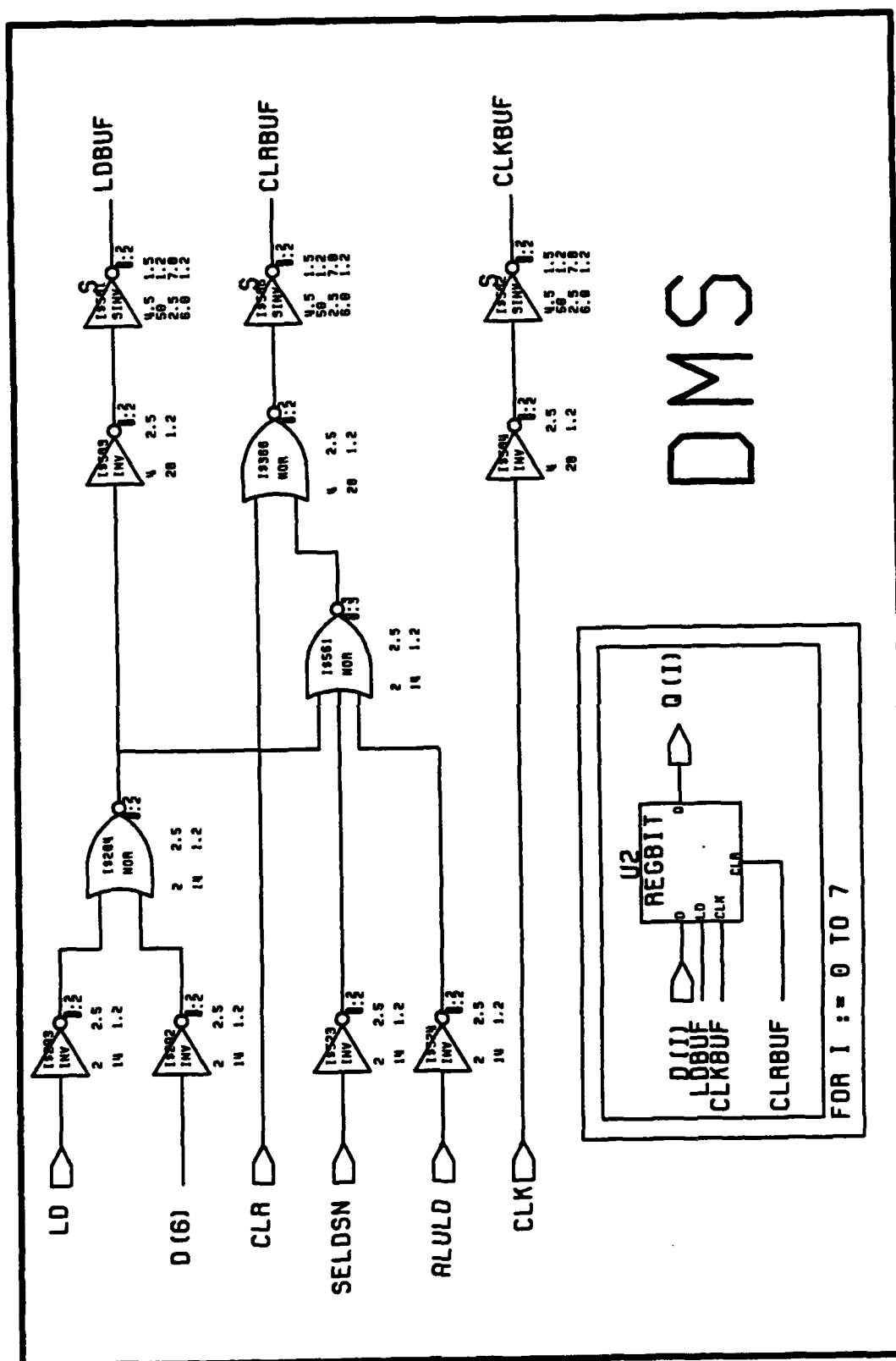
DMC

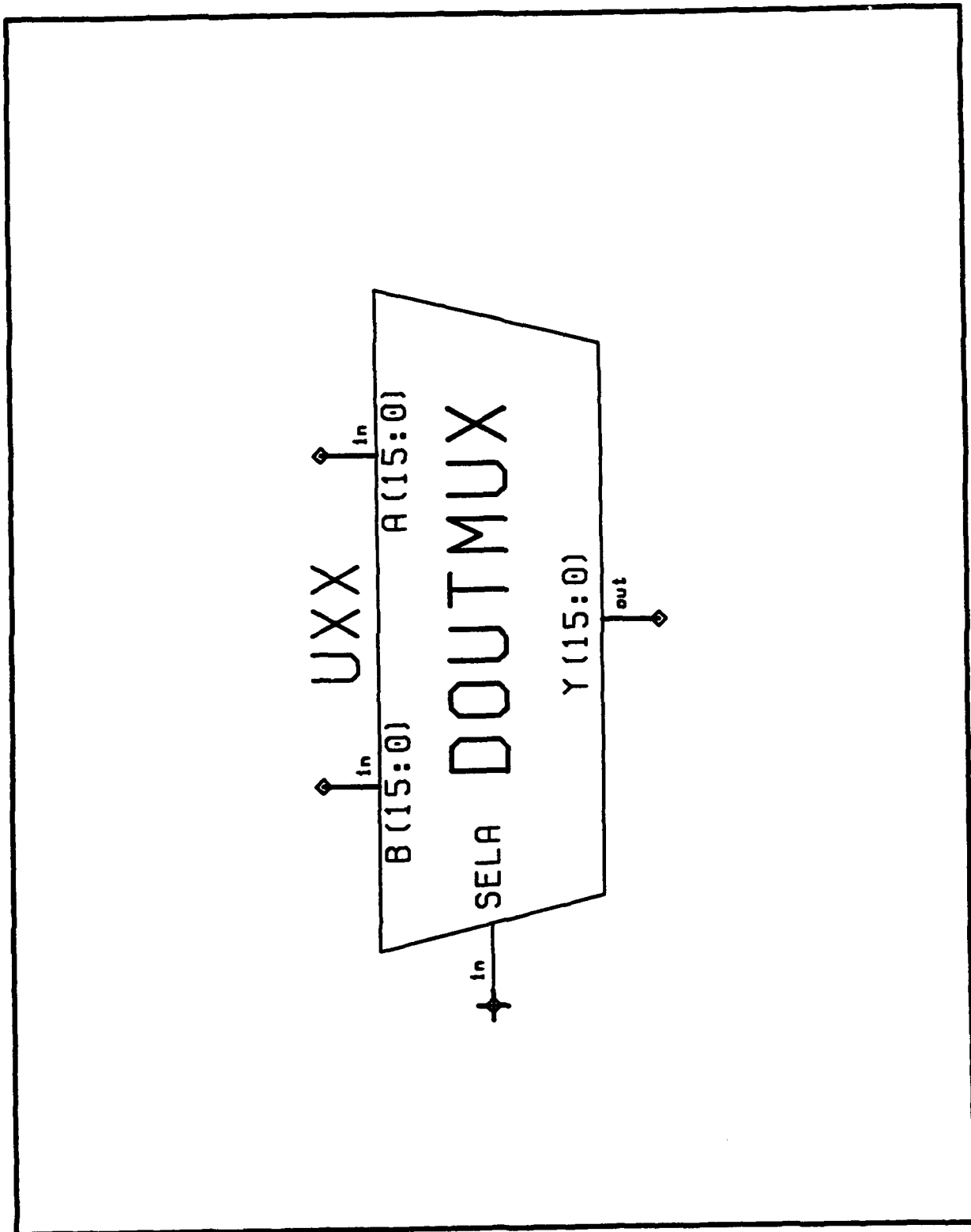
DMC  
dmc.bin

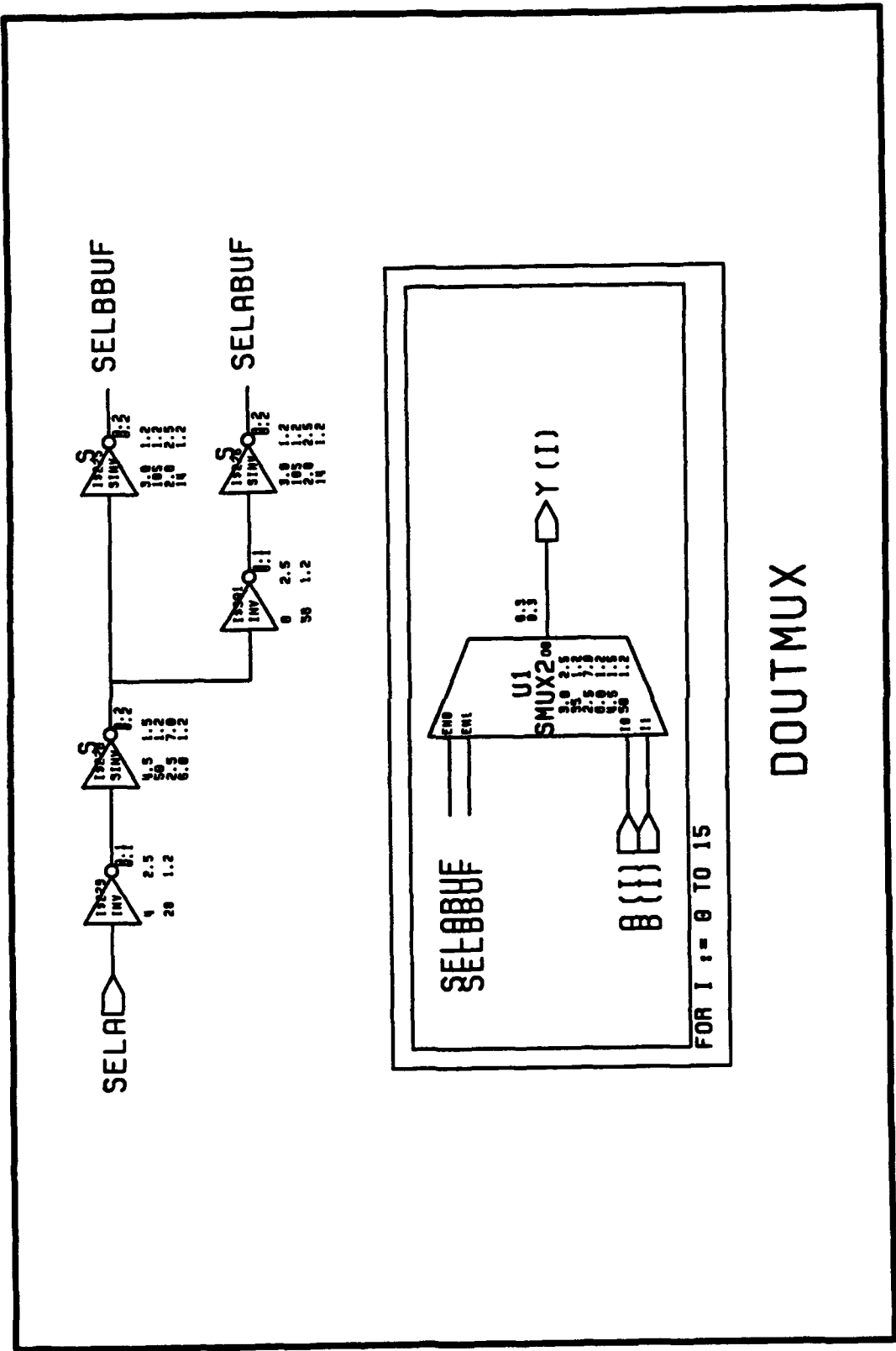












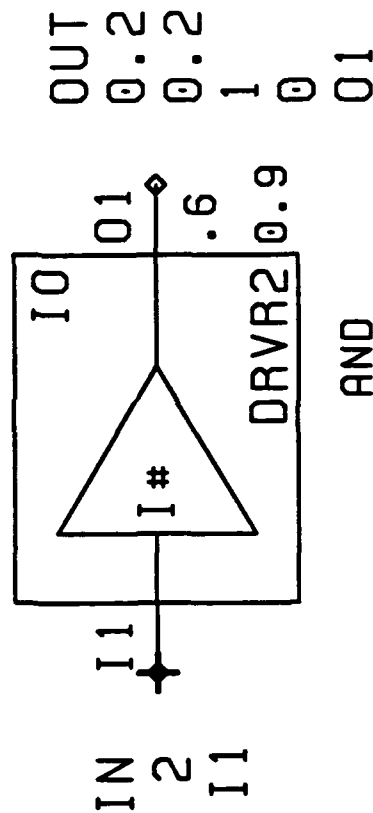


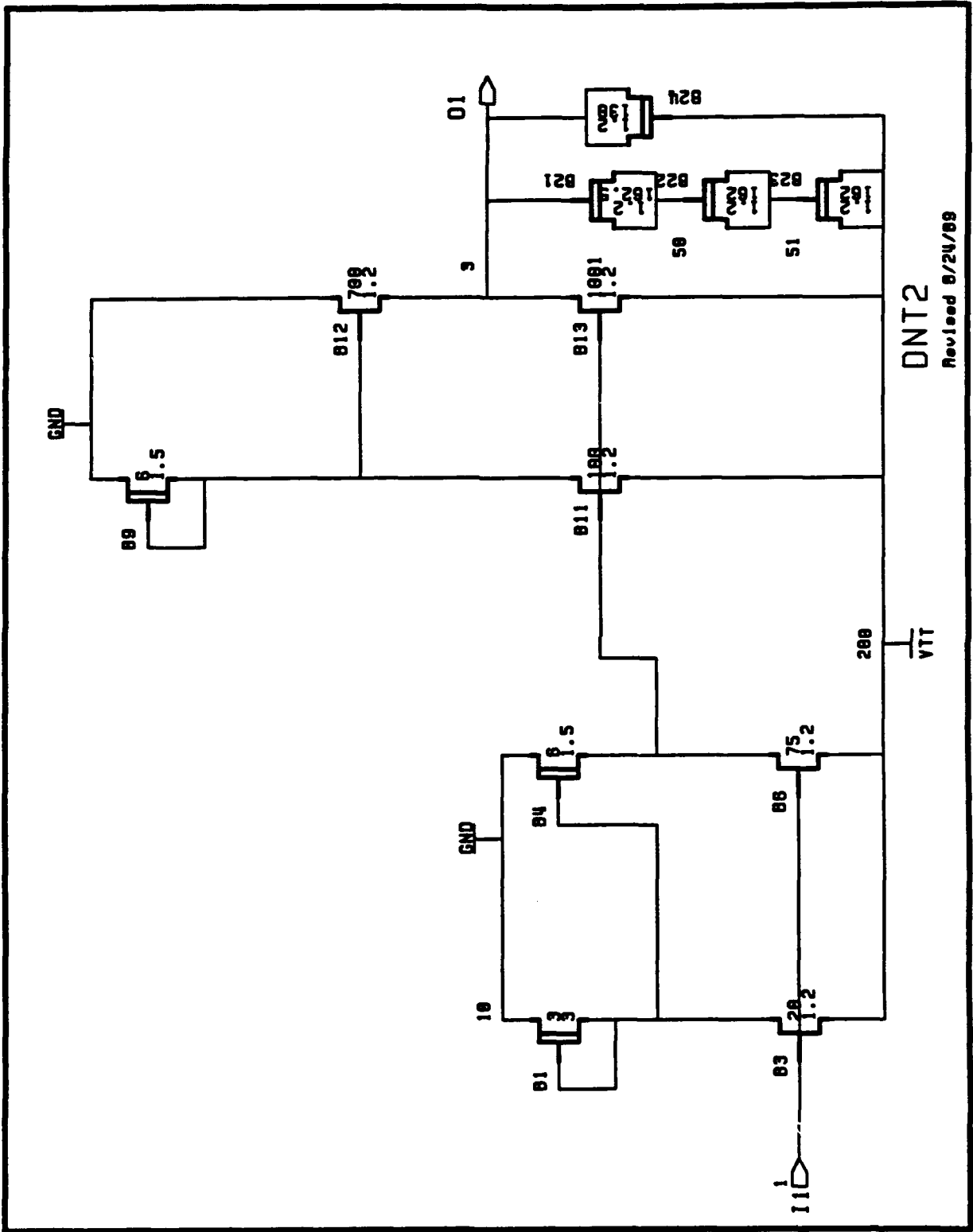
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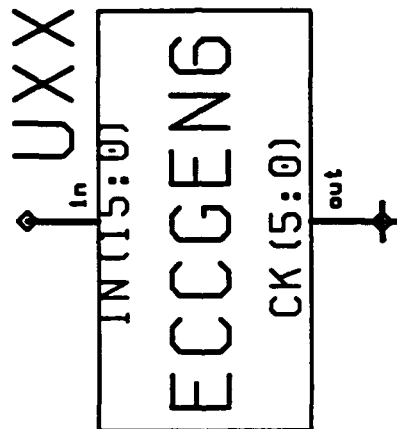
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NAME: DRVR2

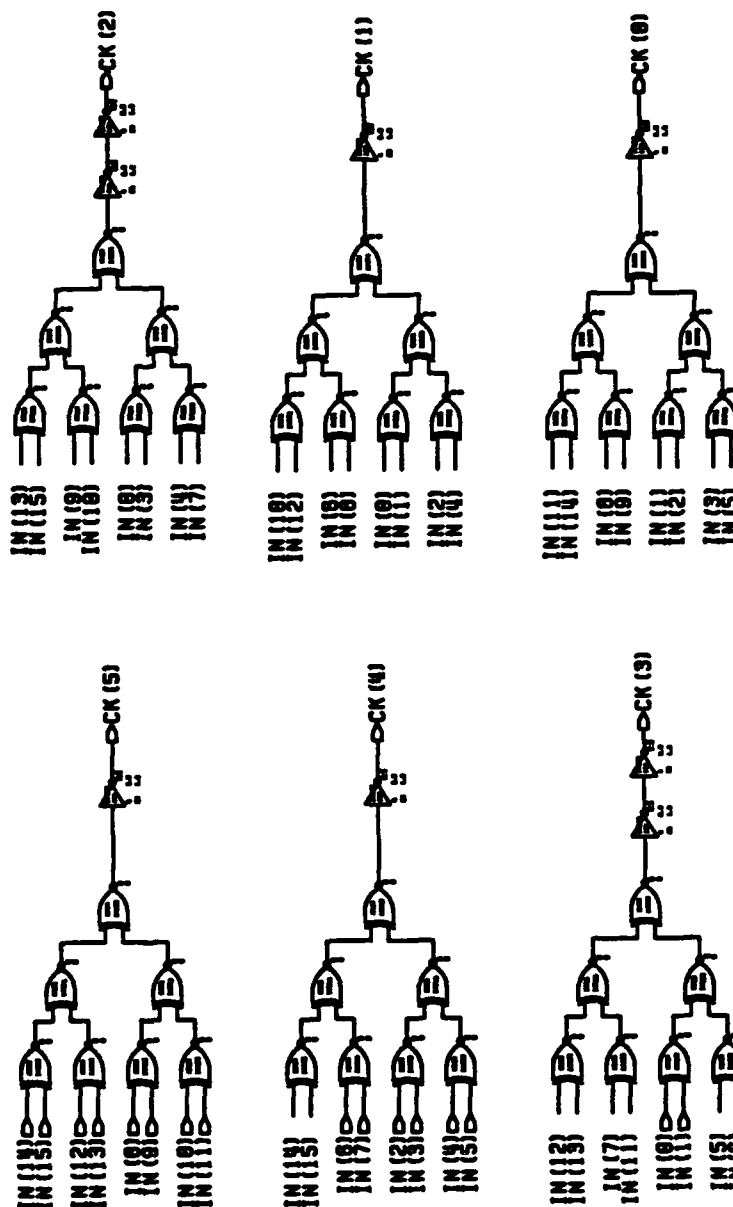
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD

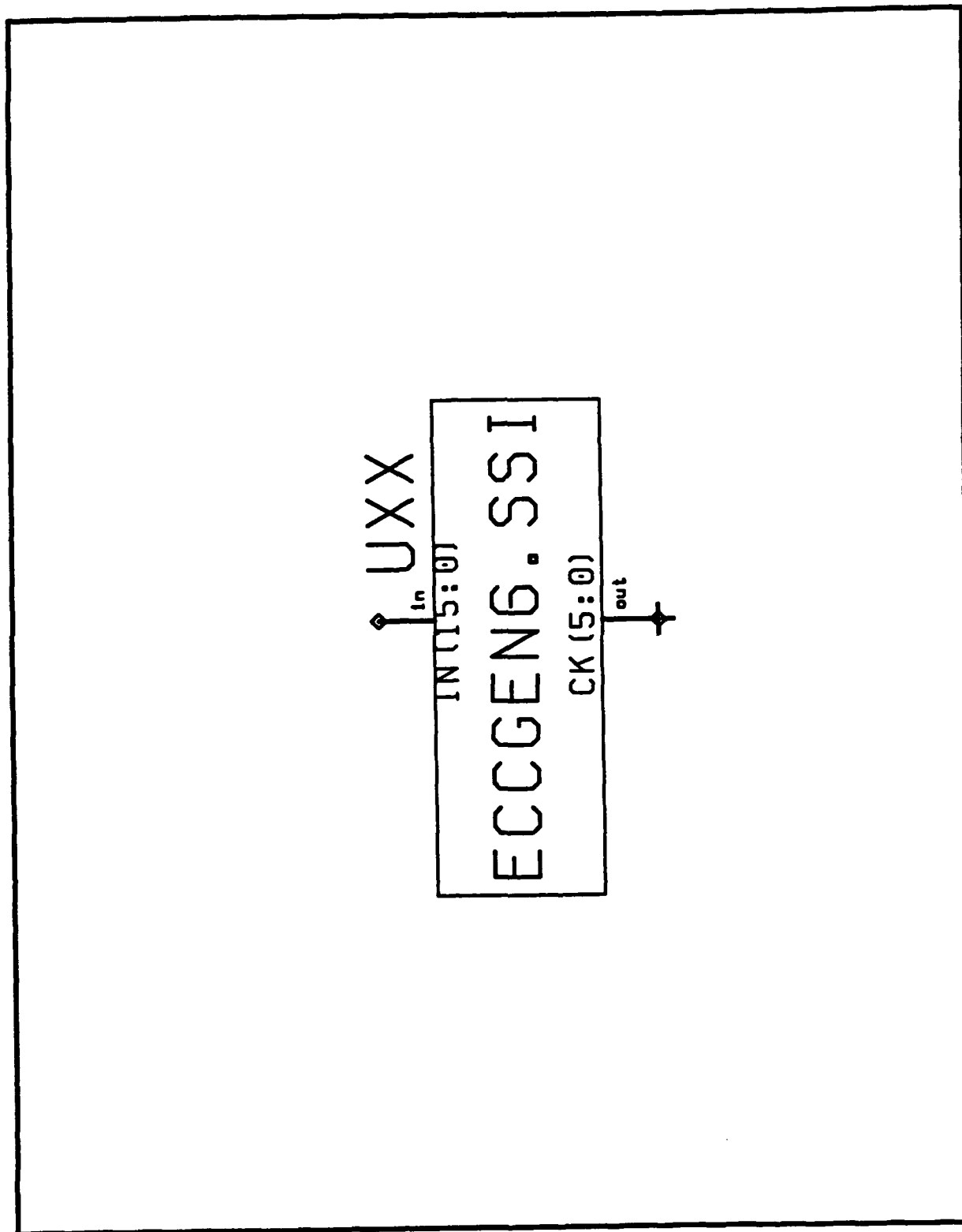




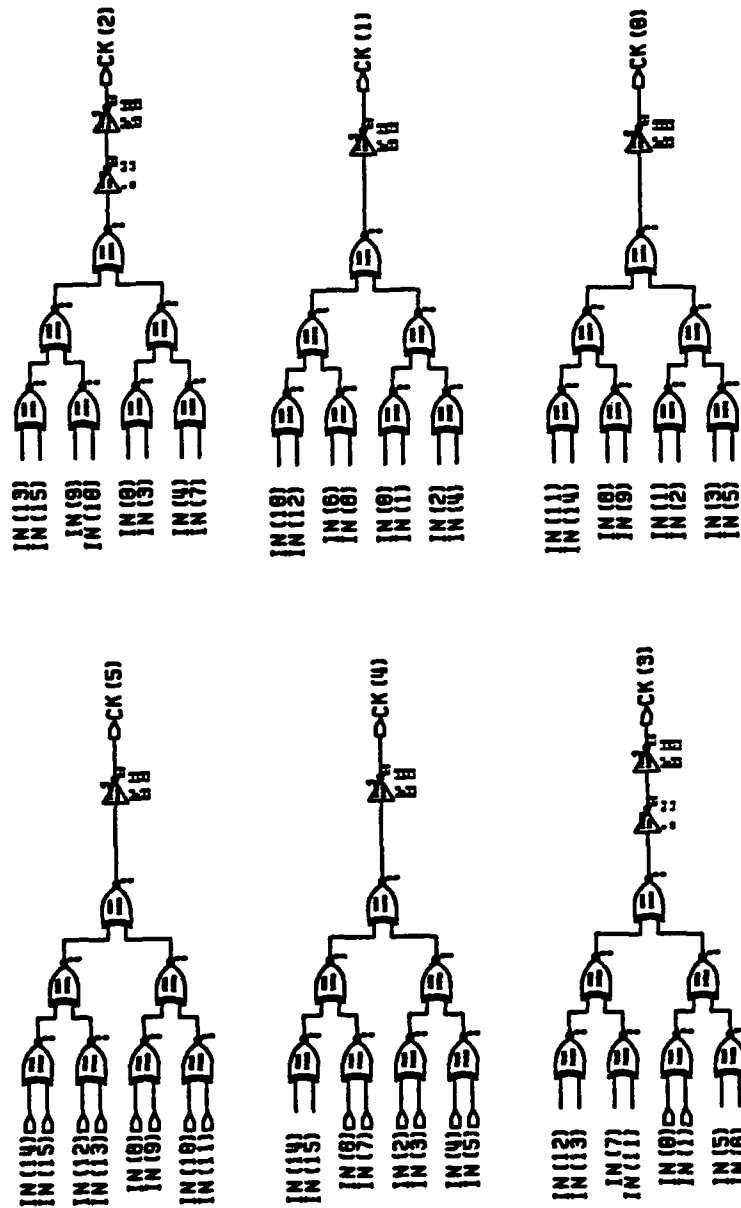


ECCGEN6: ECC CHECK BIT GENERATION





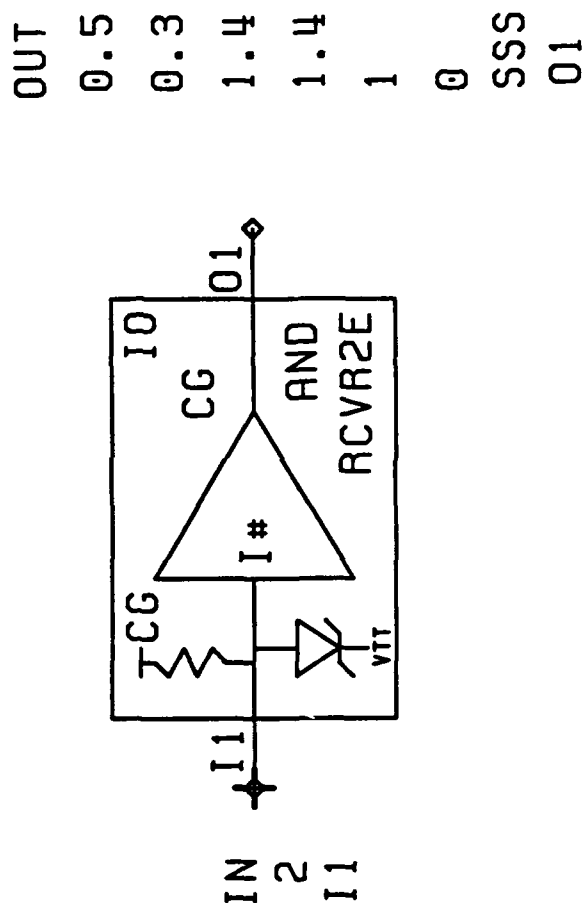
ECCGEN6.SSI: ECC CHECK BIT GENERATION

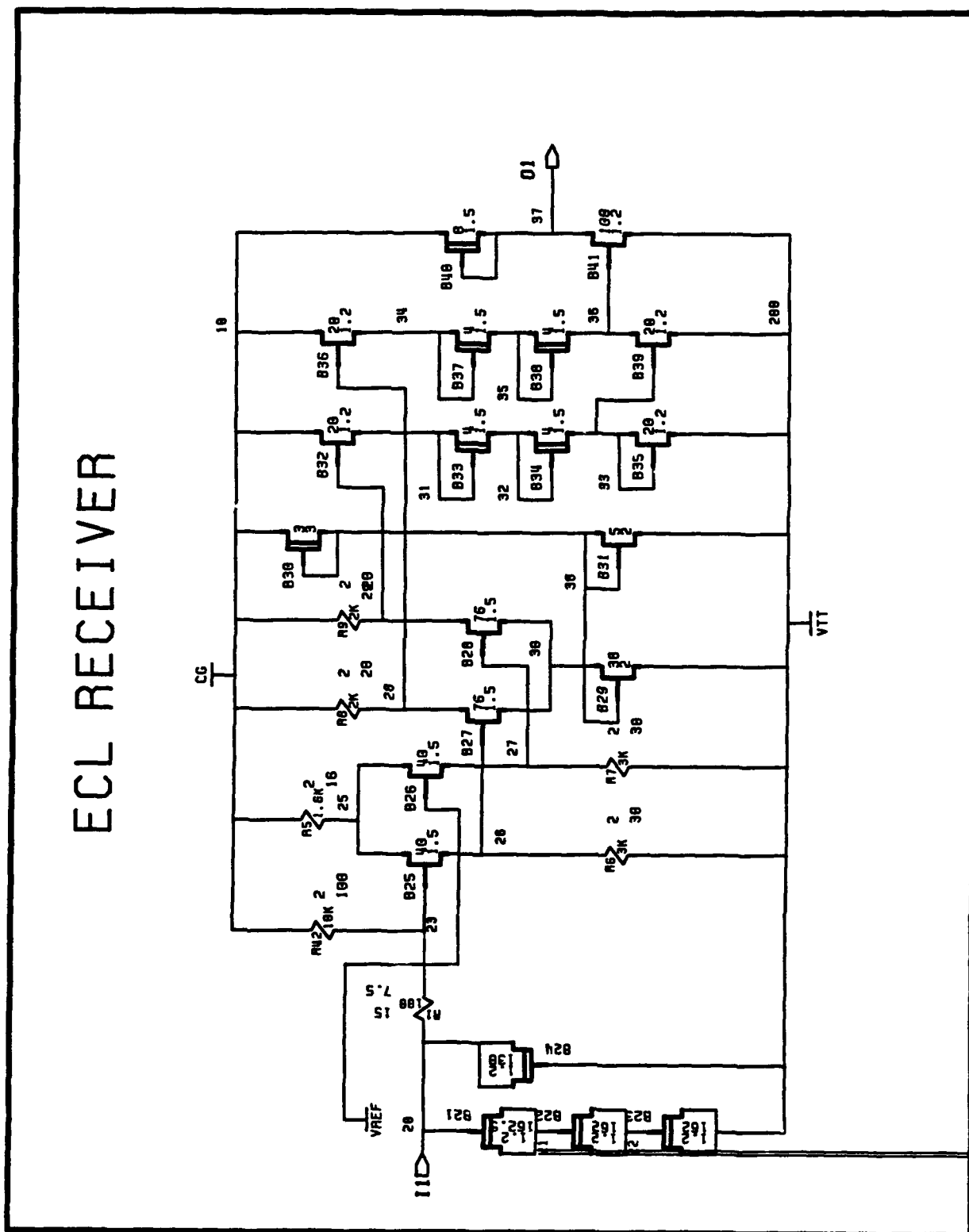


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NAME: RCVR2E

DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD





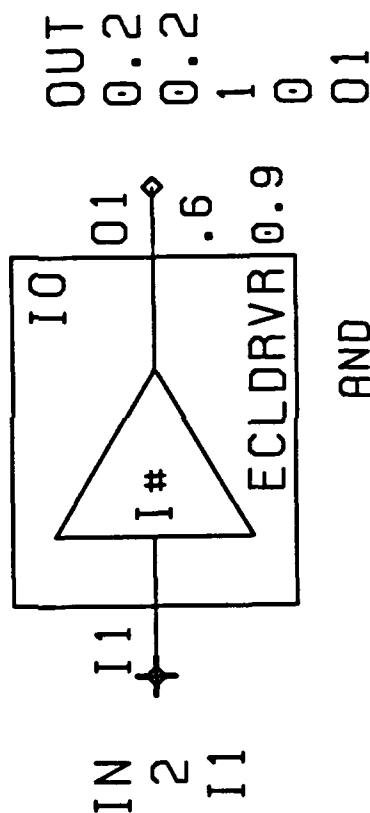


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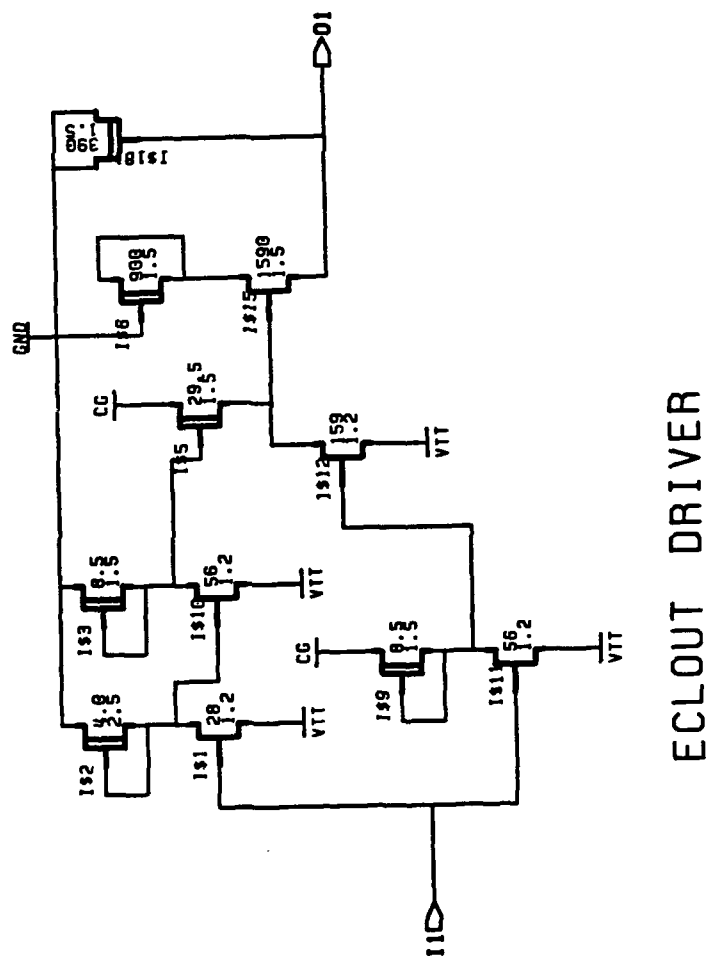
Version 0.8

NAME: ECLOUT

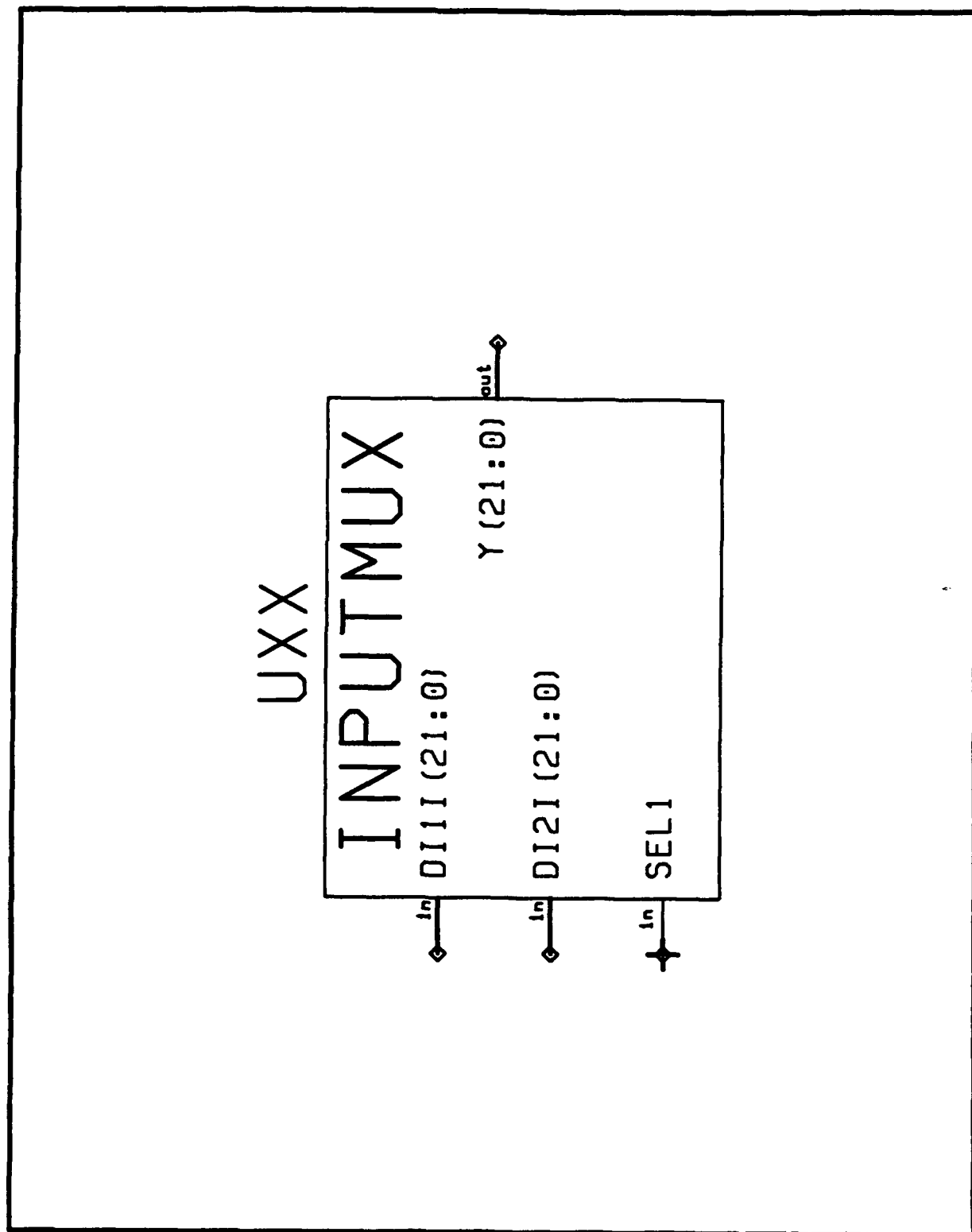
DESCRIPTION: ECL OUTPUT DRVR FOR DMC

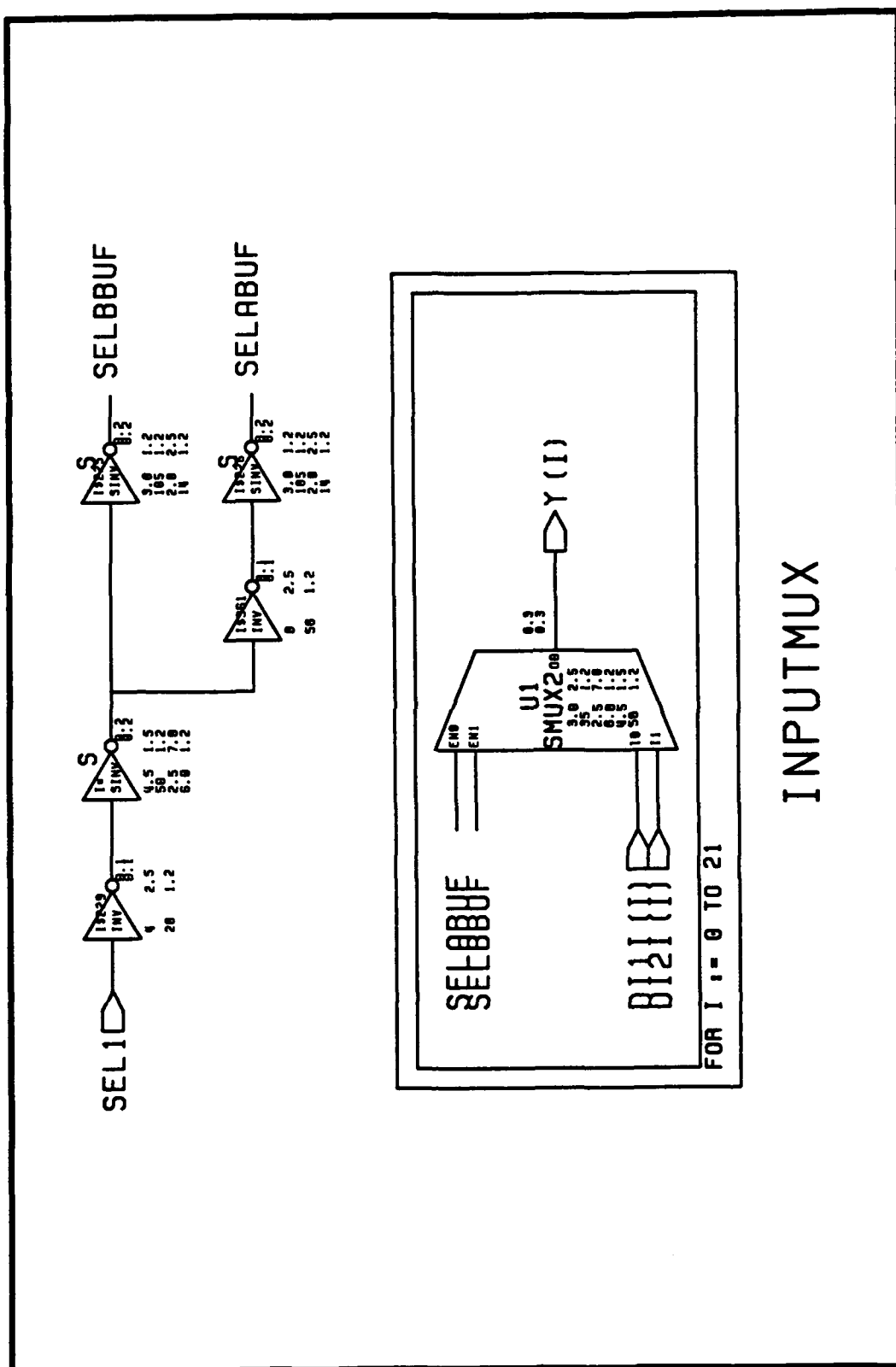


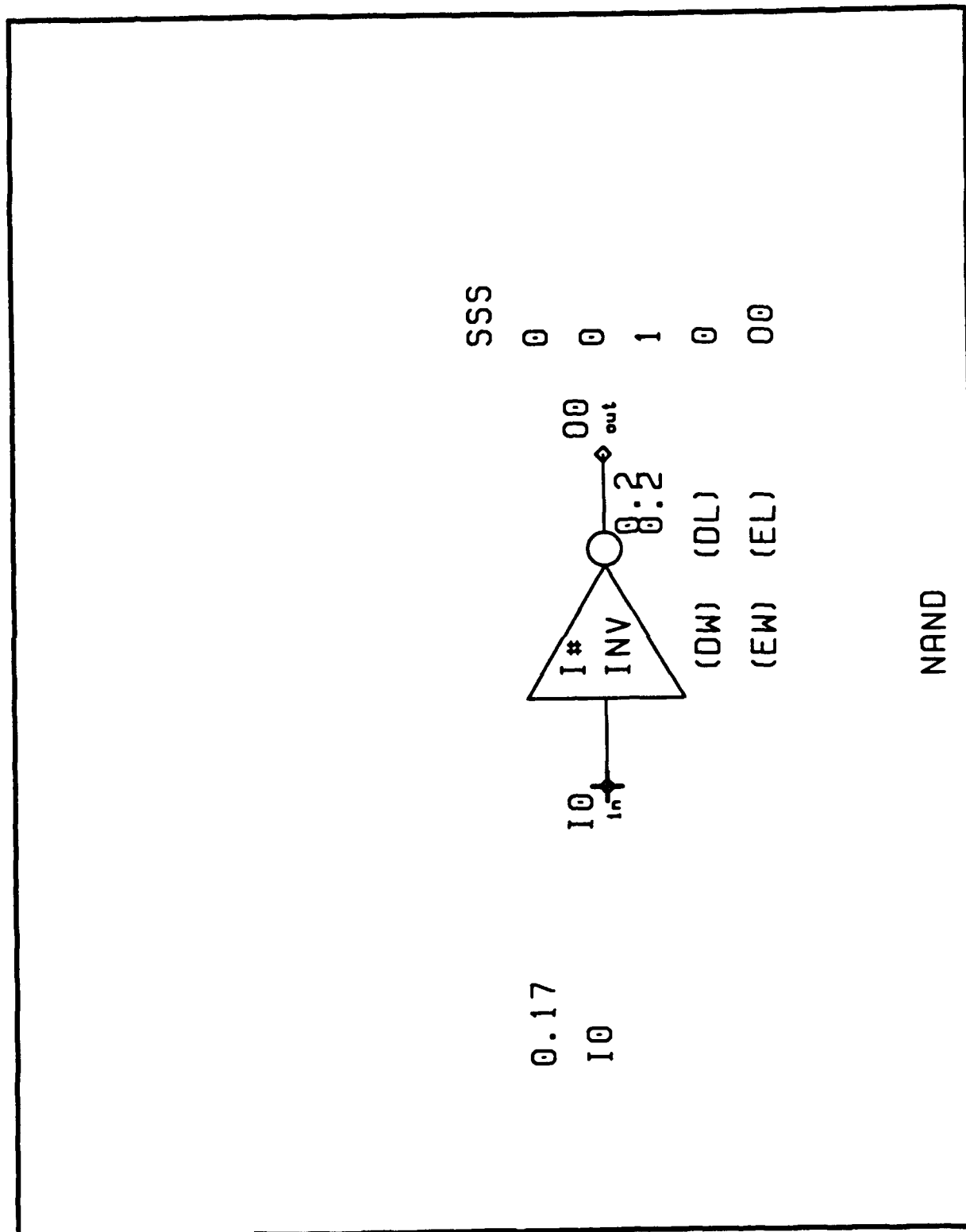
AND

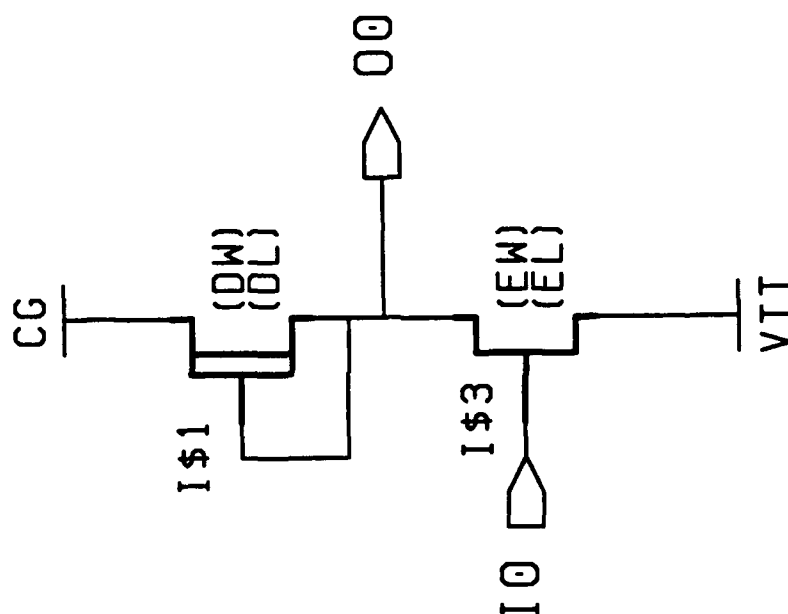


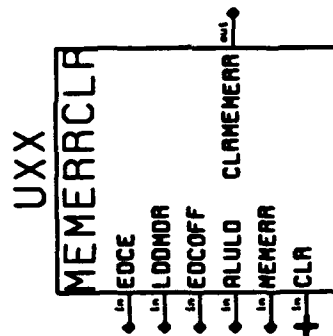
ECLOUT DRIVER





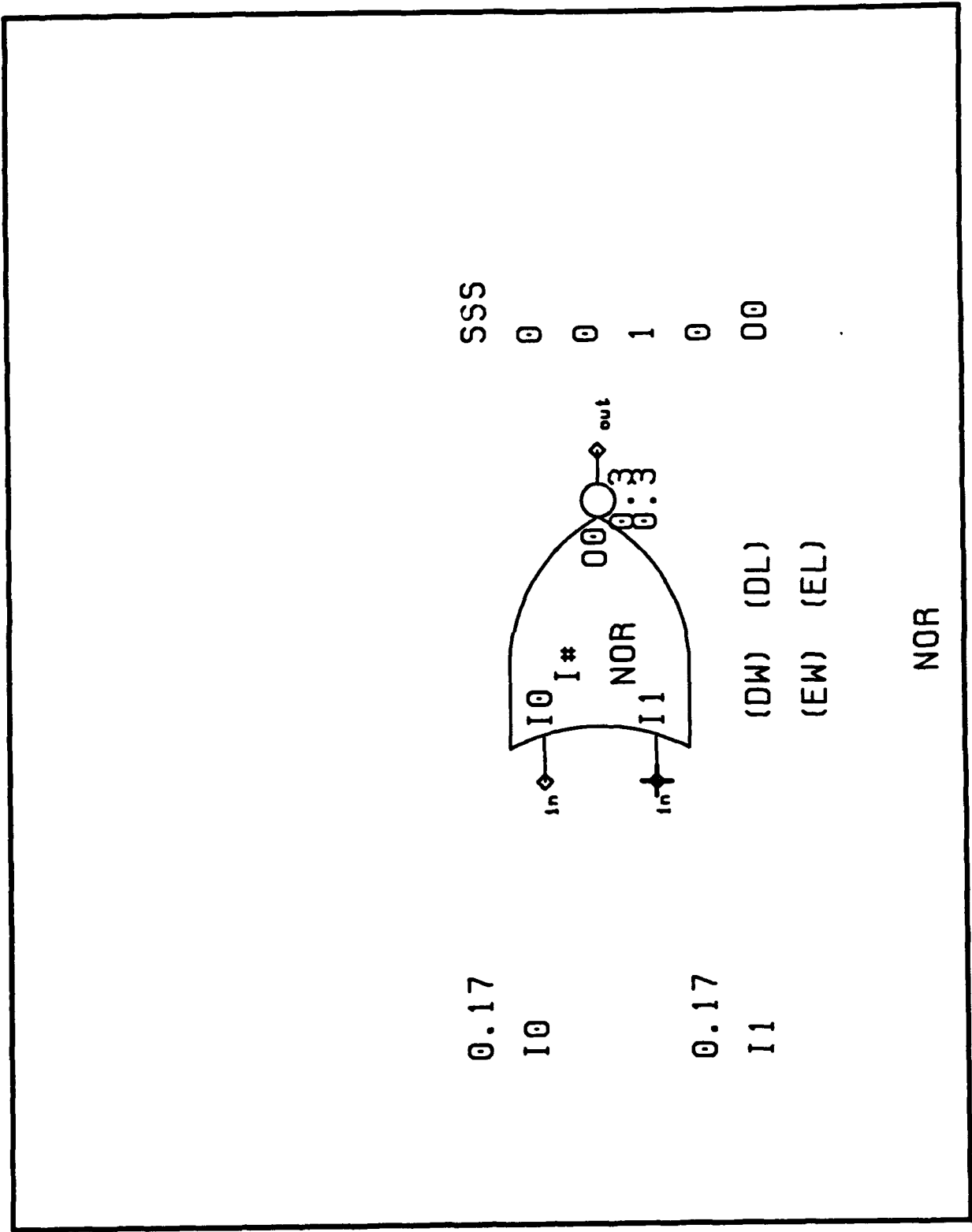


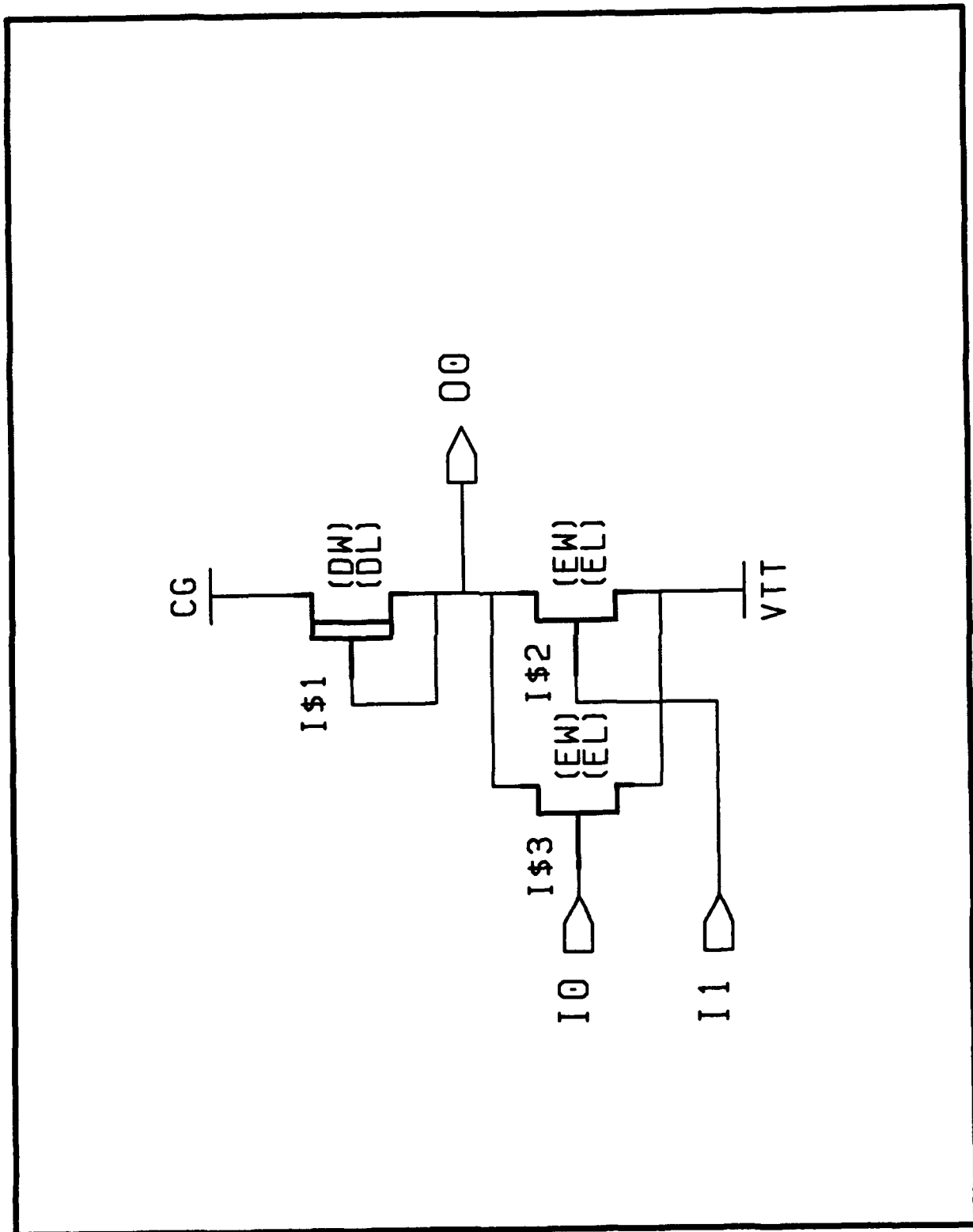


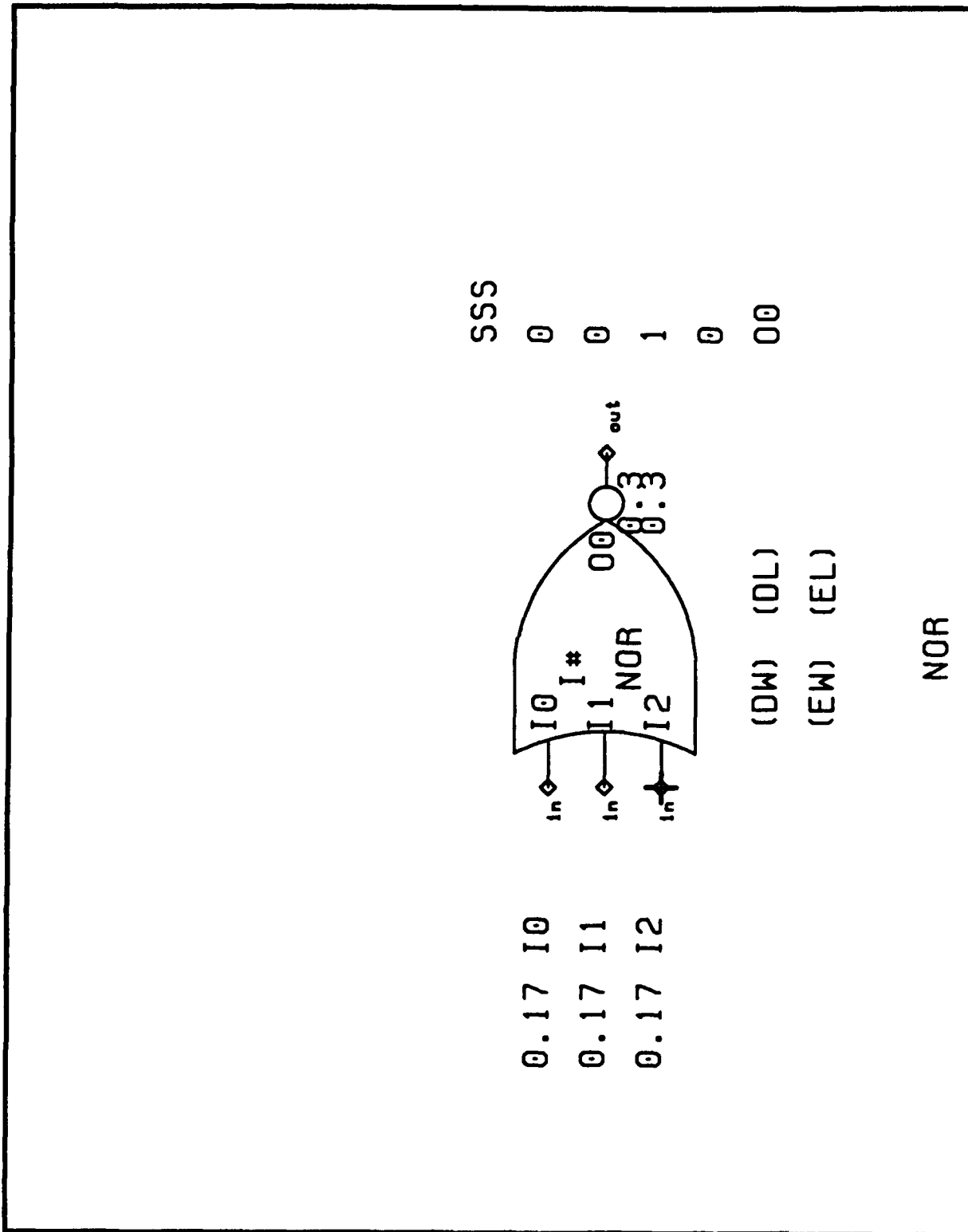


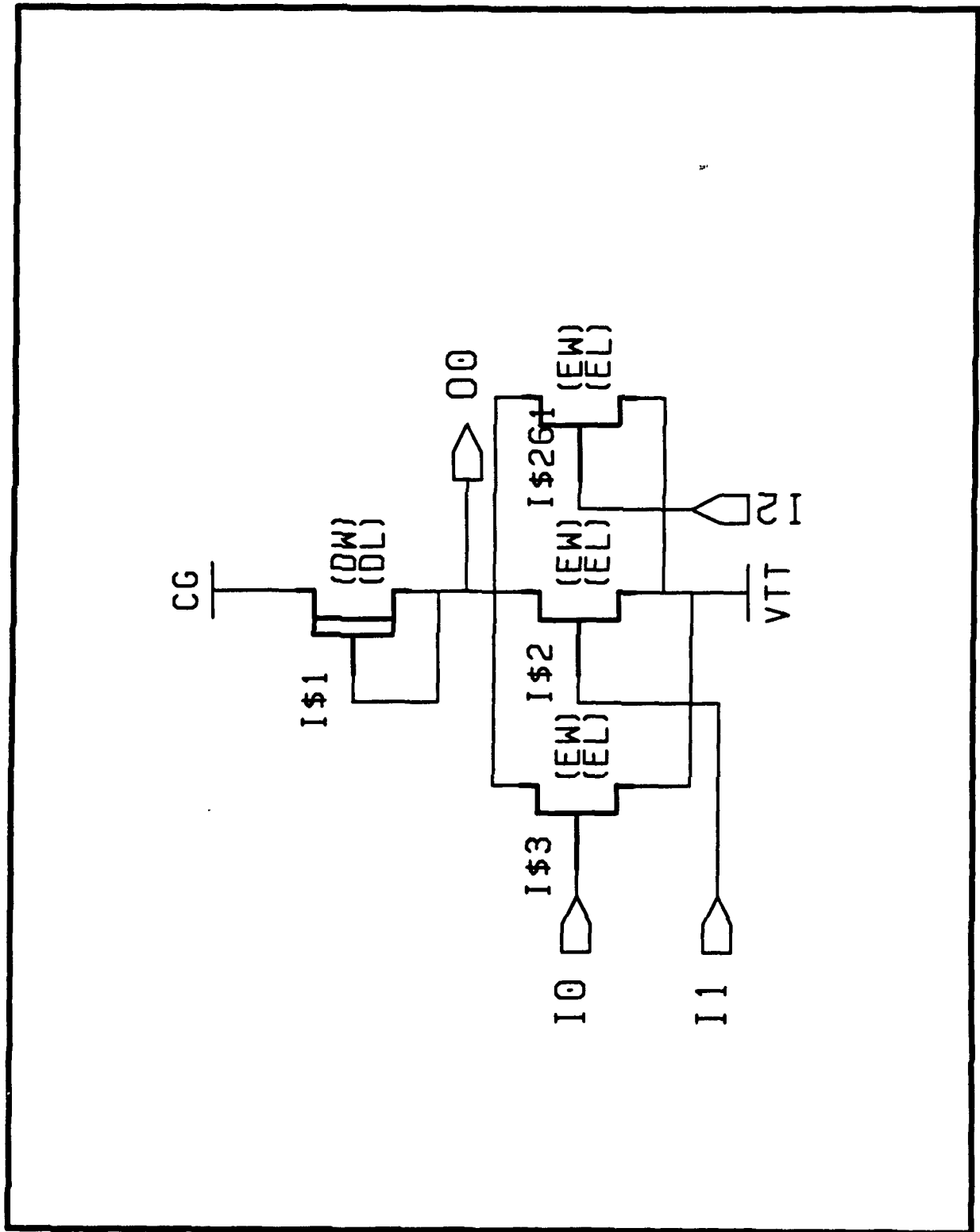


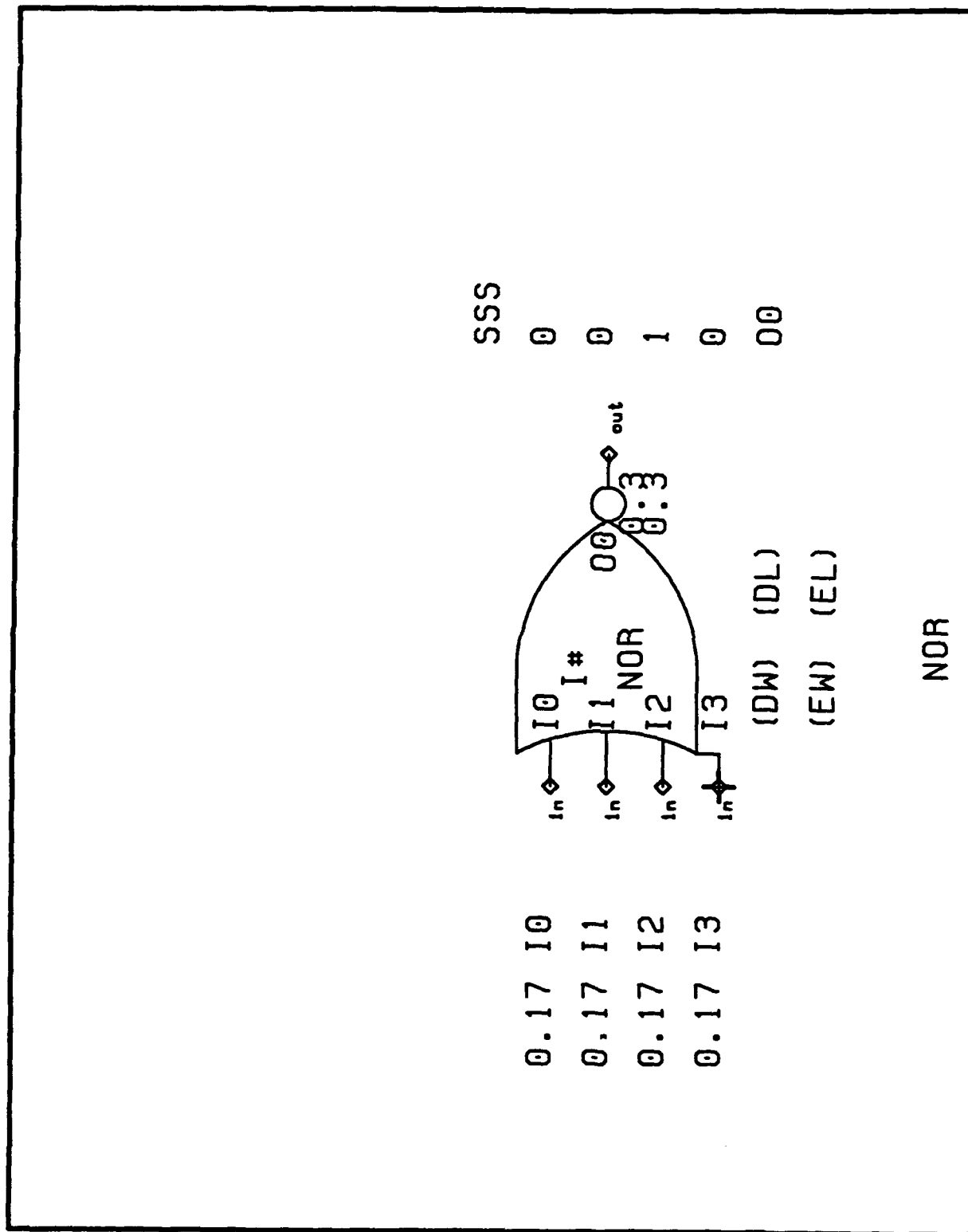


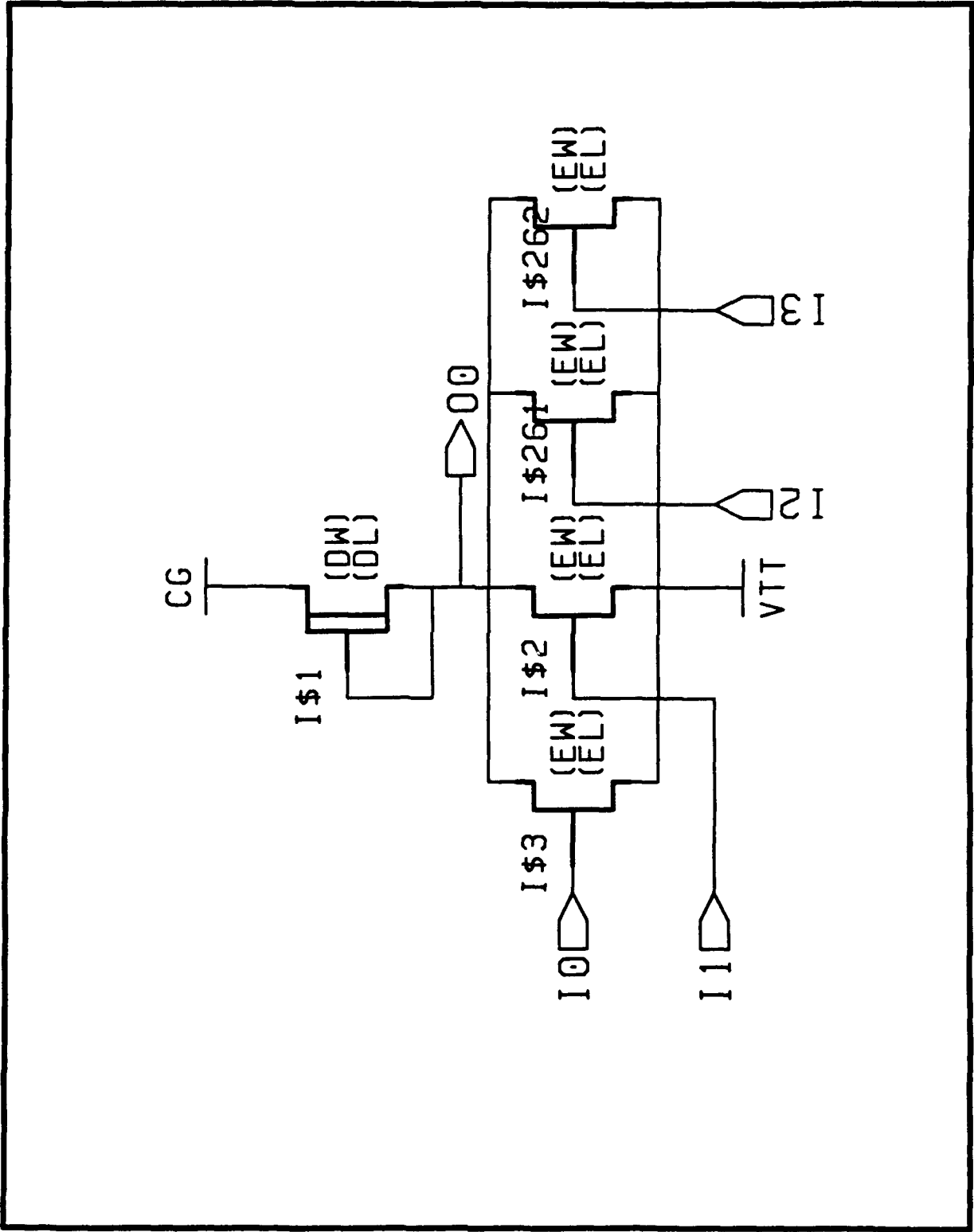


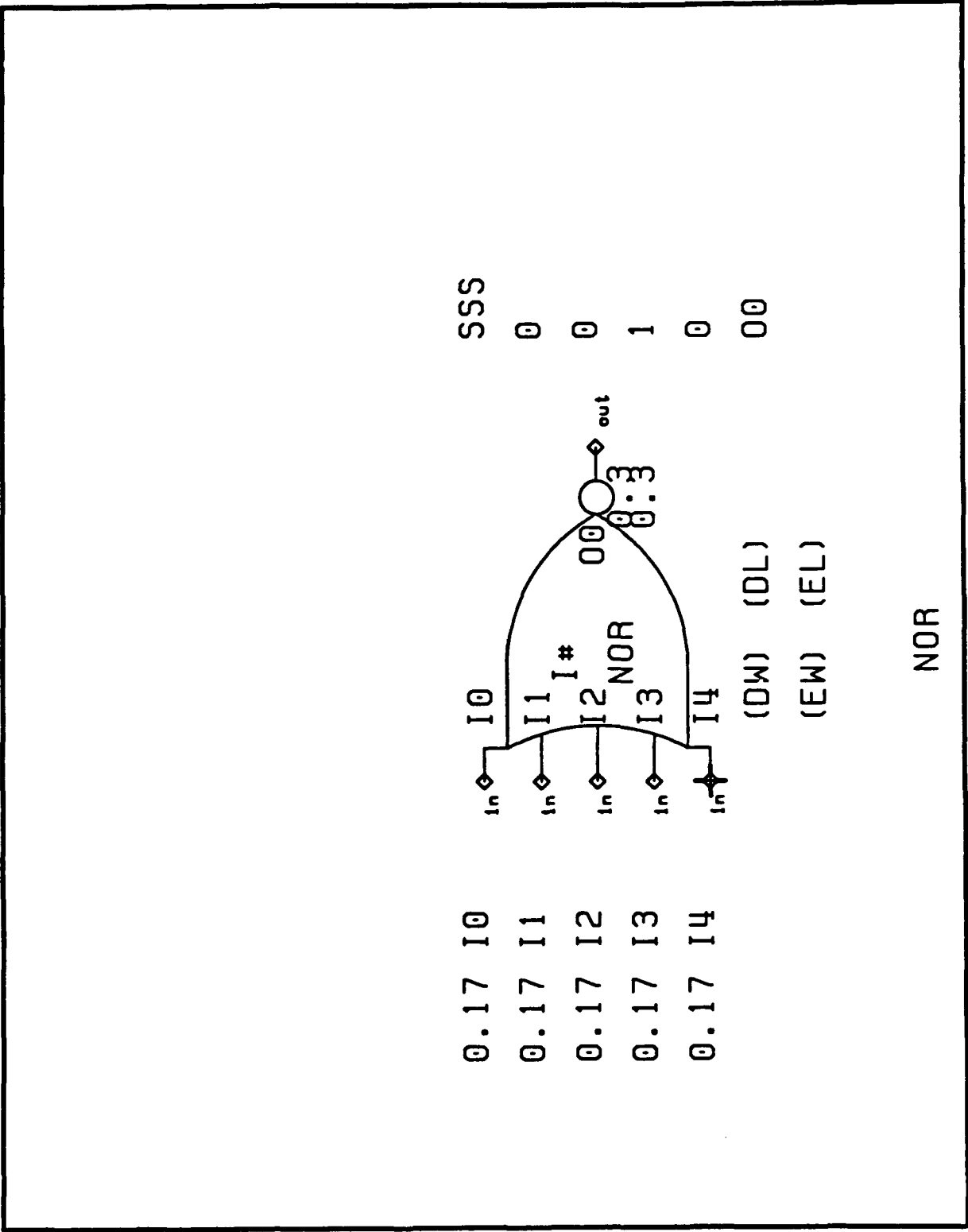


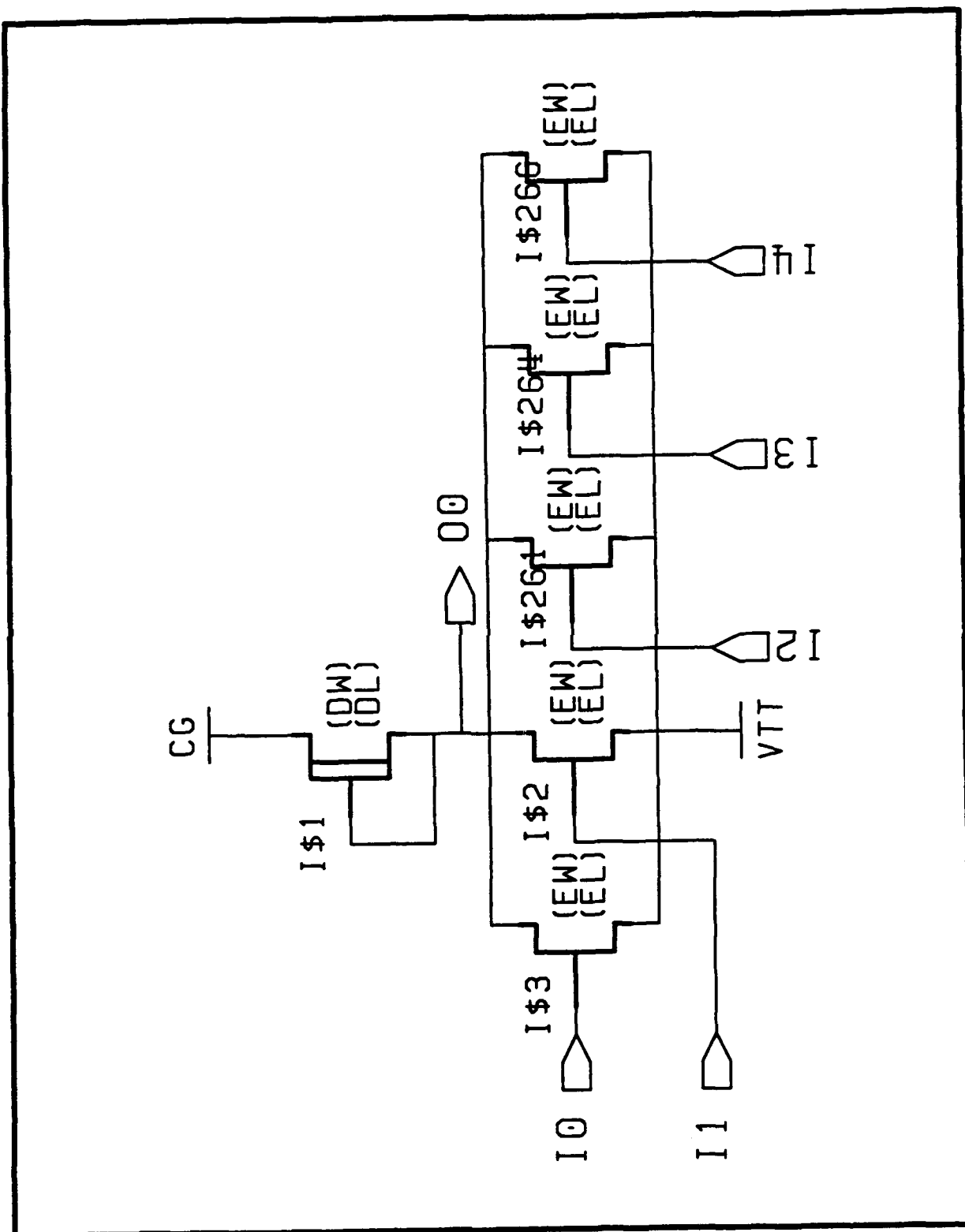




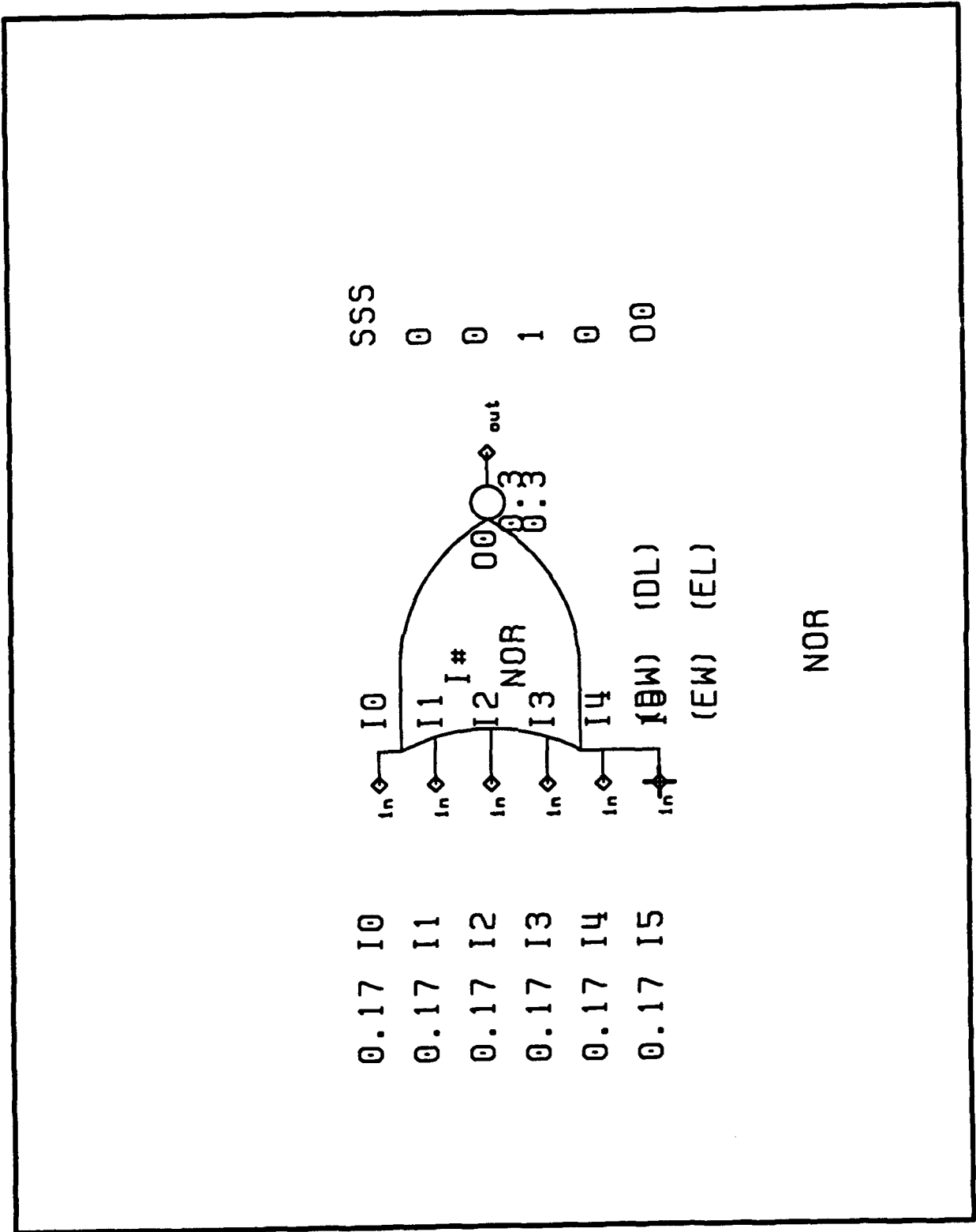


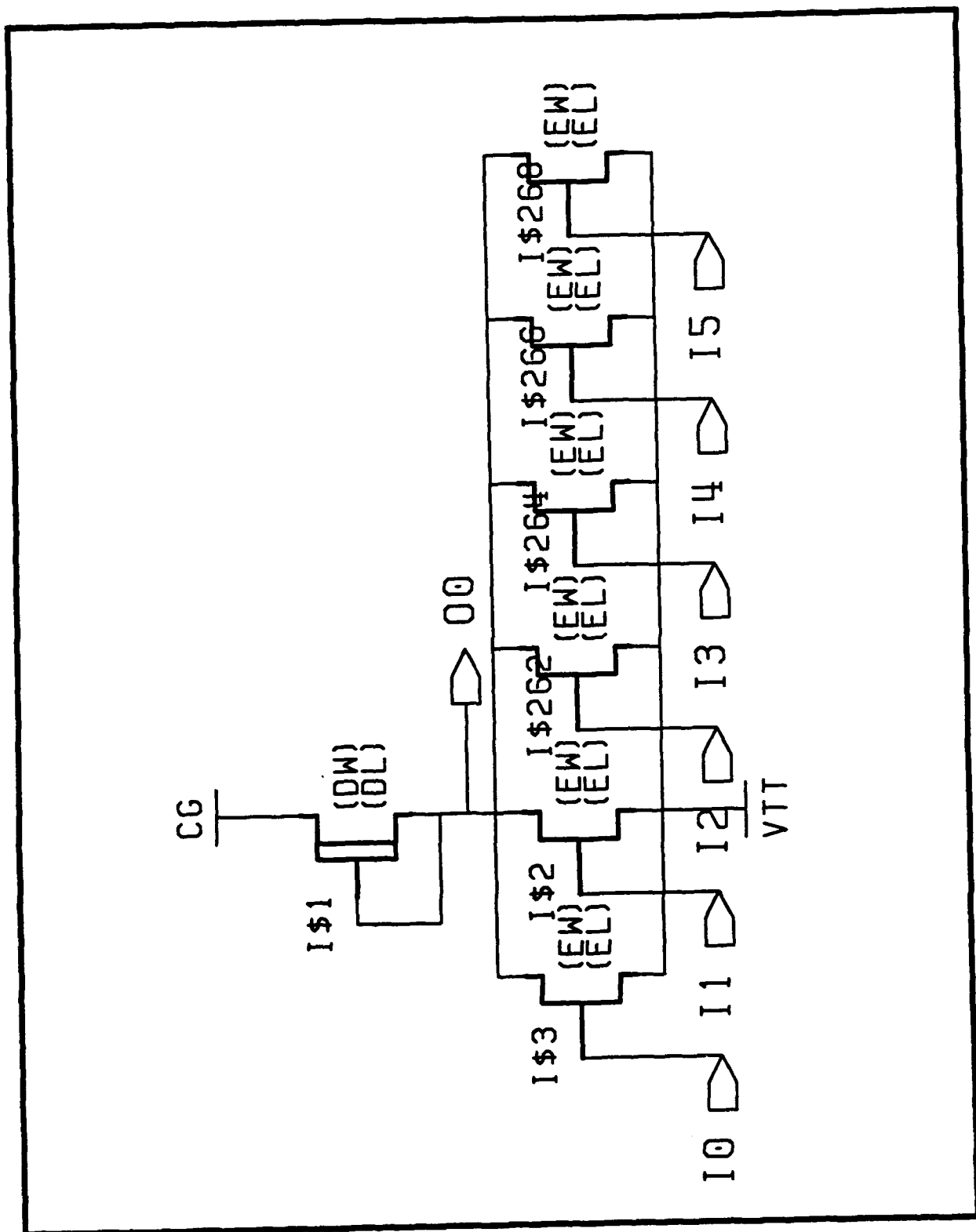






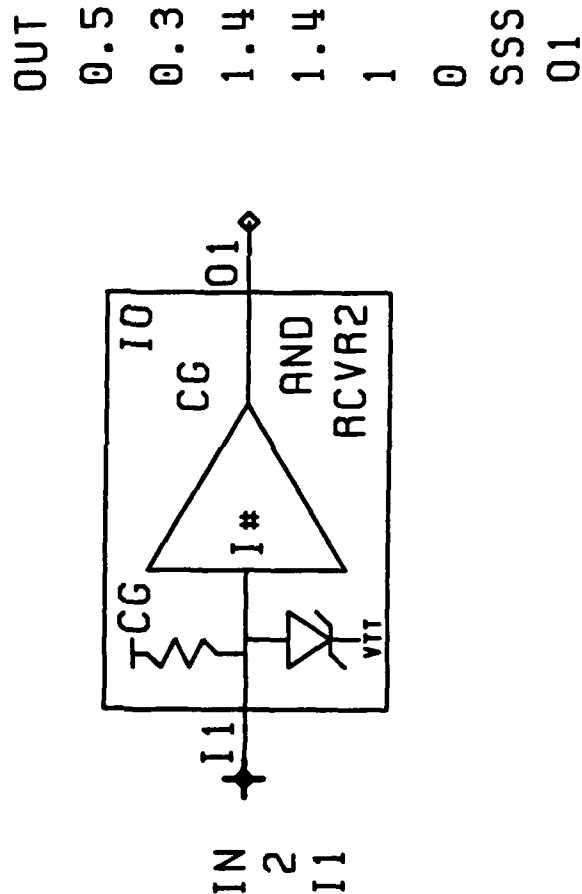


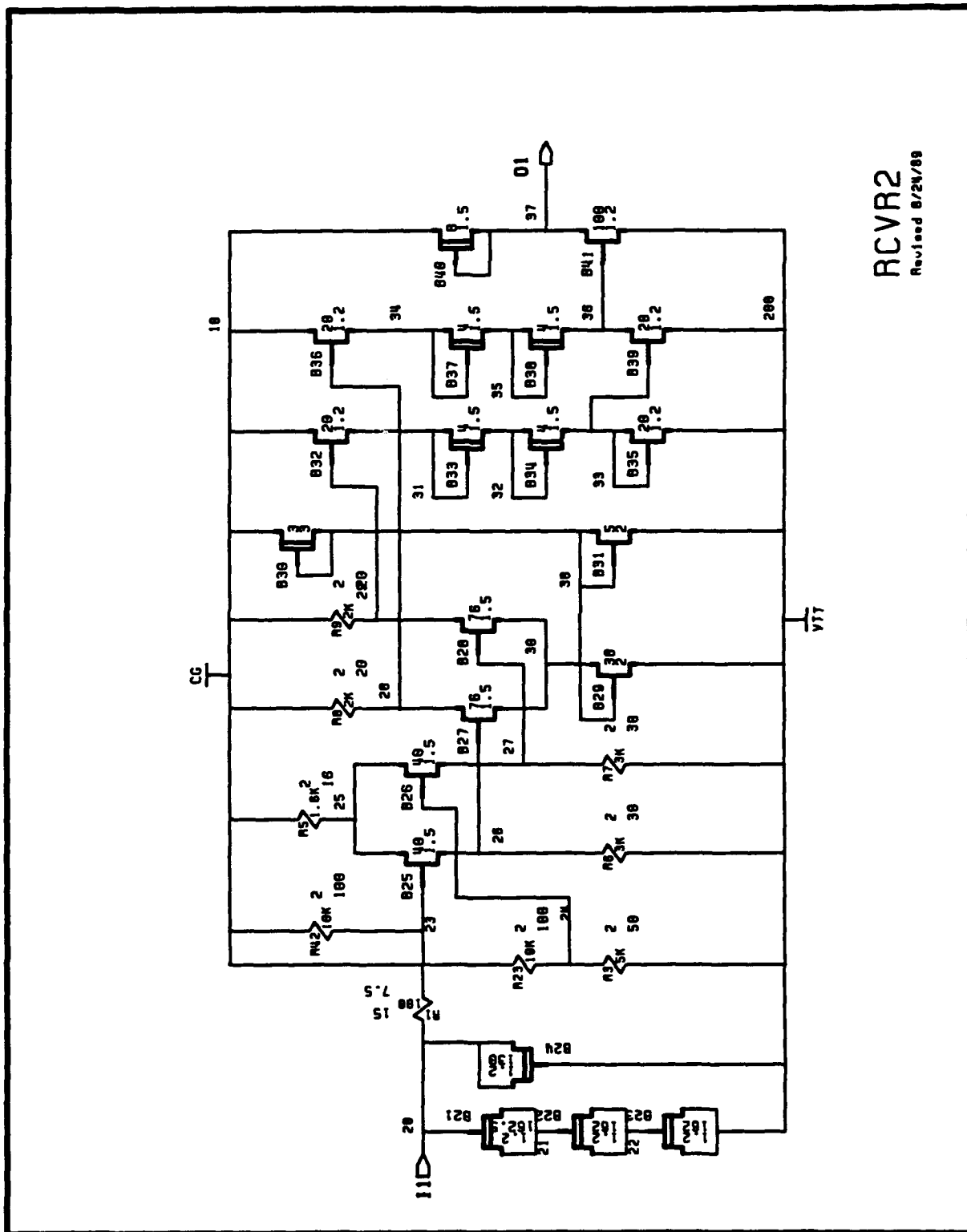




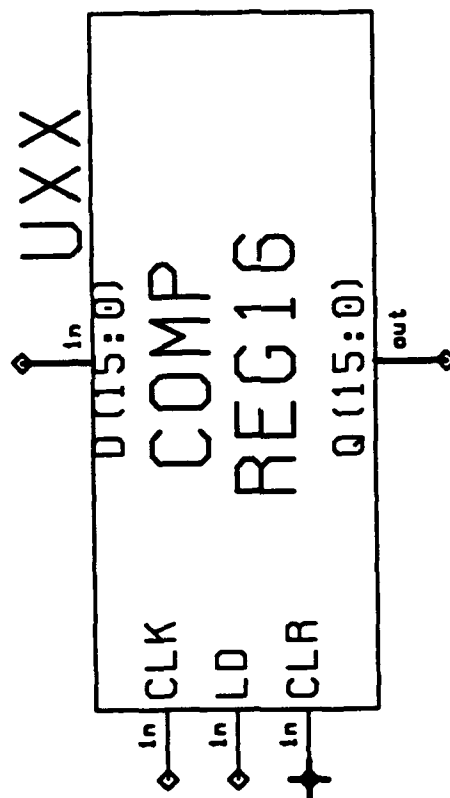
VITESSE GAAS CELL LIBRARY  
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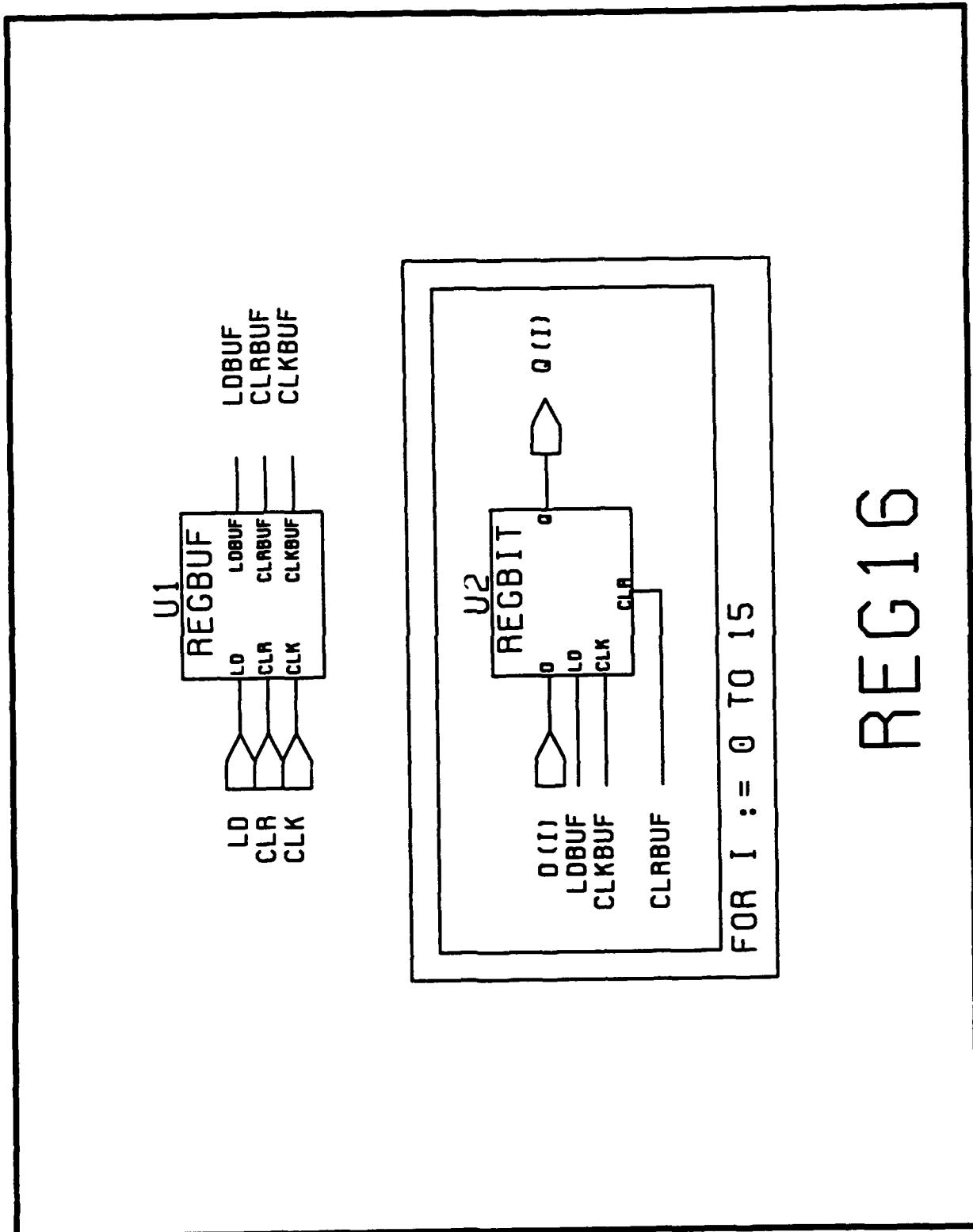
NAME: RCVR2  
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD

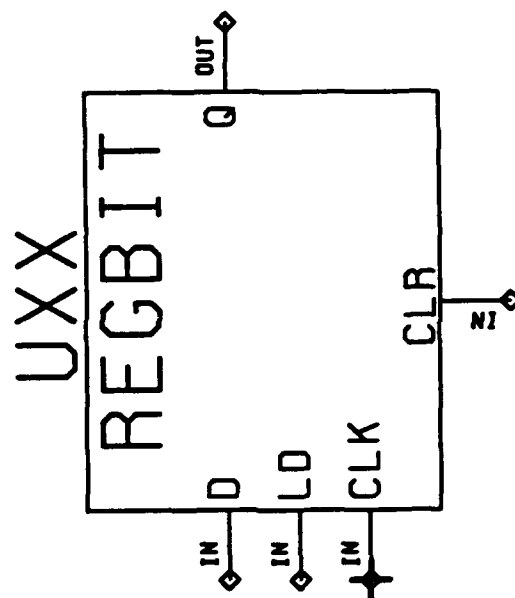


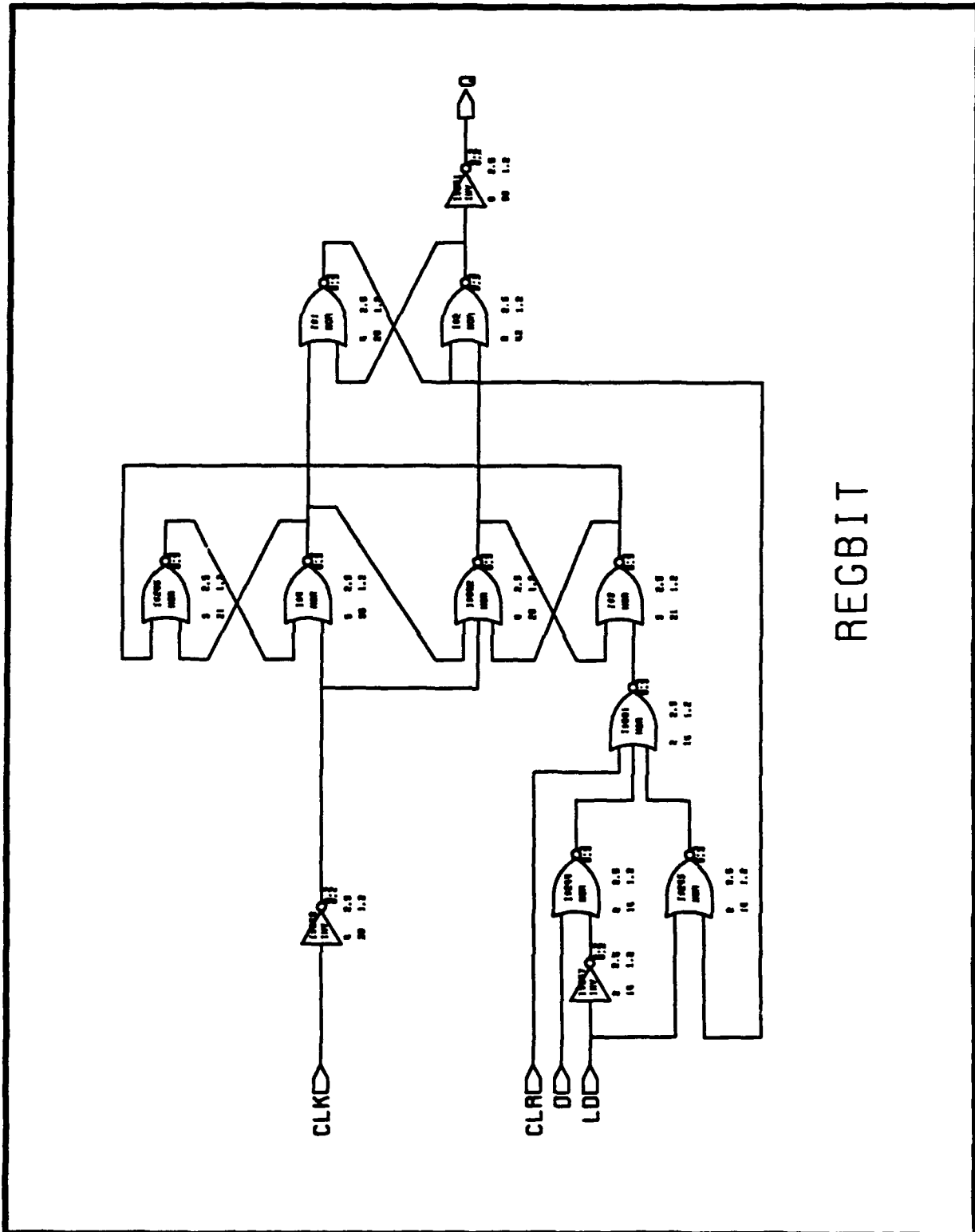


RCVR2  
Revised 8/24/89

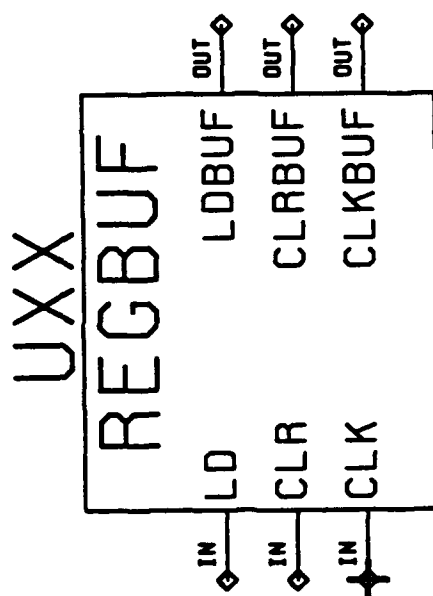


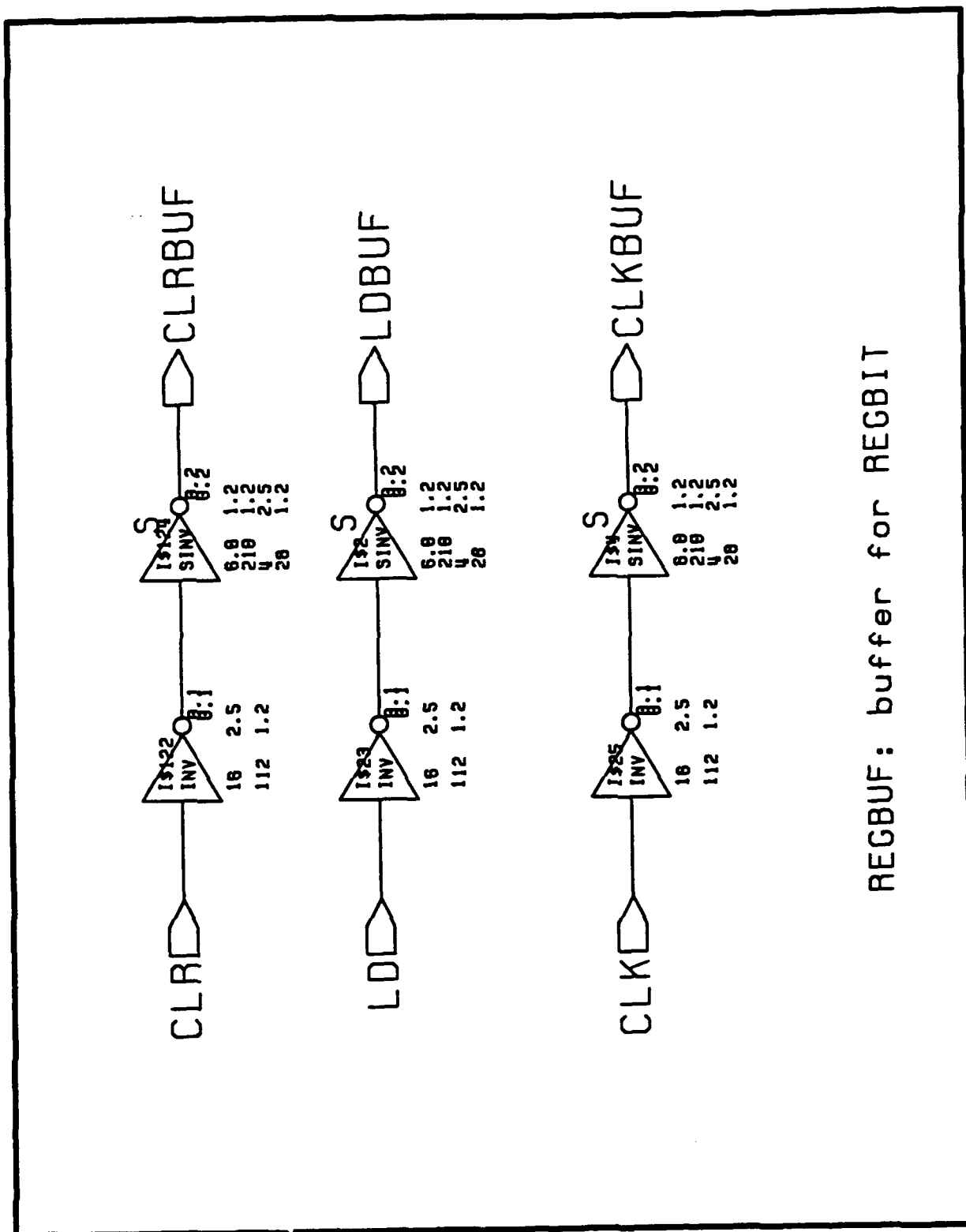


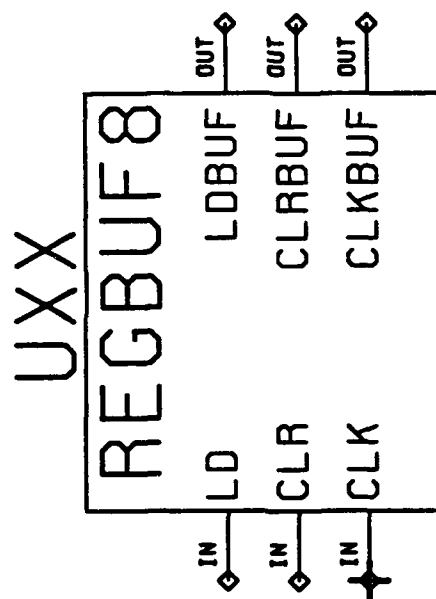


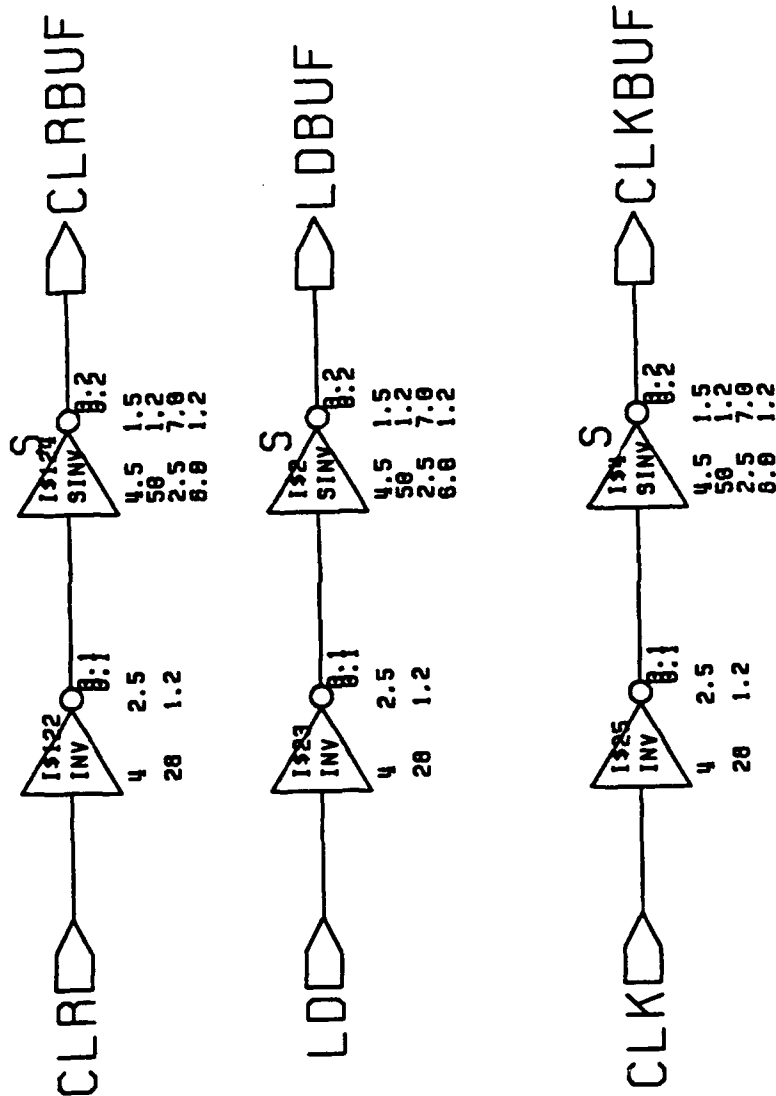




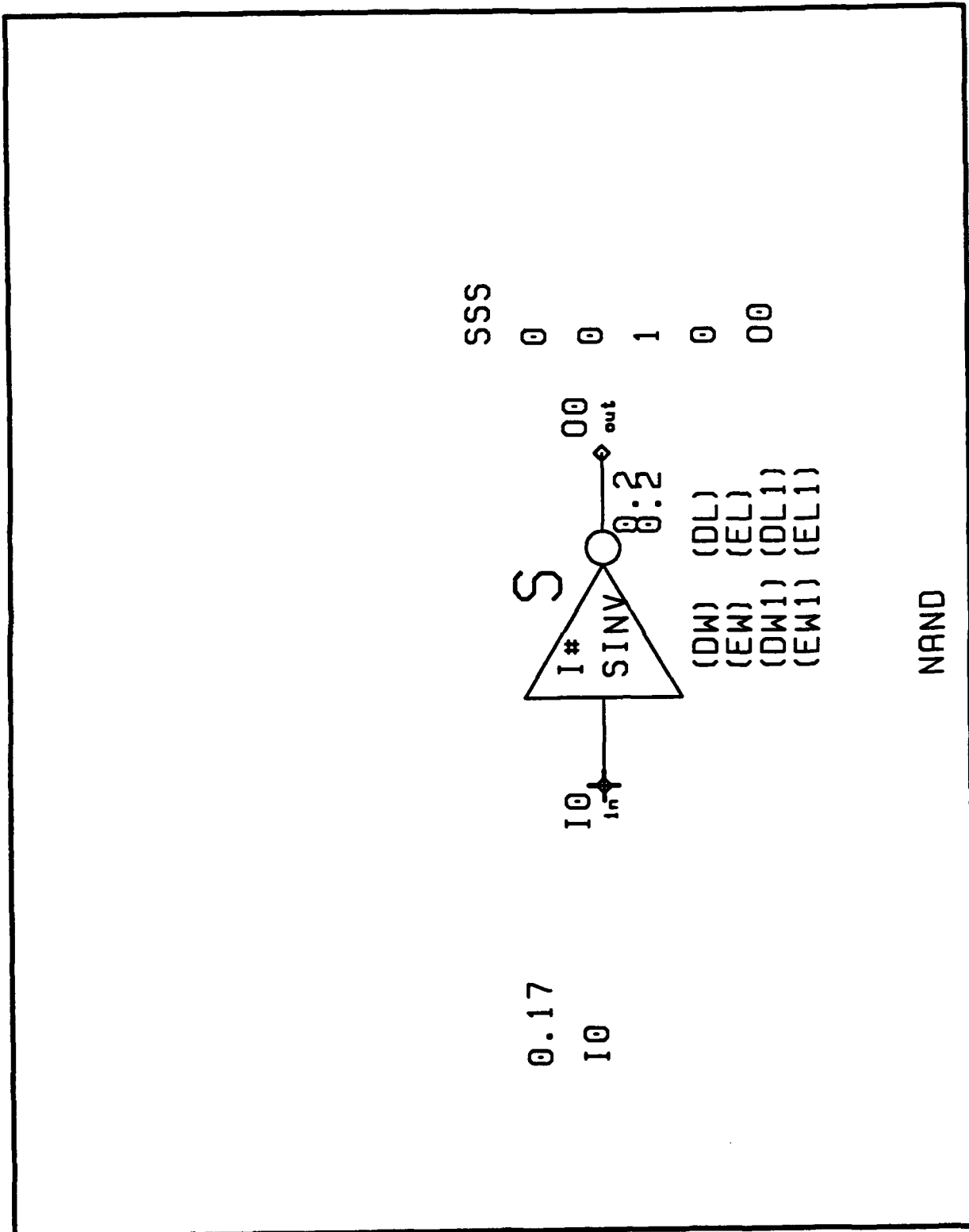


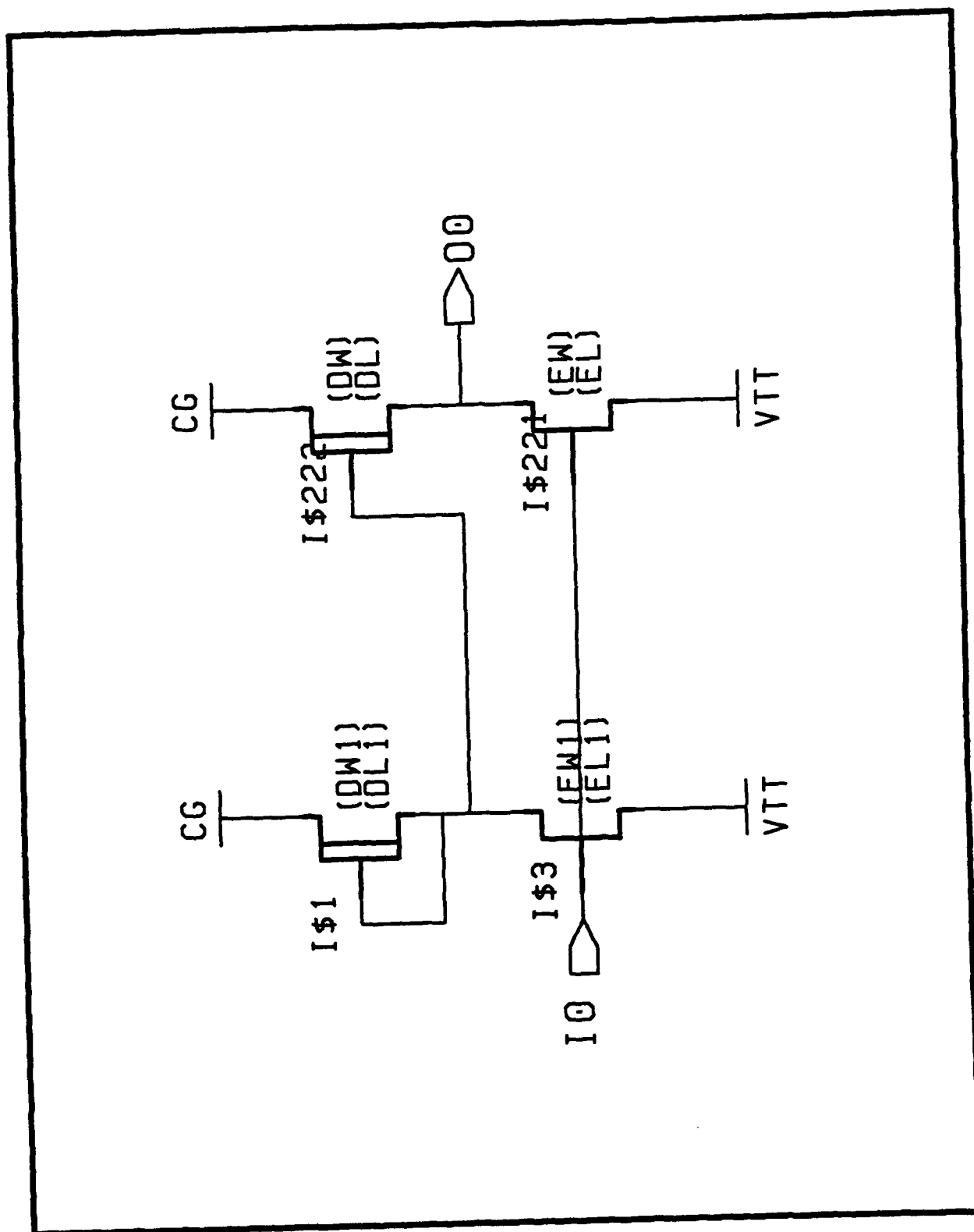


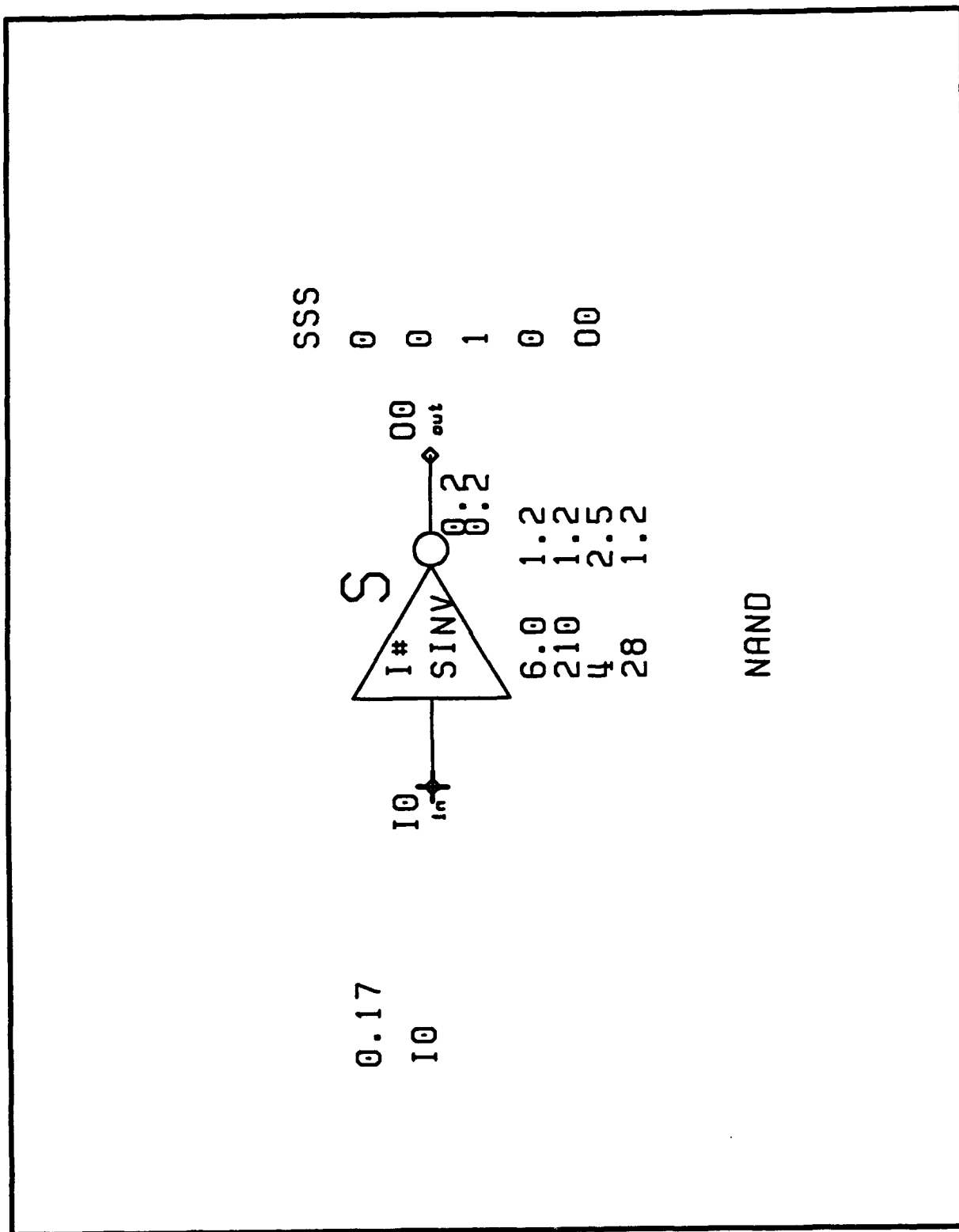


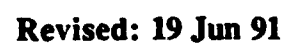


REGBUF8: buffer for 8 REGBIT's

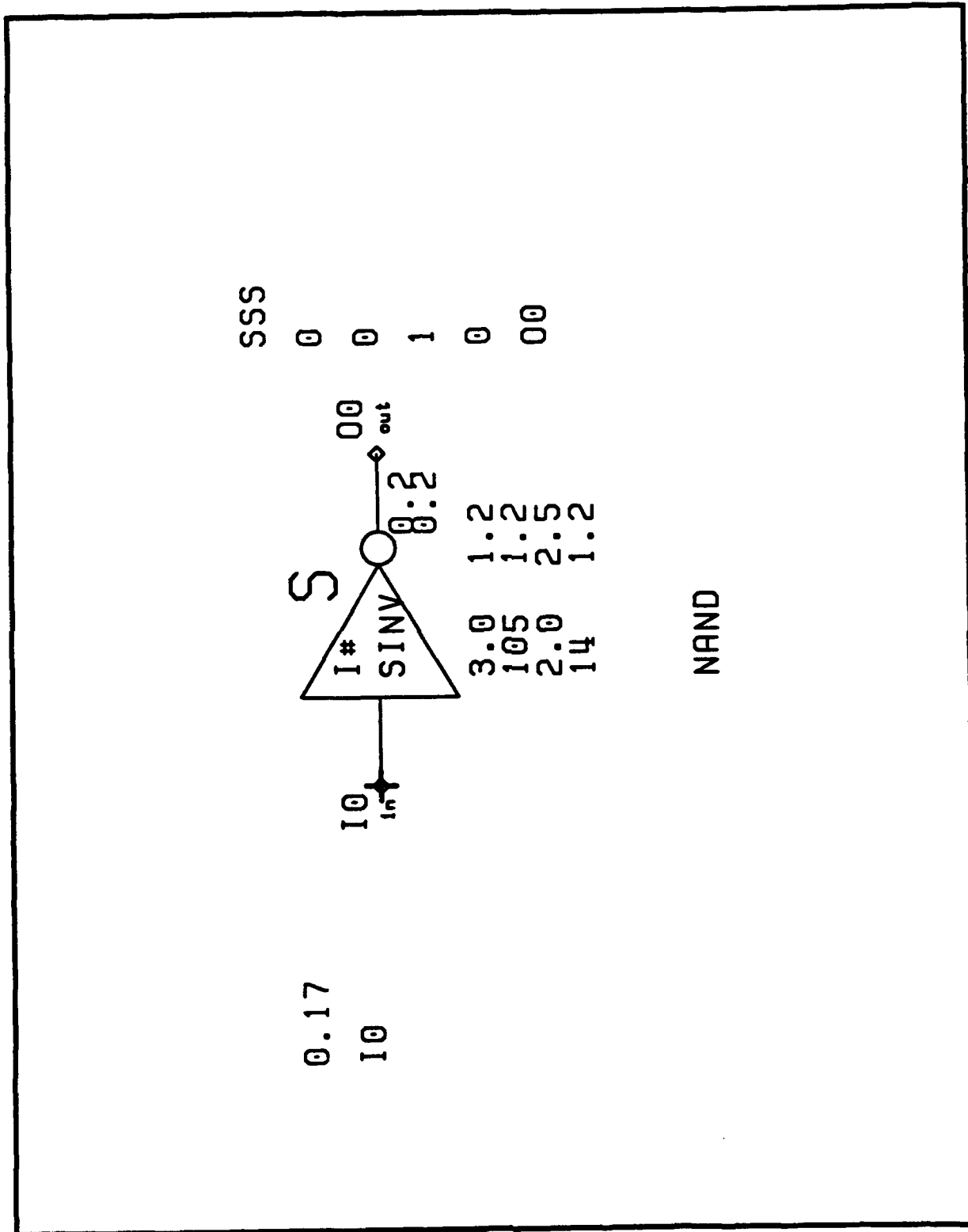


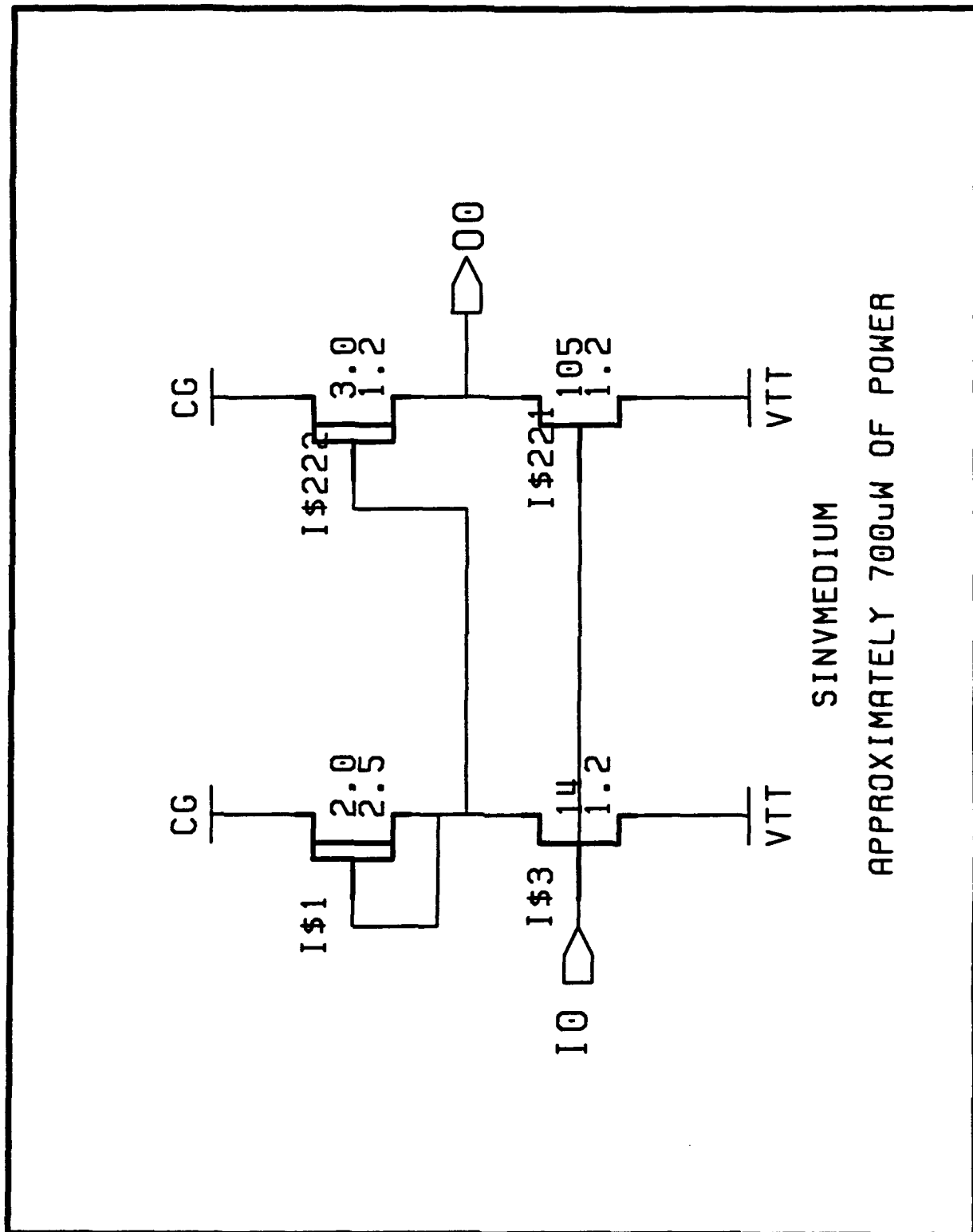


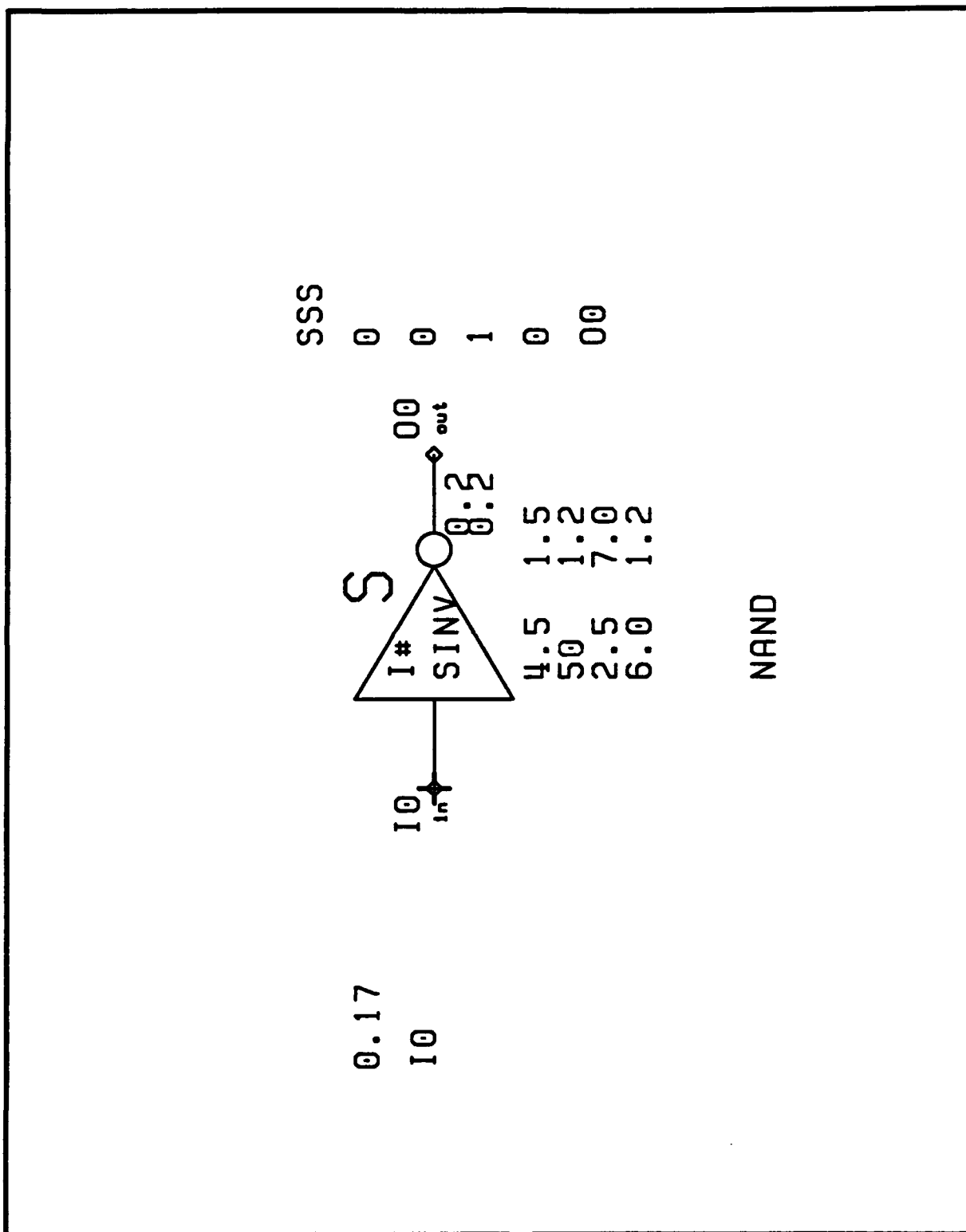


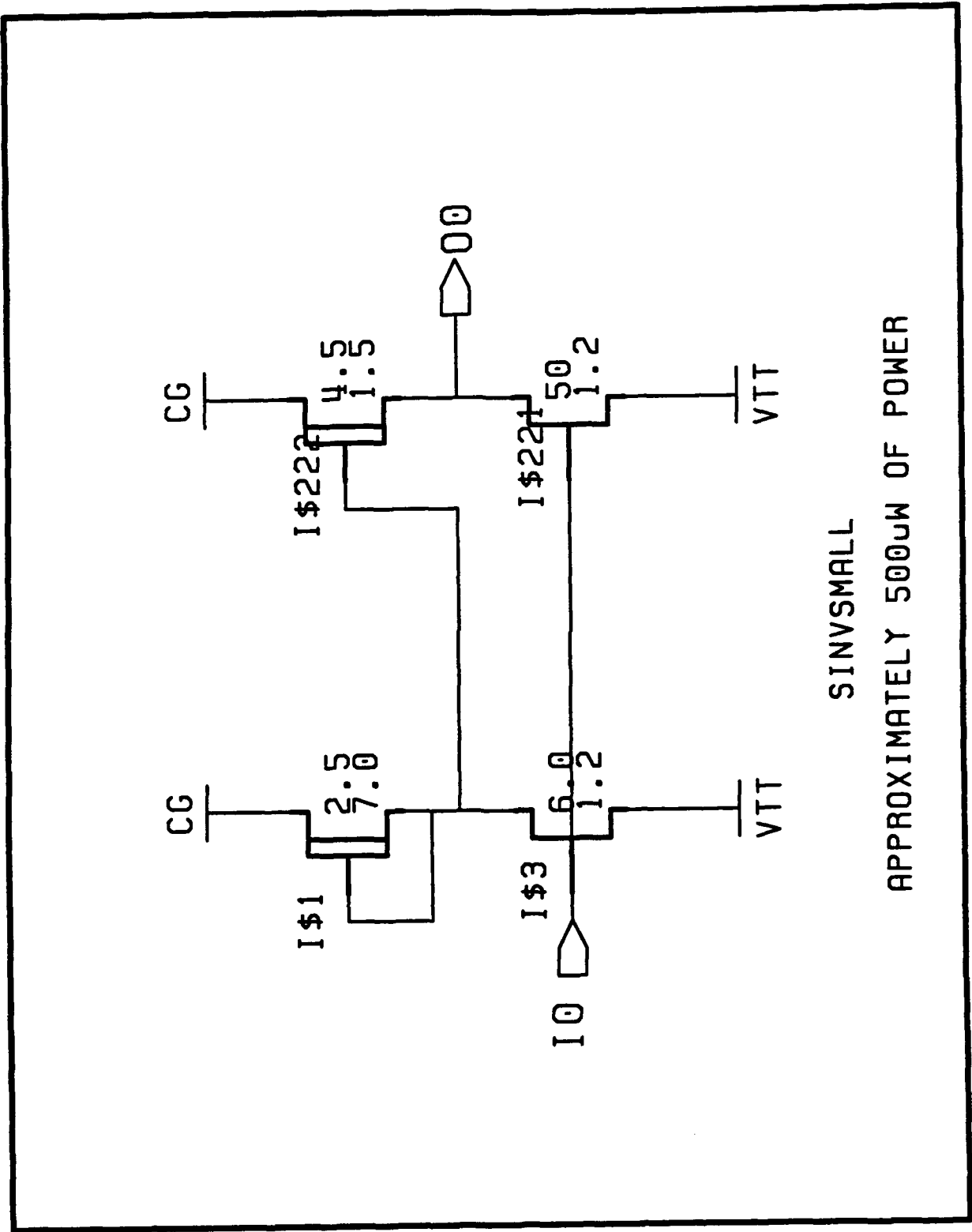


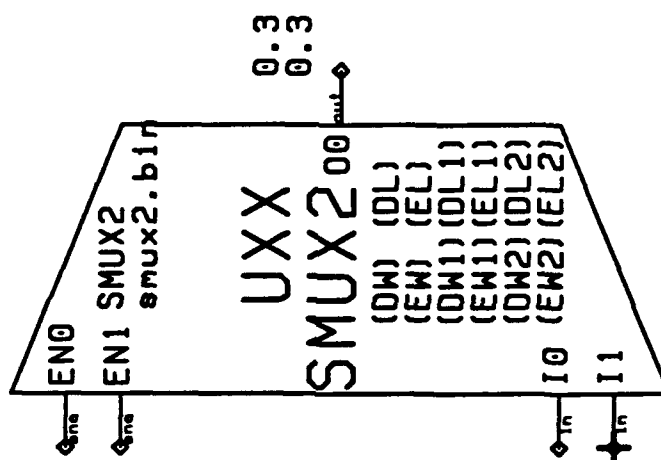


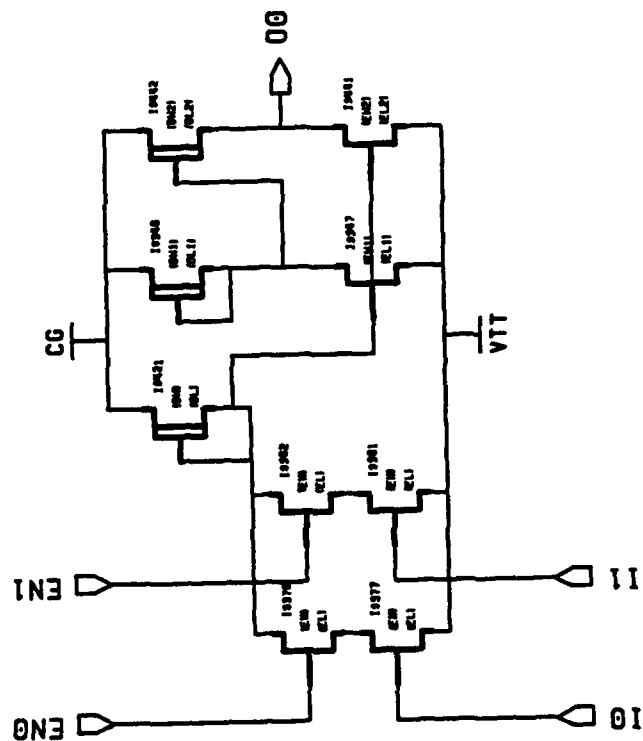


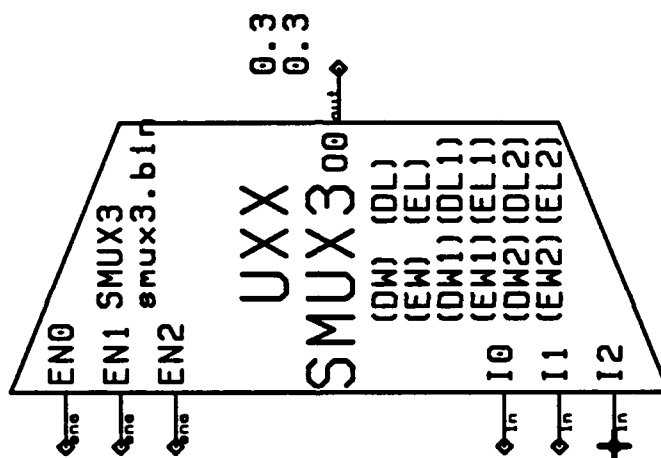


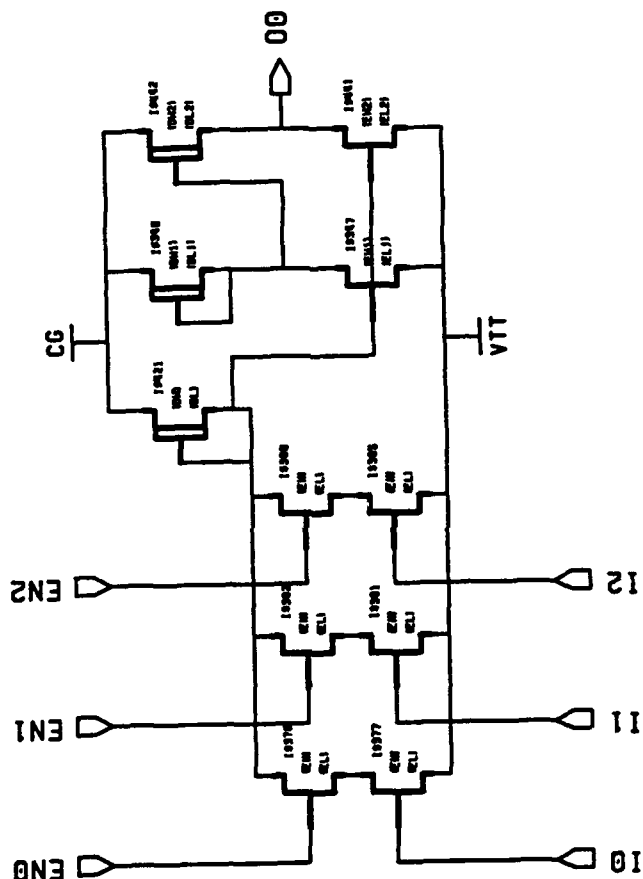




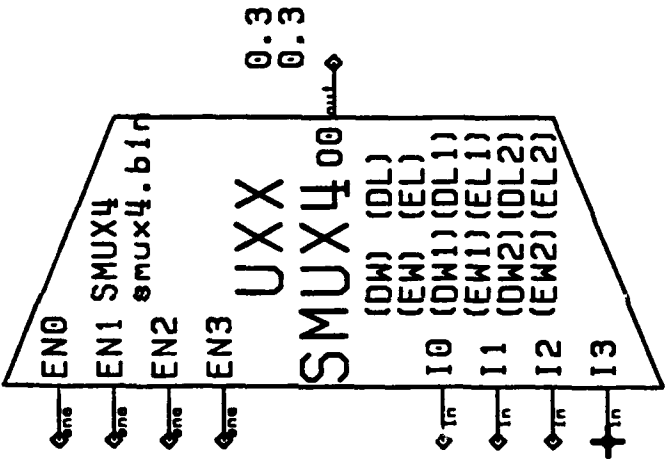


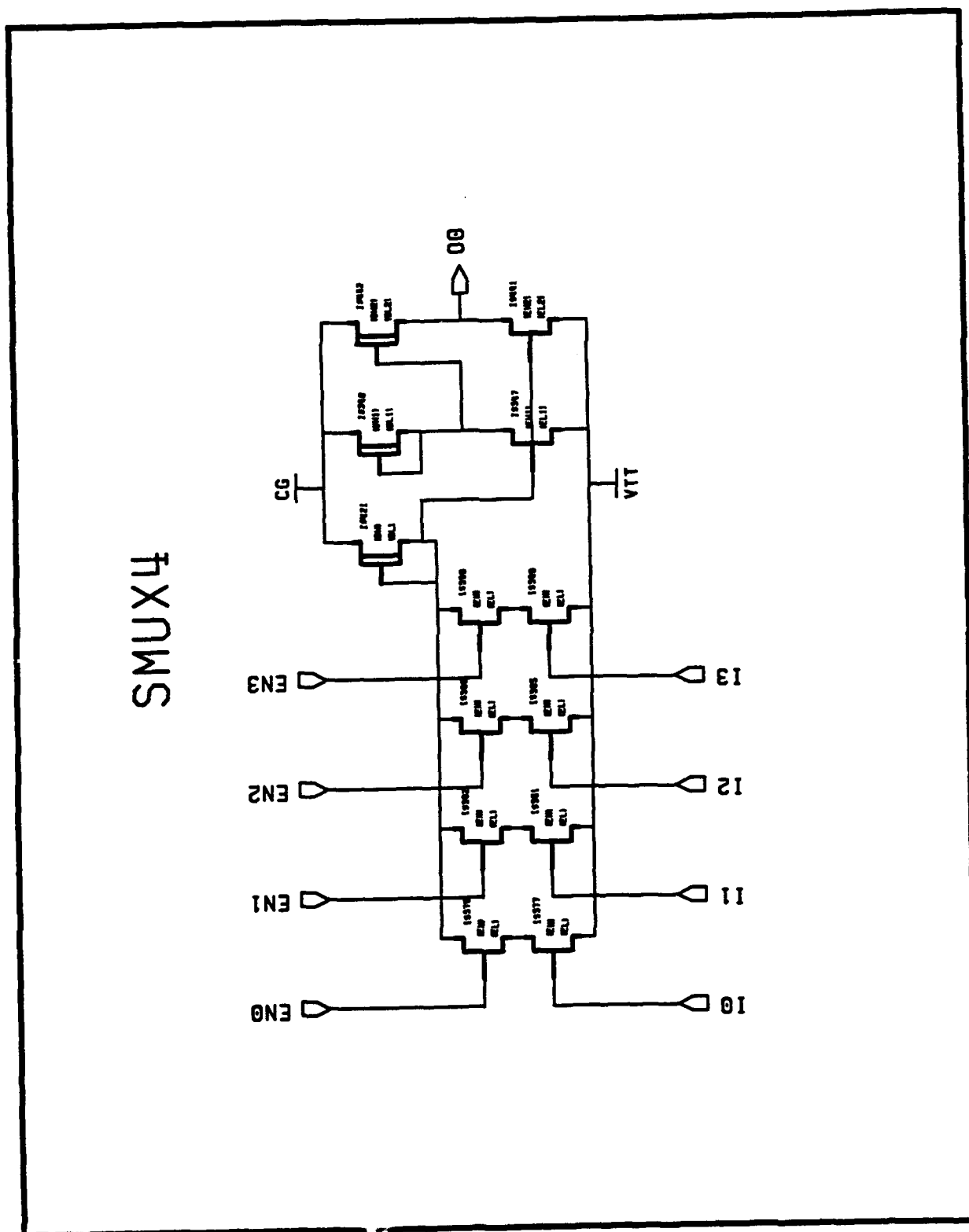


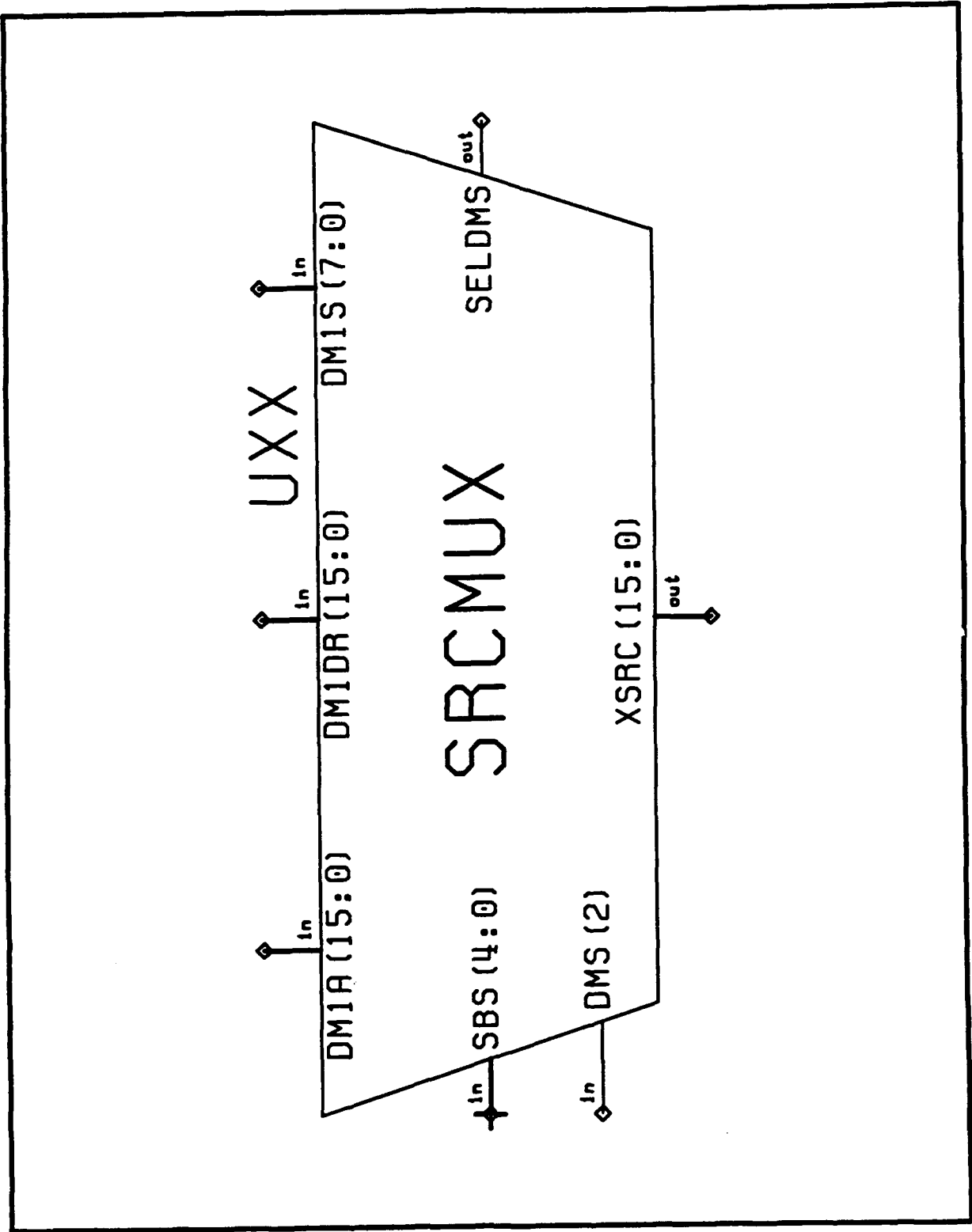


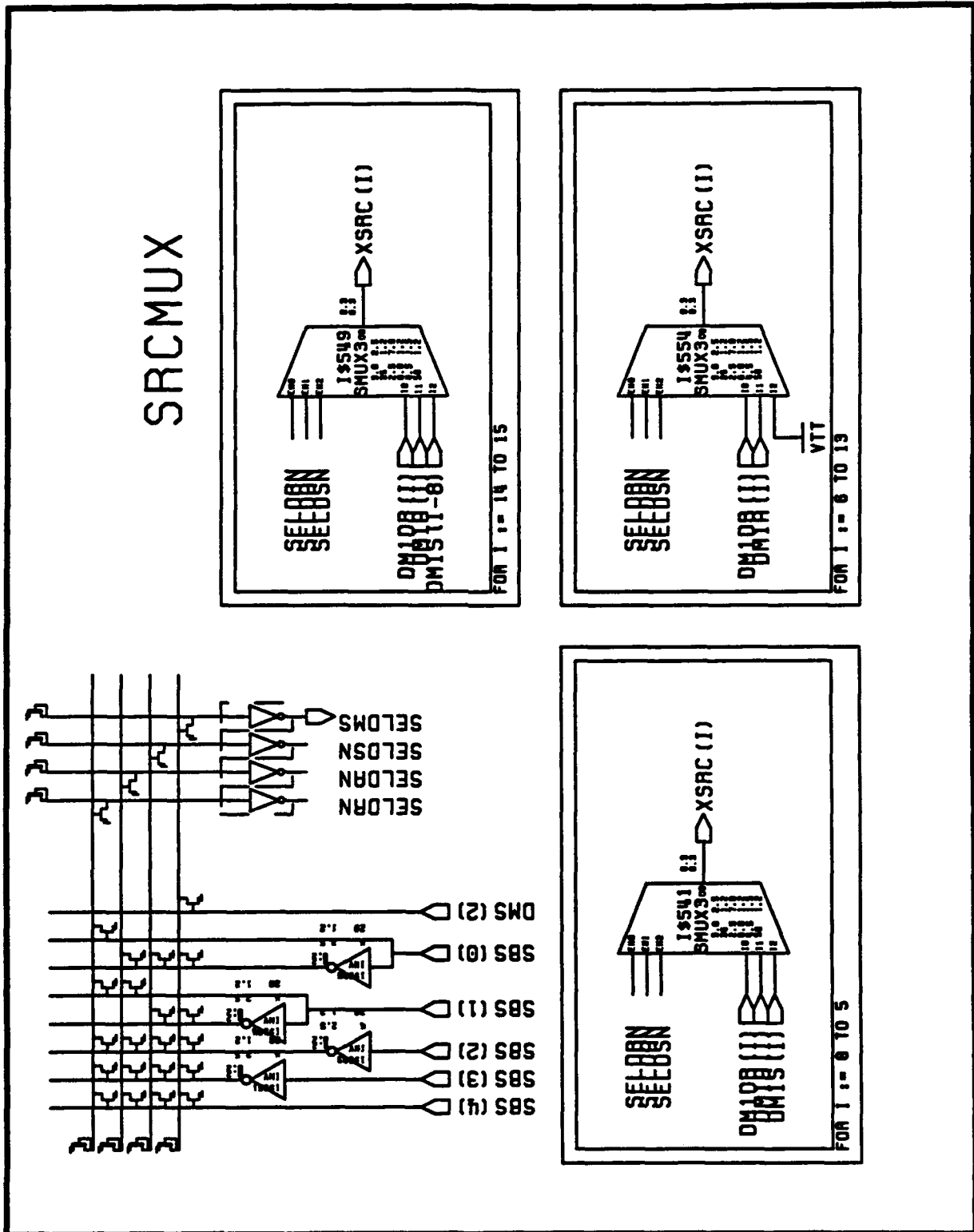


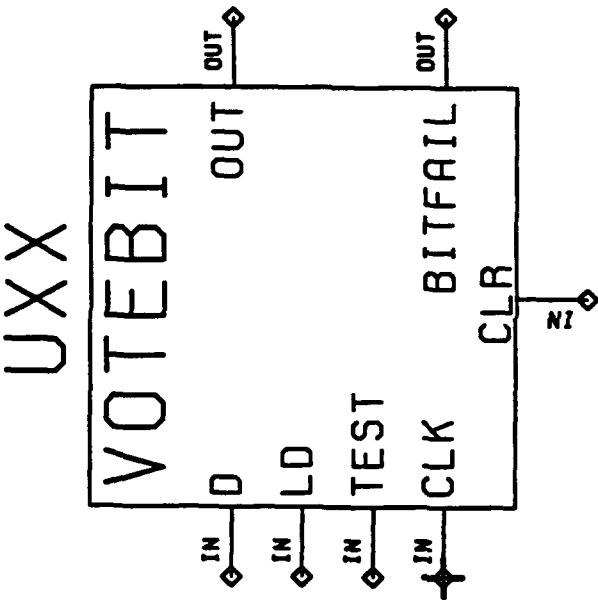


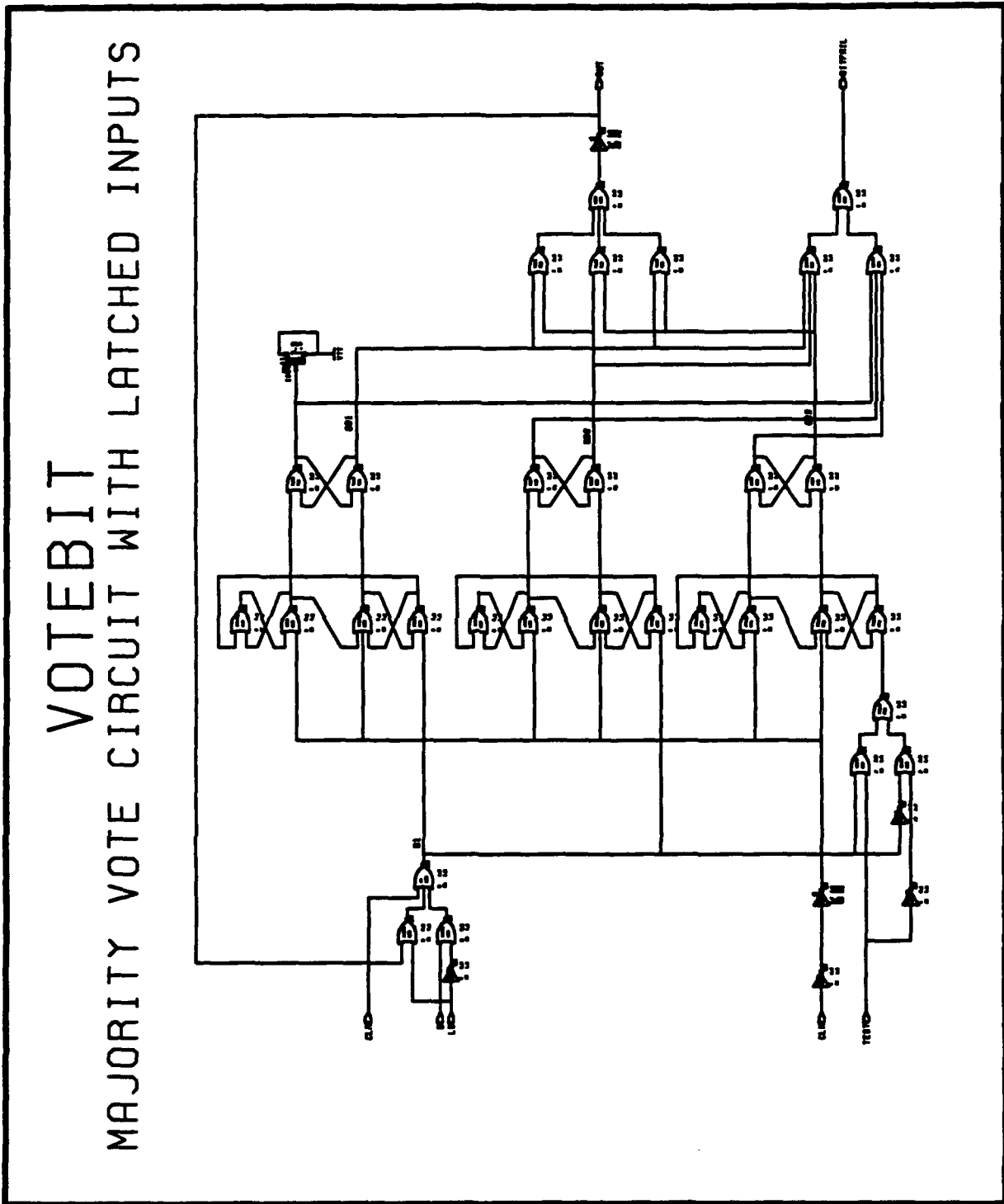


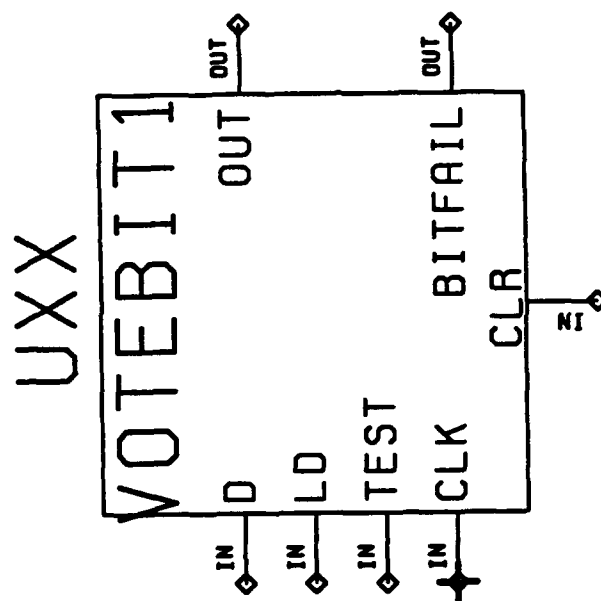




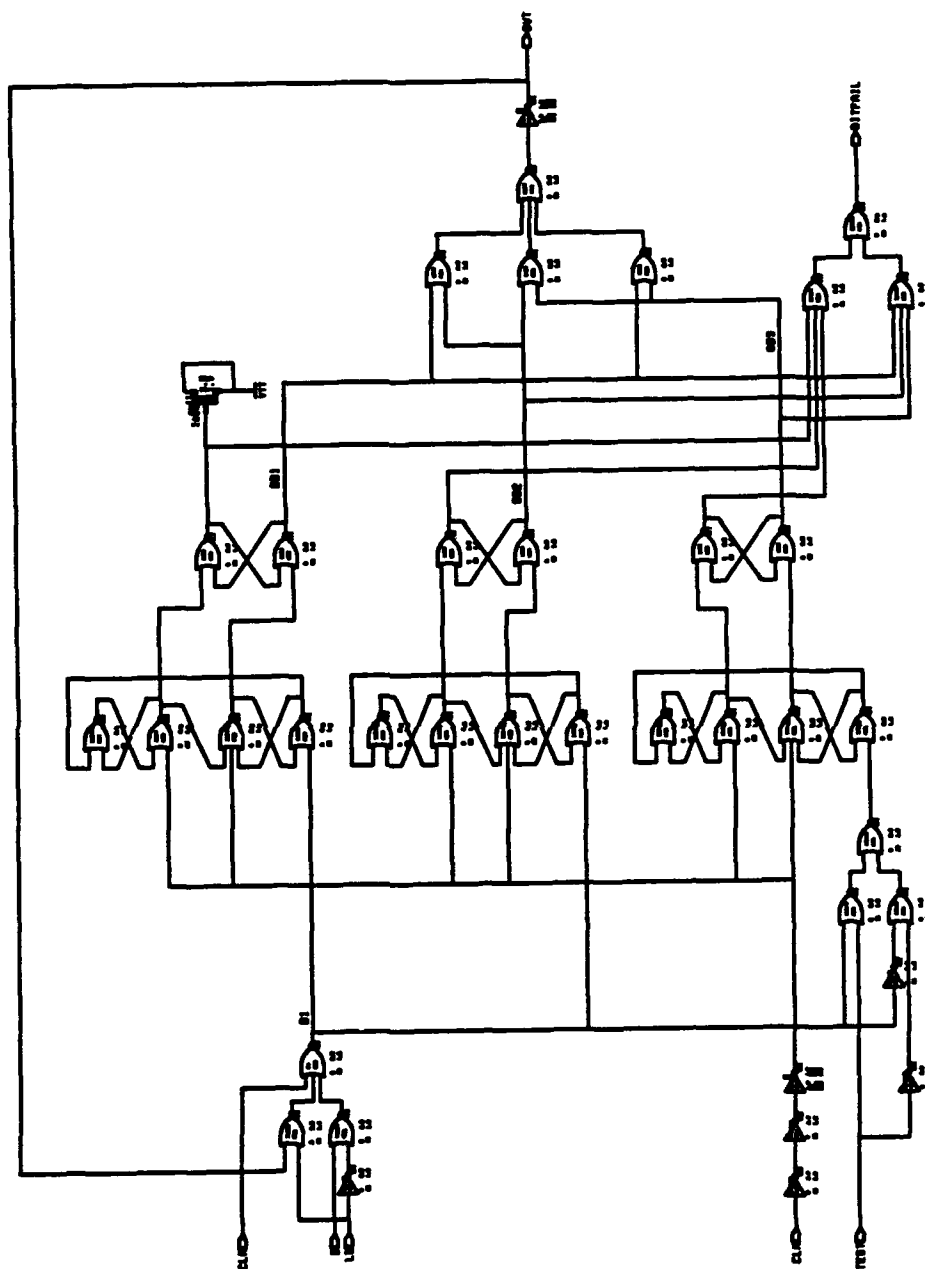




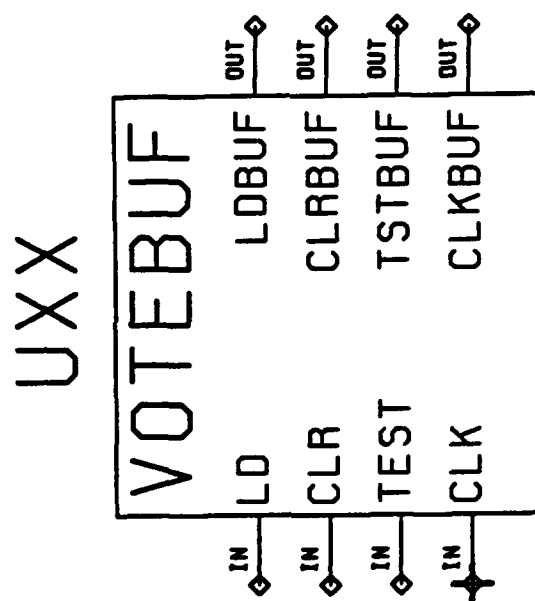


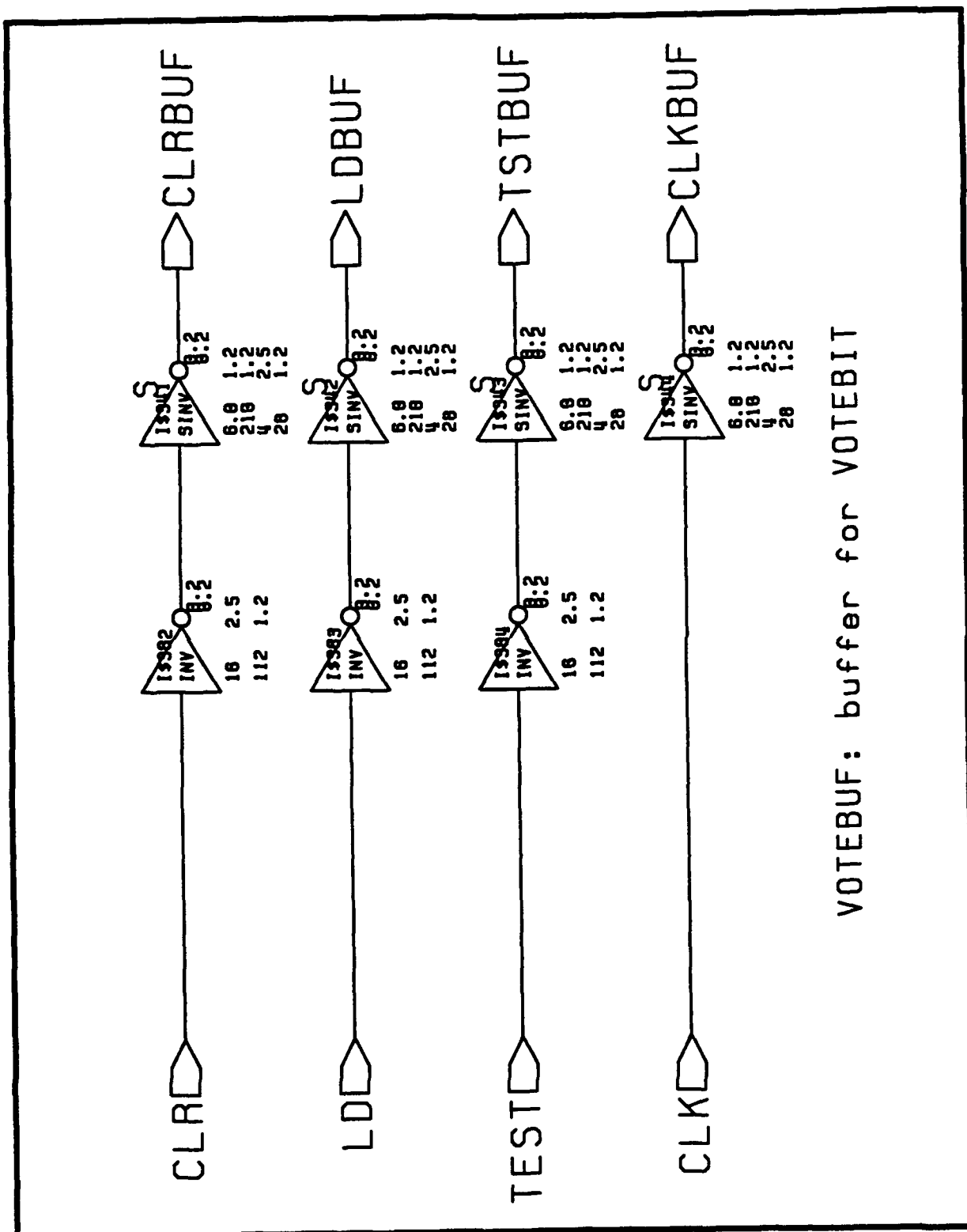


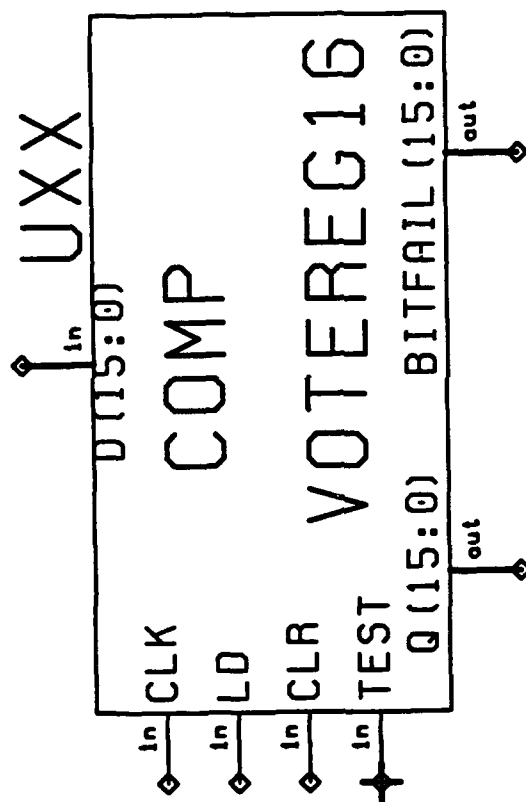
VOTE BIT 1  
MAJORITY VOTE CIRCUIT WITH LATCHED INPUTS

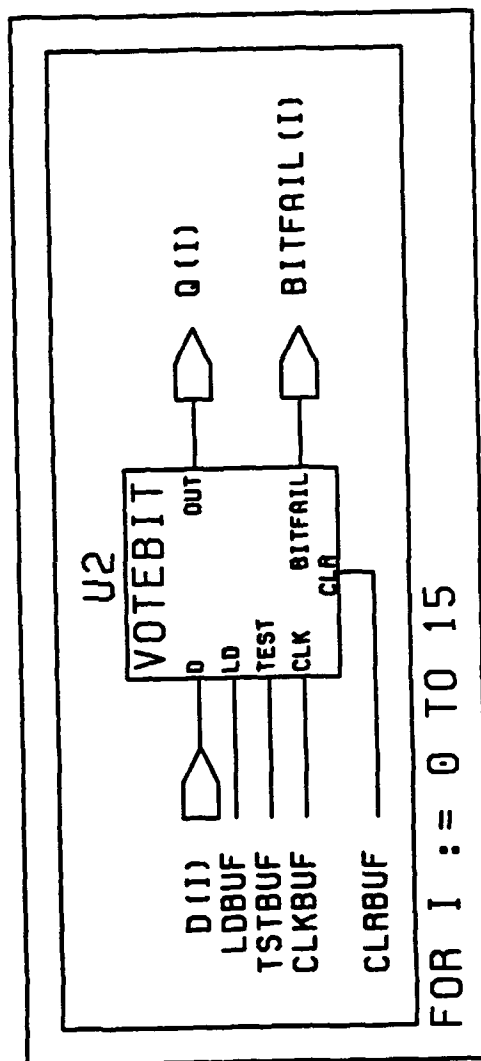
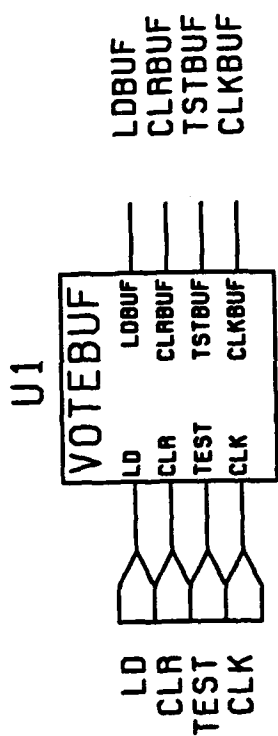




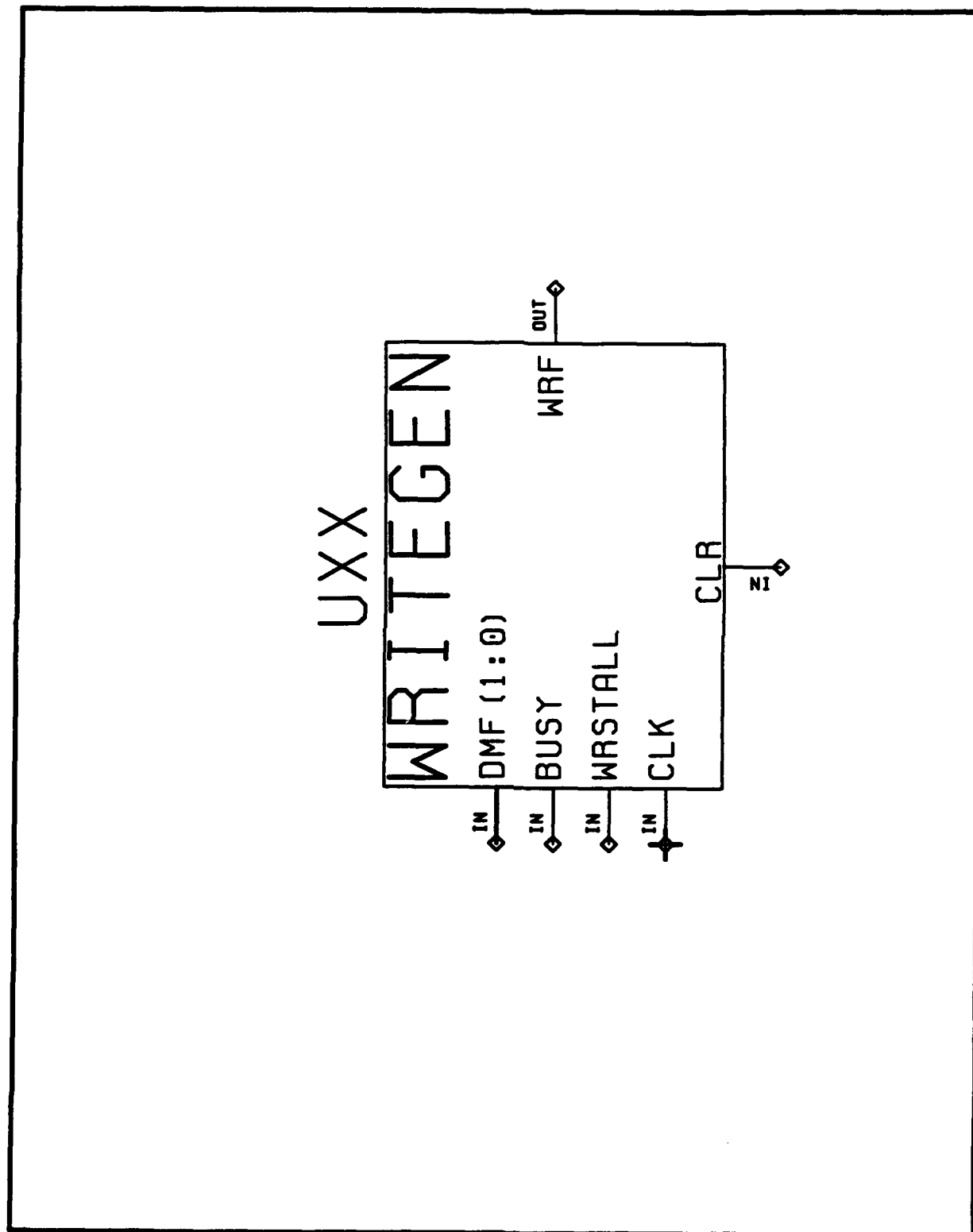


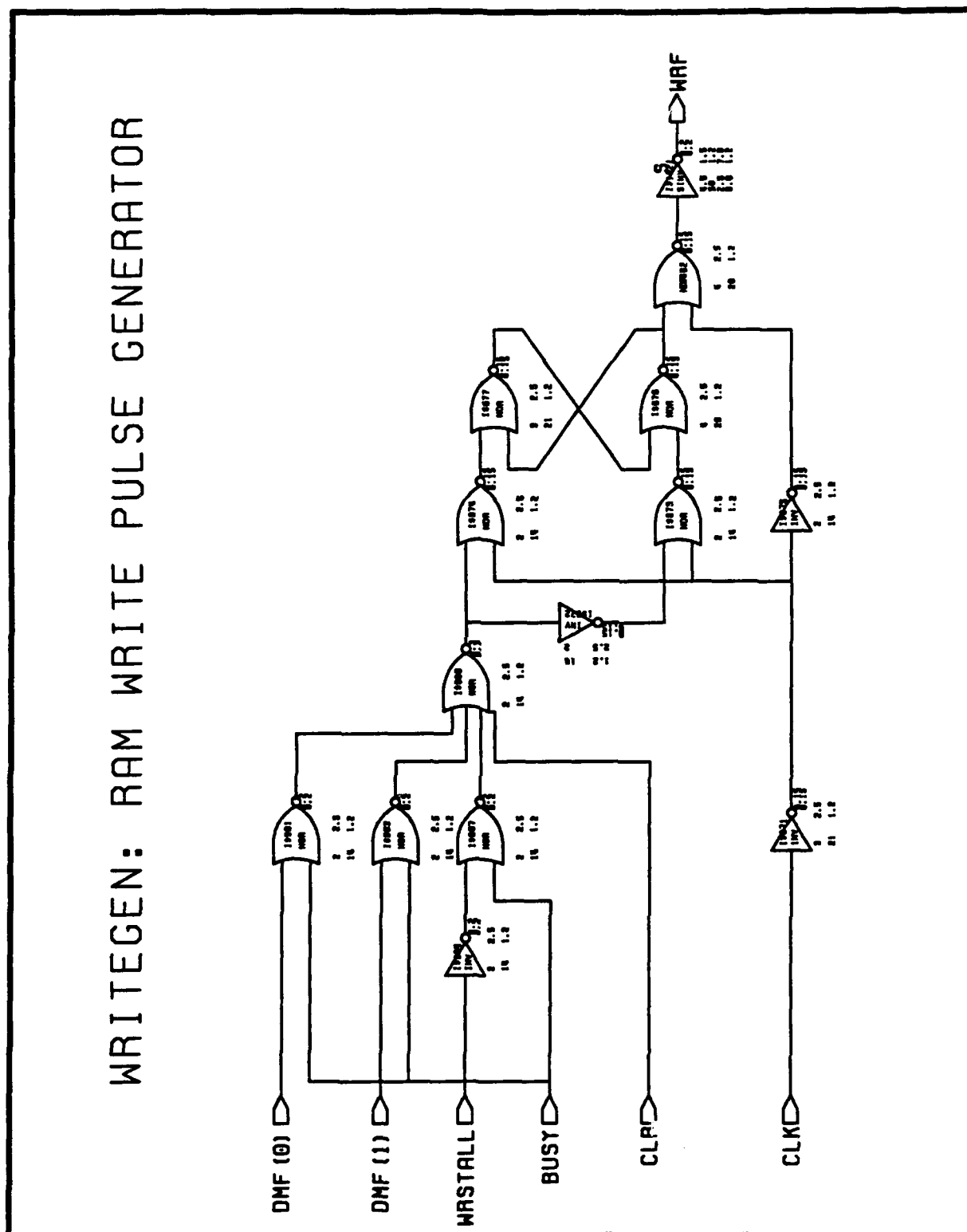


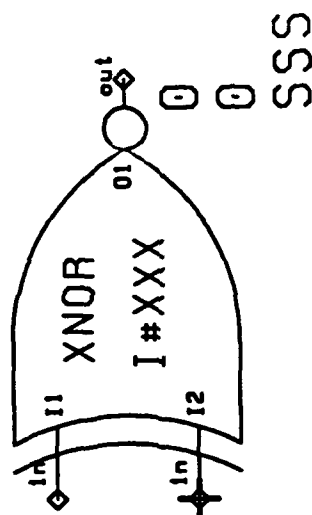


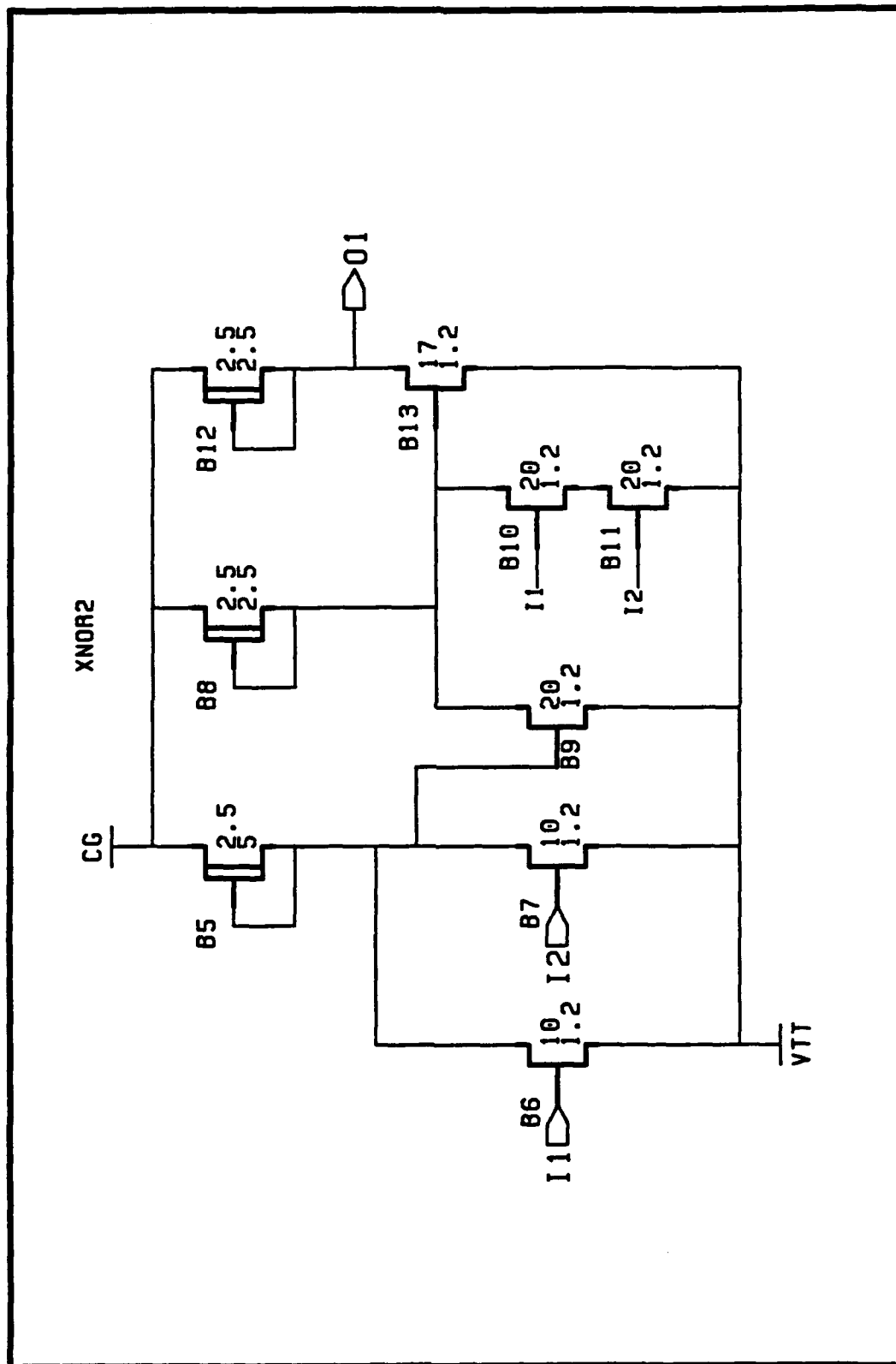


VOTEREG16

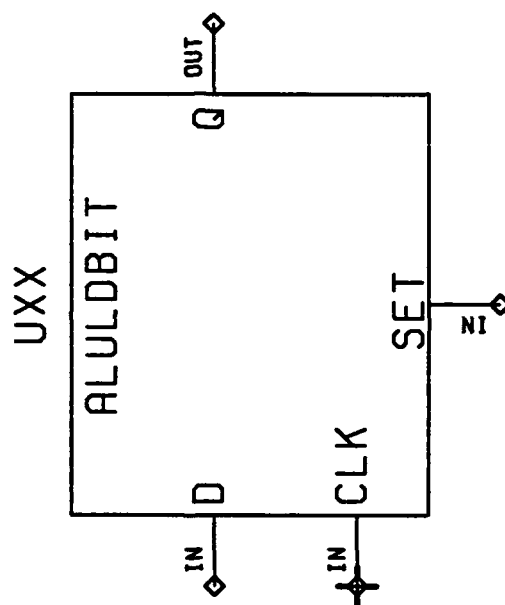


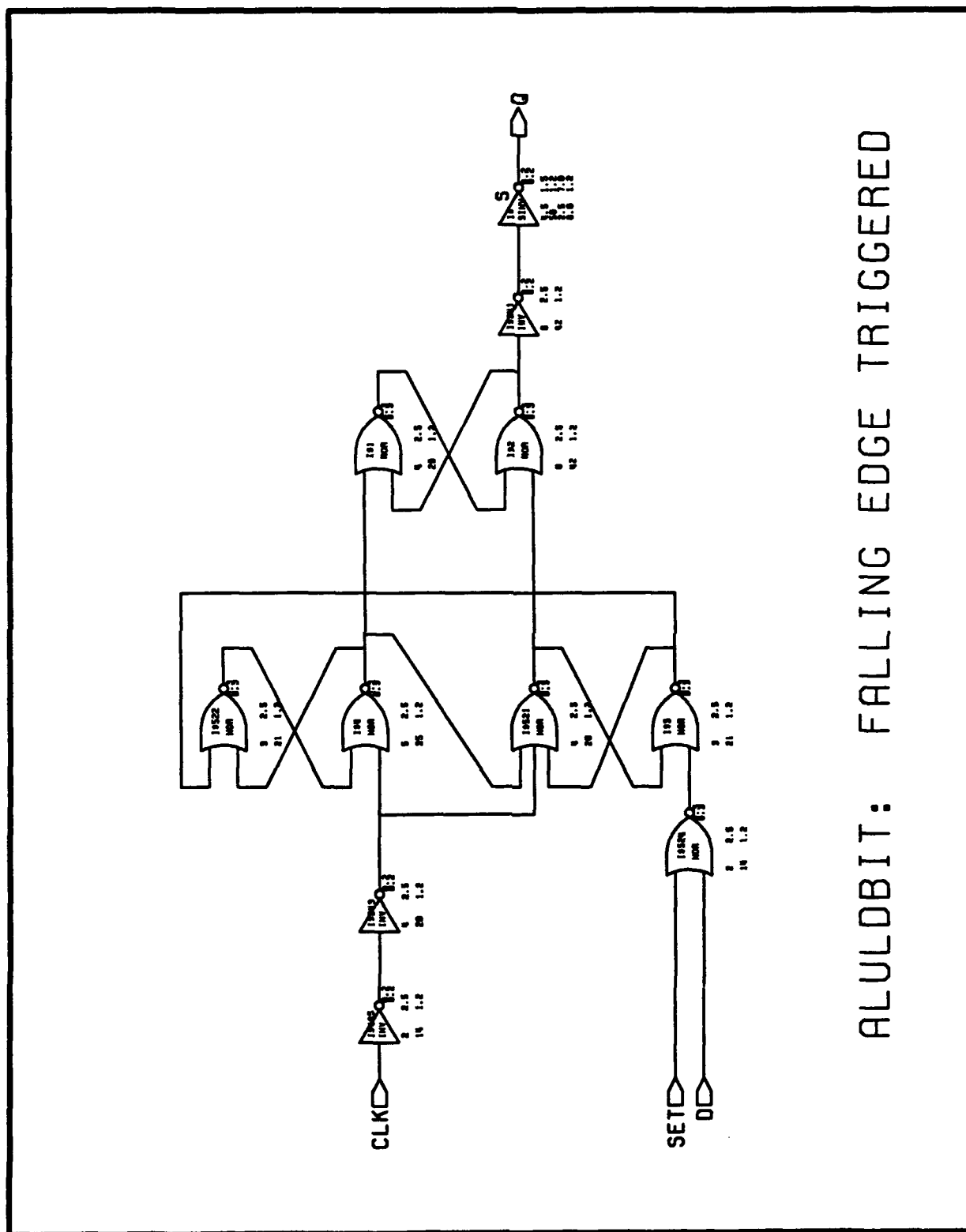


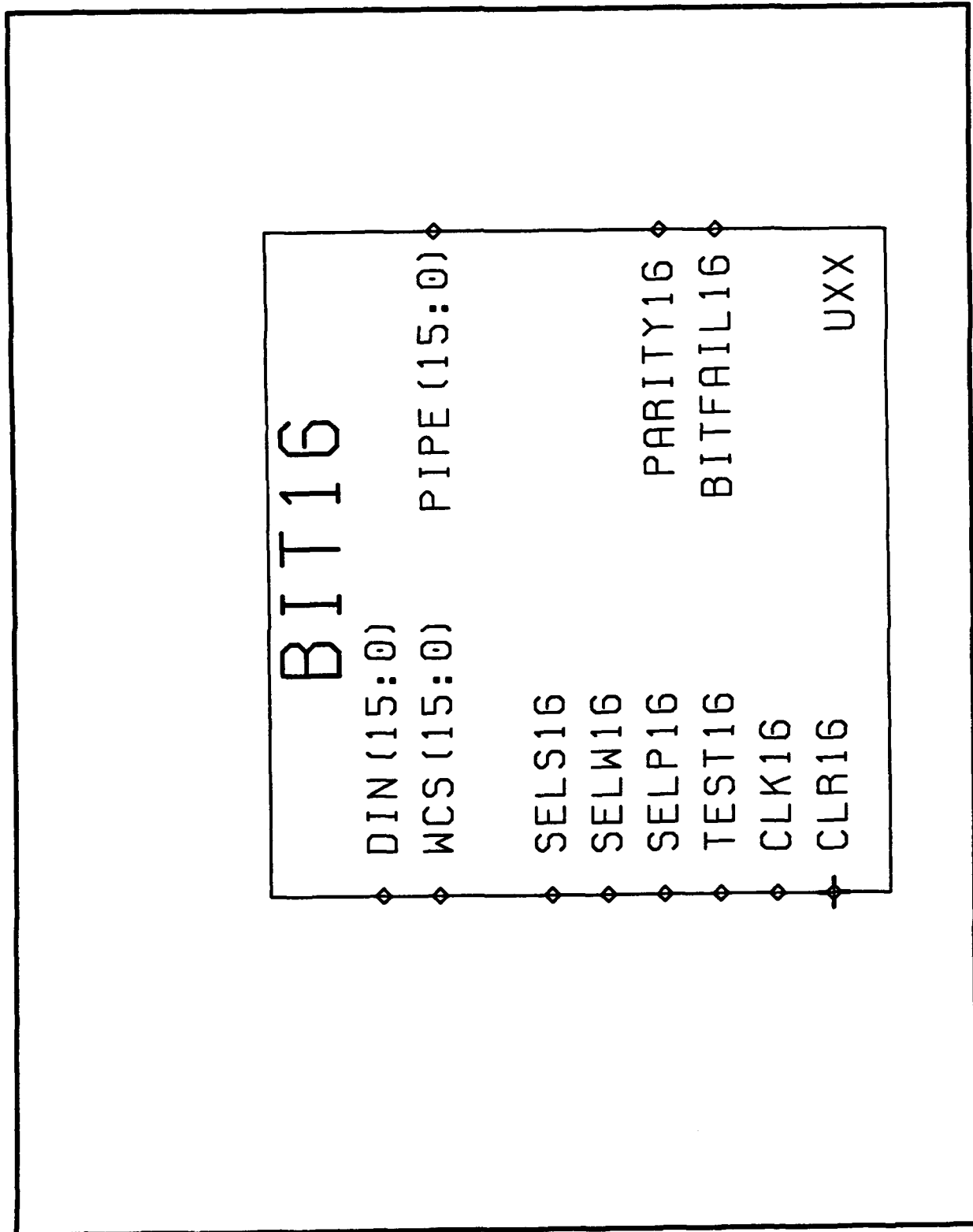


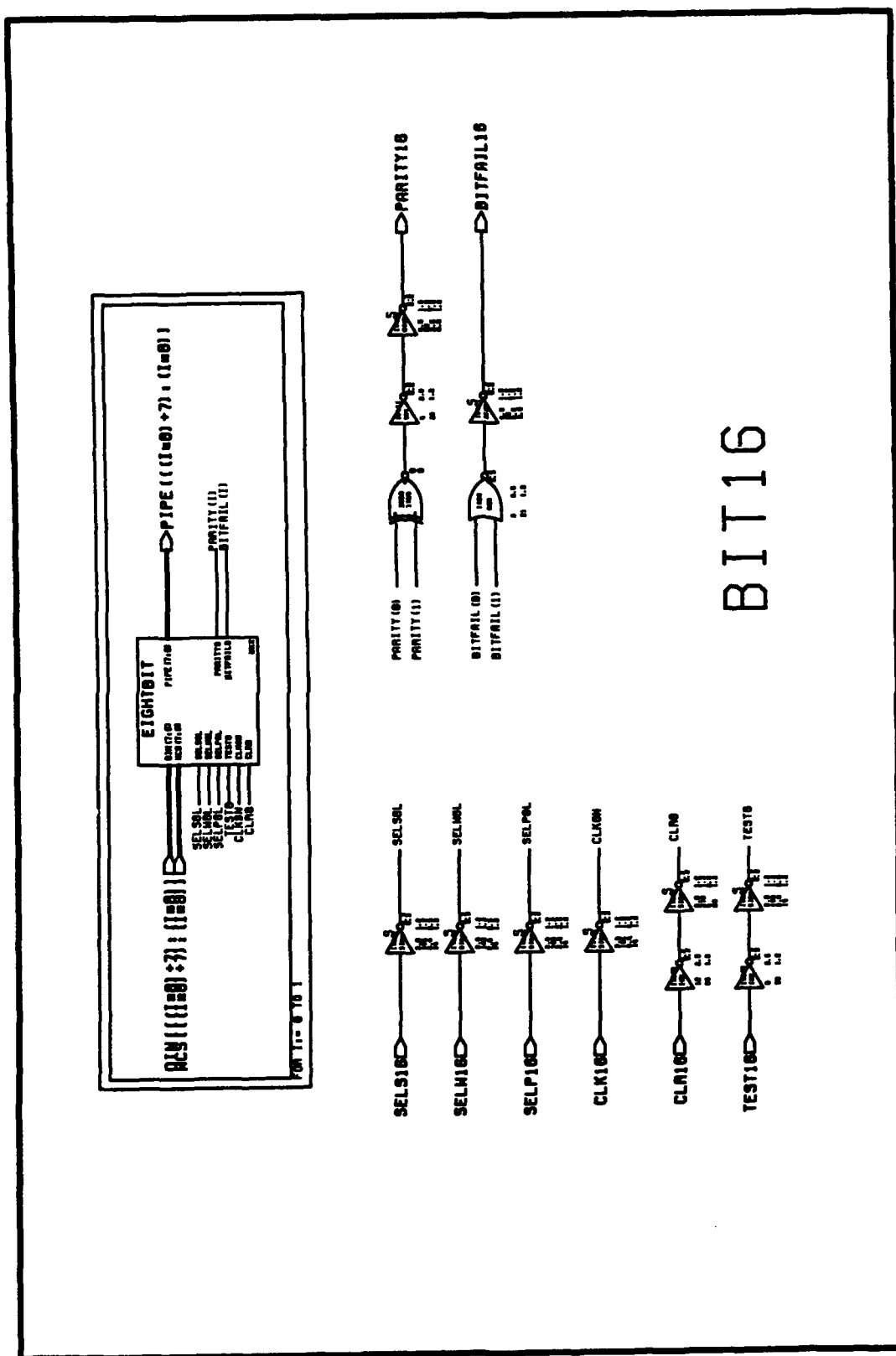






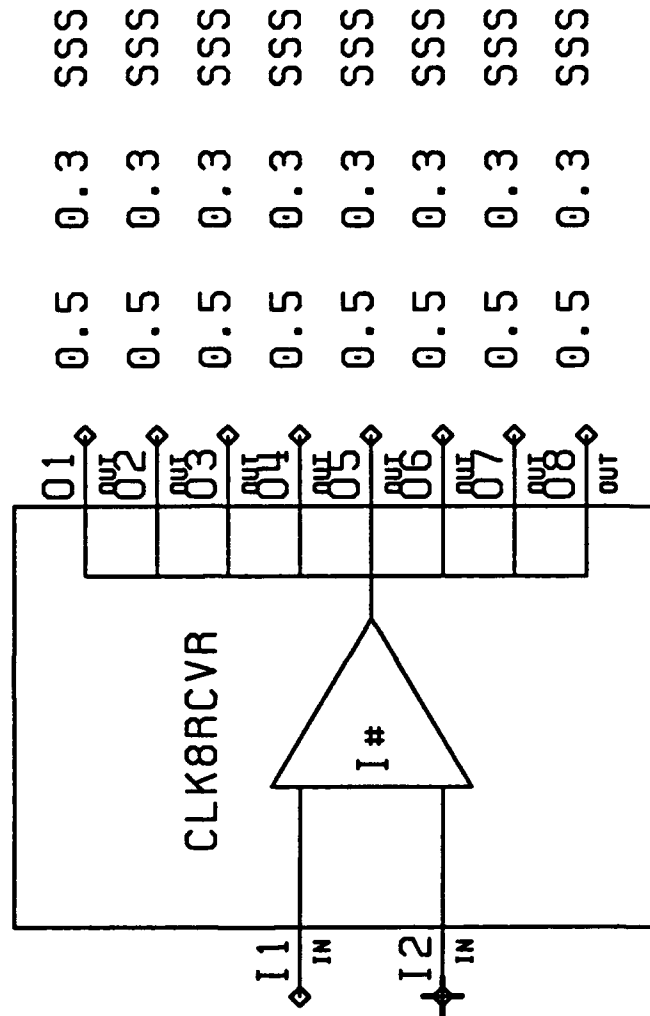




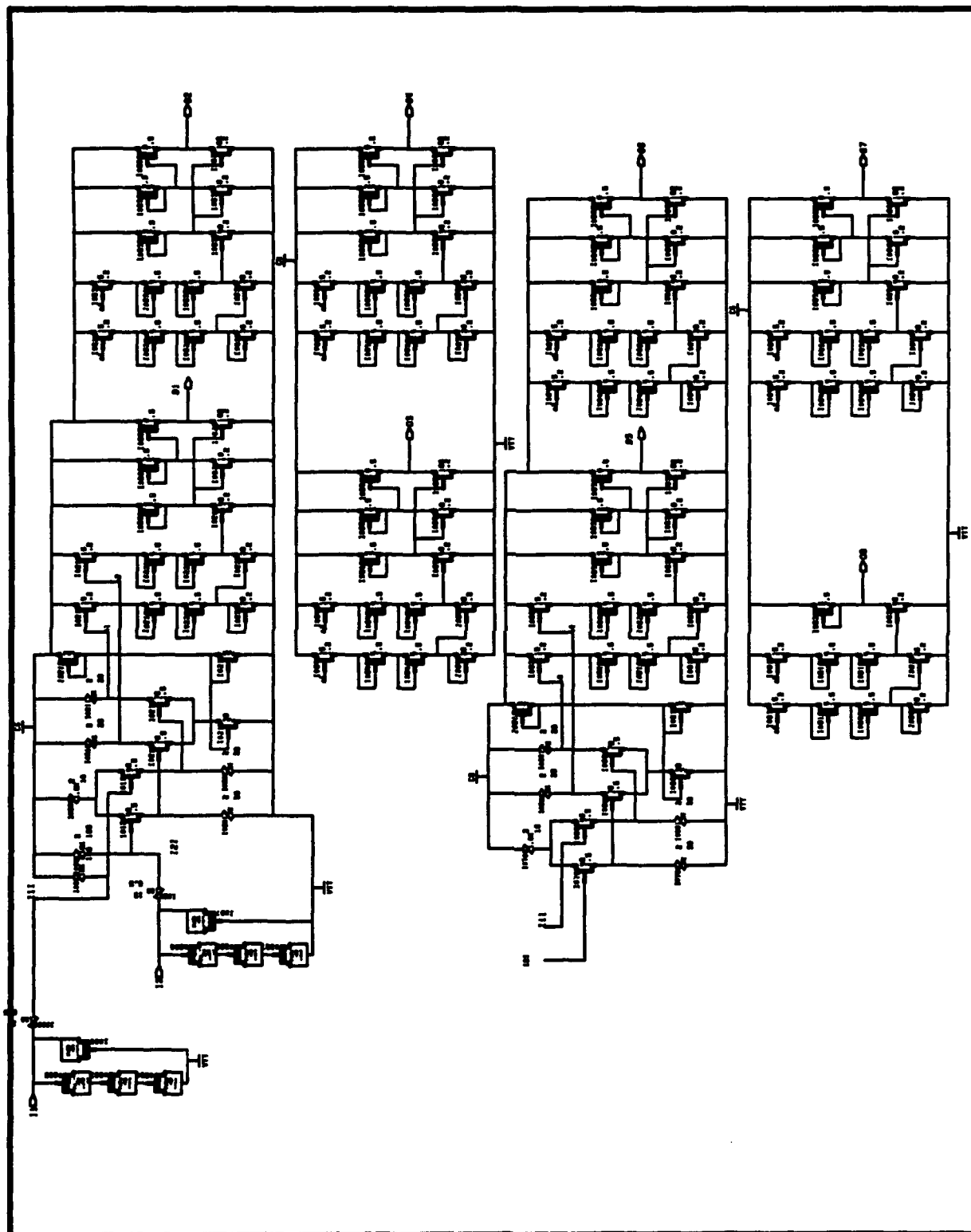


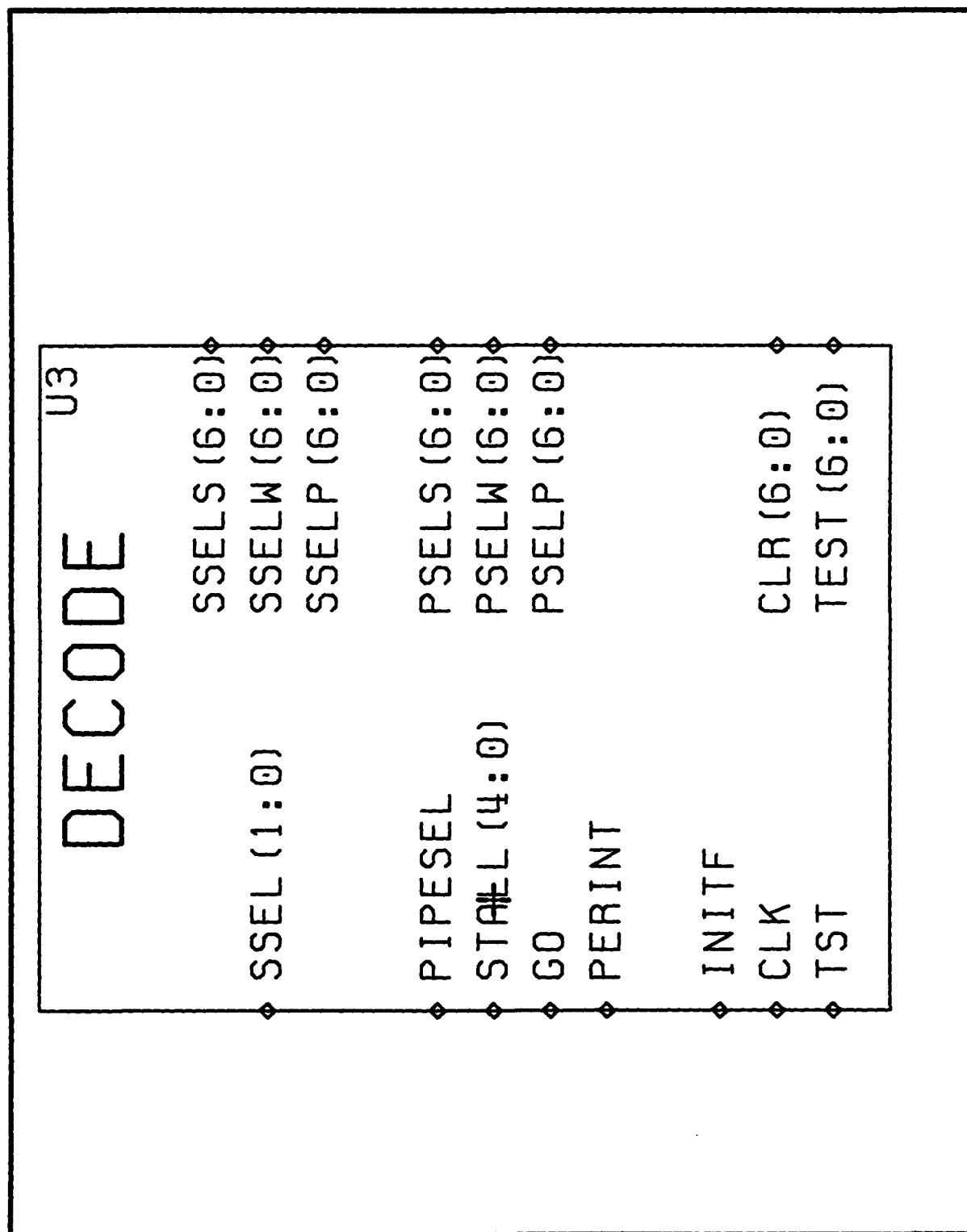
VITESSE GAAS CELL LIBRARY  
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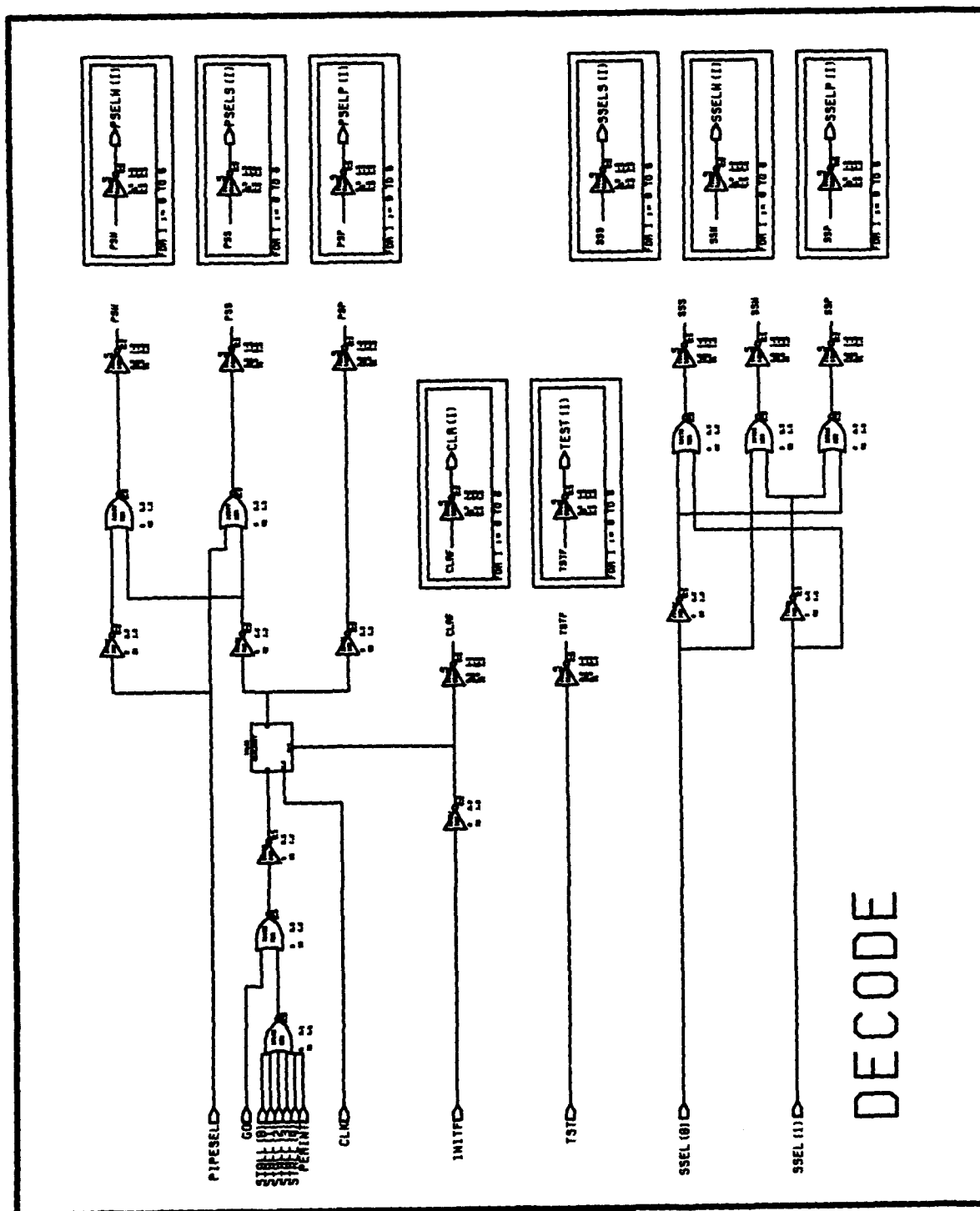
NAME: CLK8RCVR  
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER



clk8rcvr  
clk8rcvr.bin







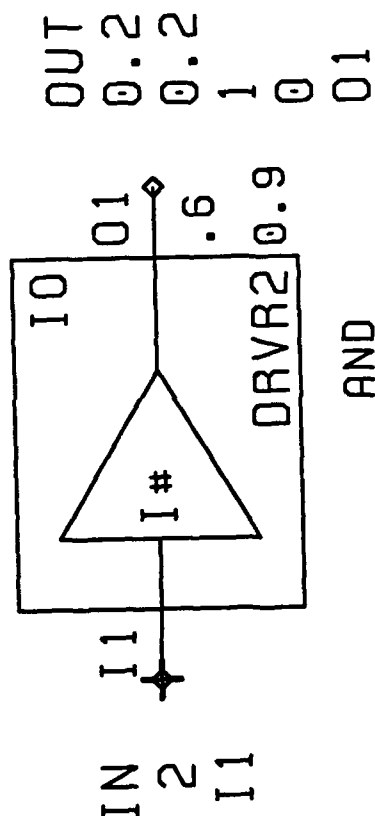


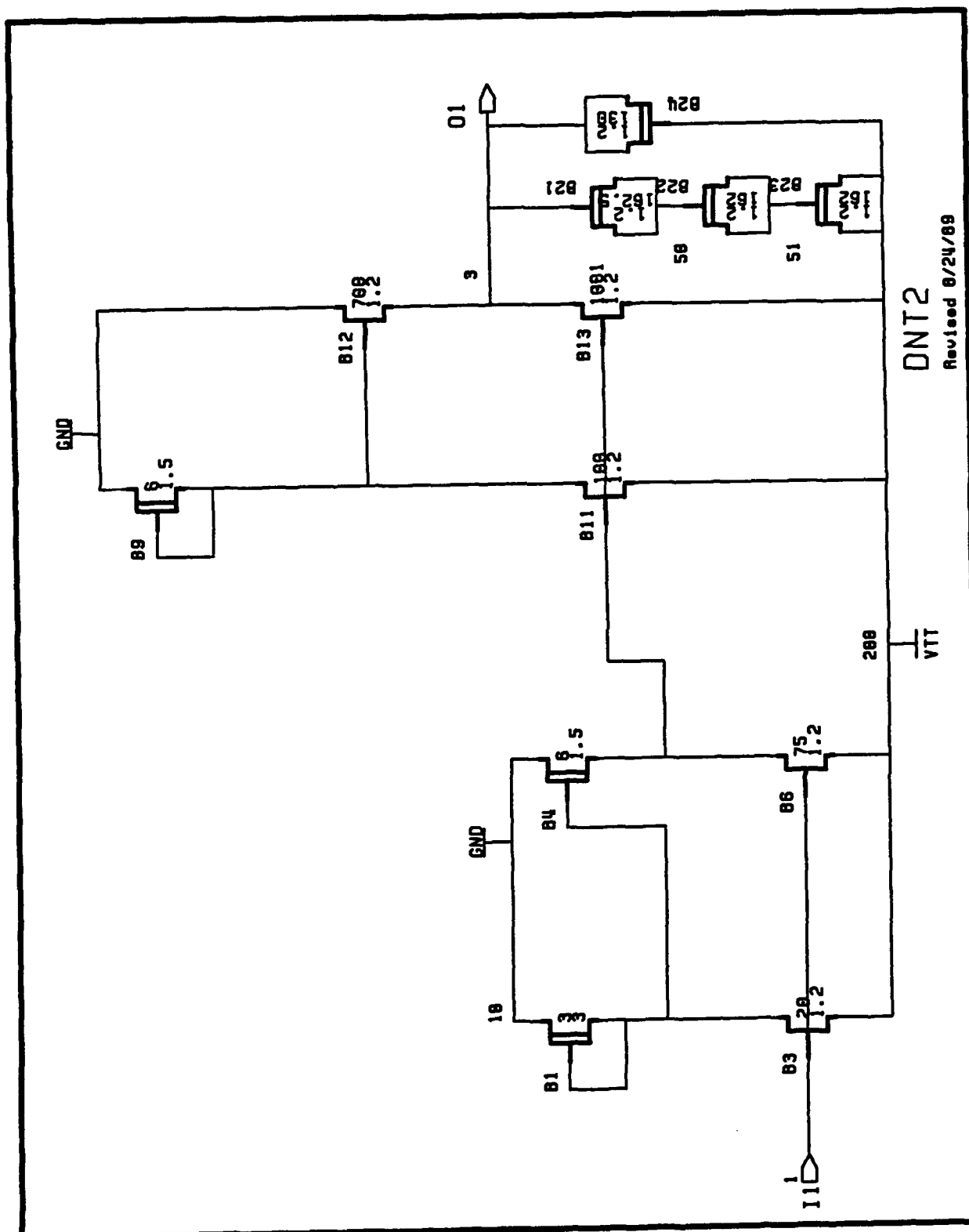
# VITESSE GAAS CELL LIBRARY

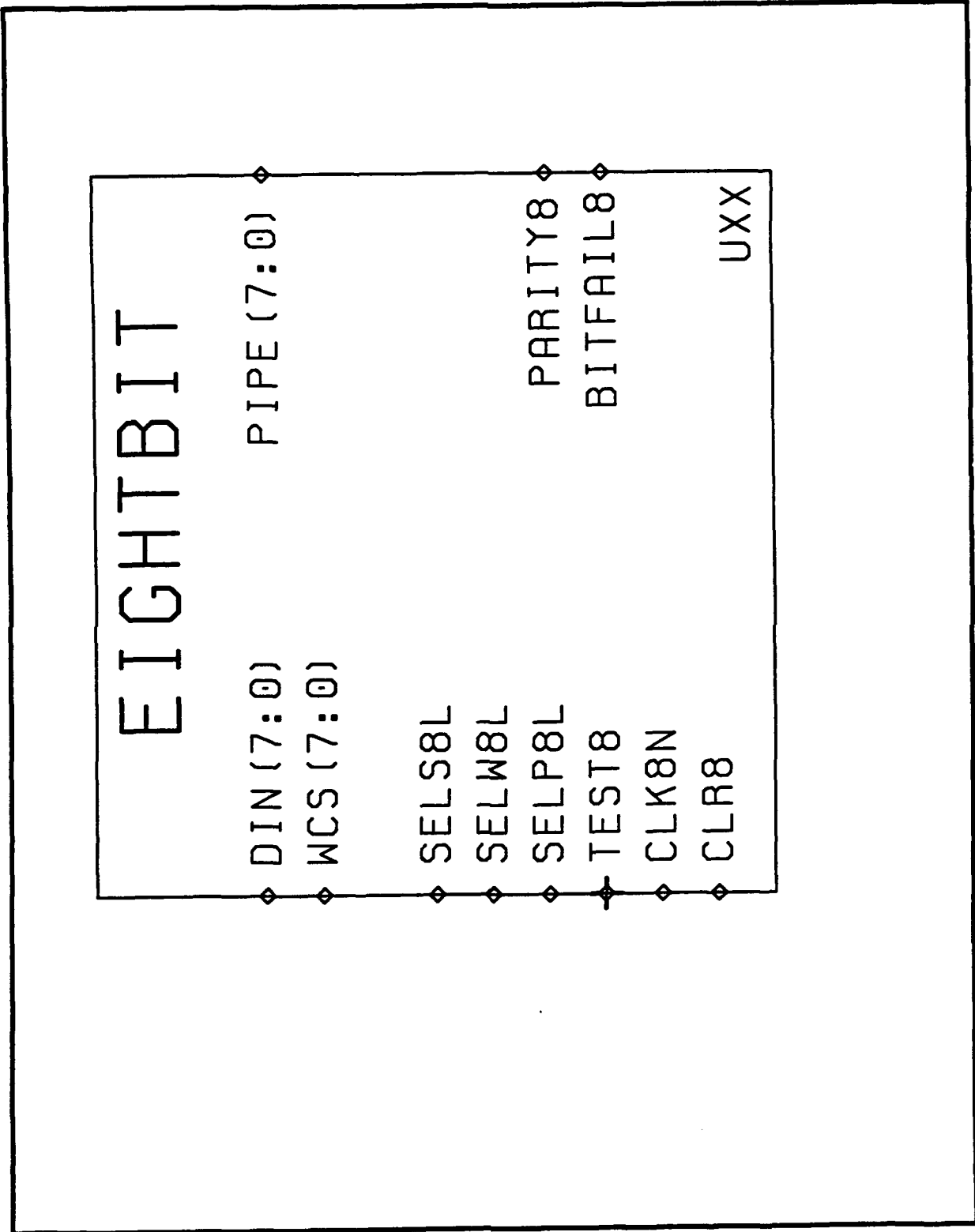
Version 0.8

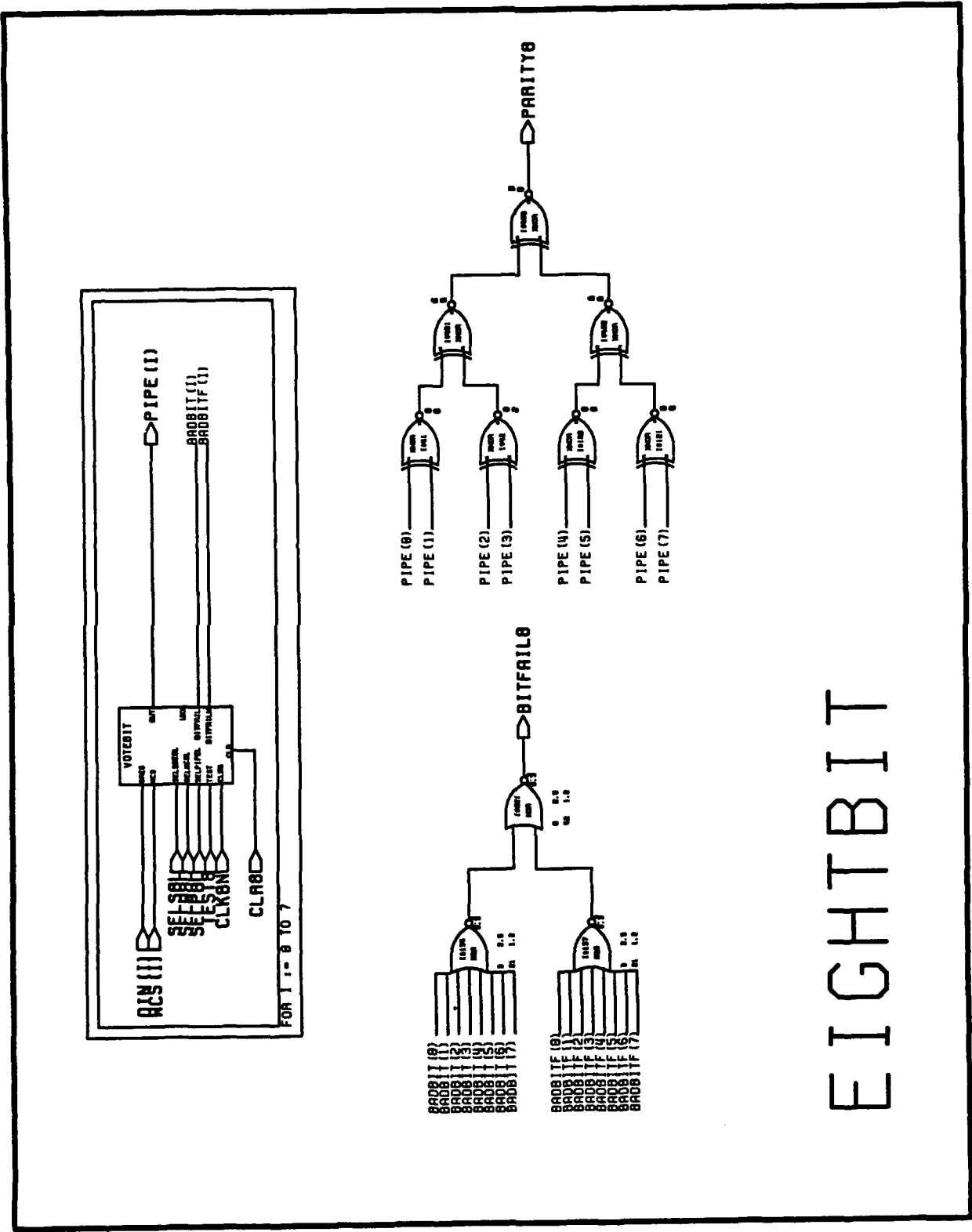
NAME: DRV2

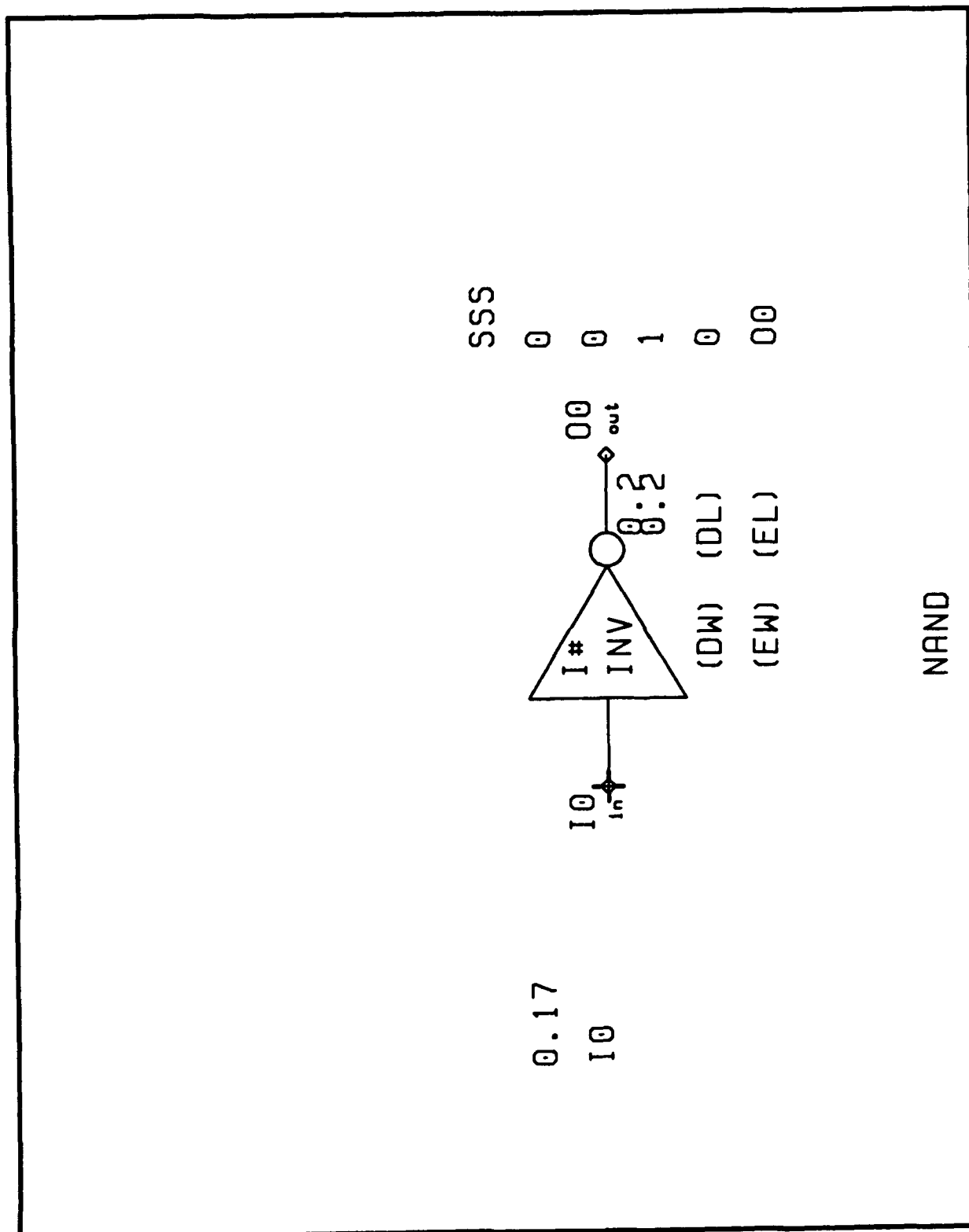
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD

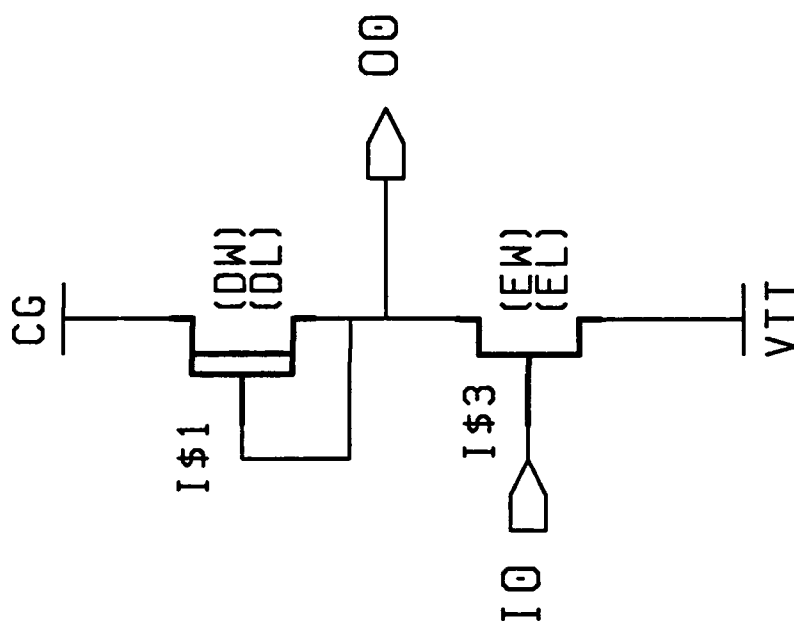


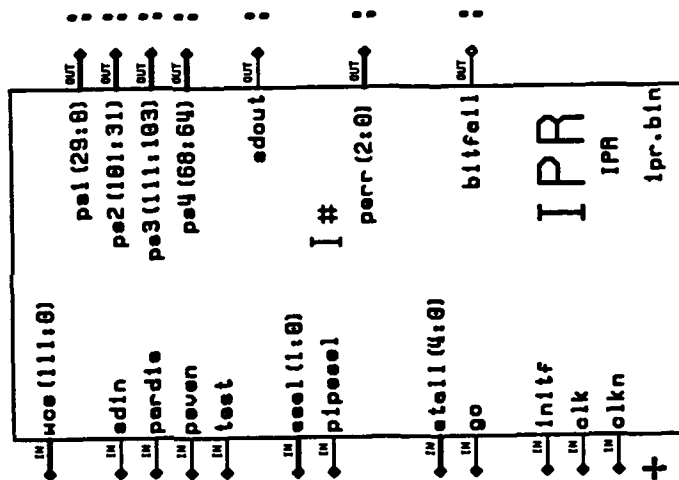


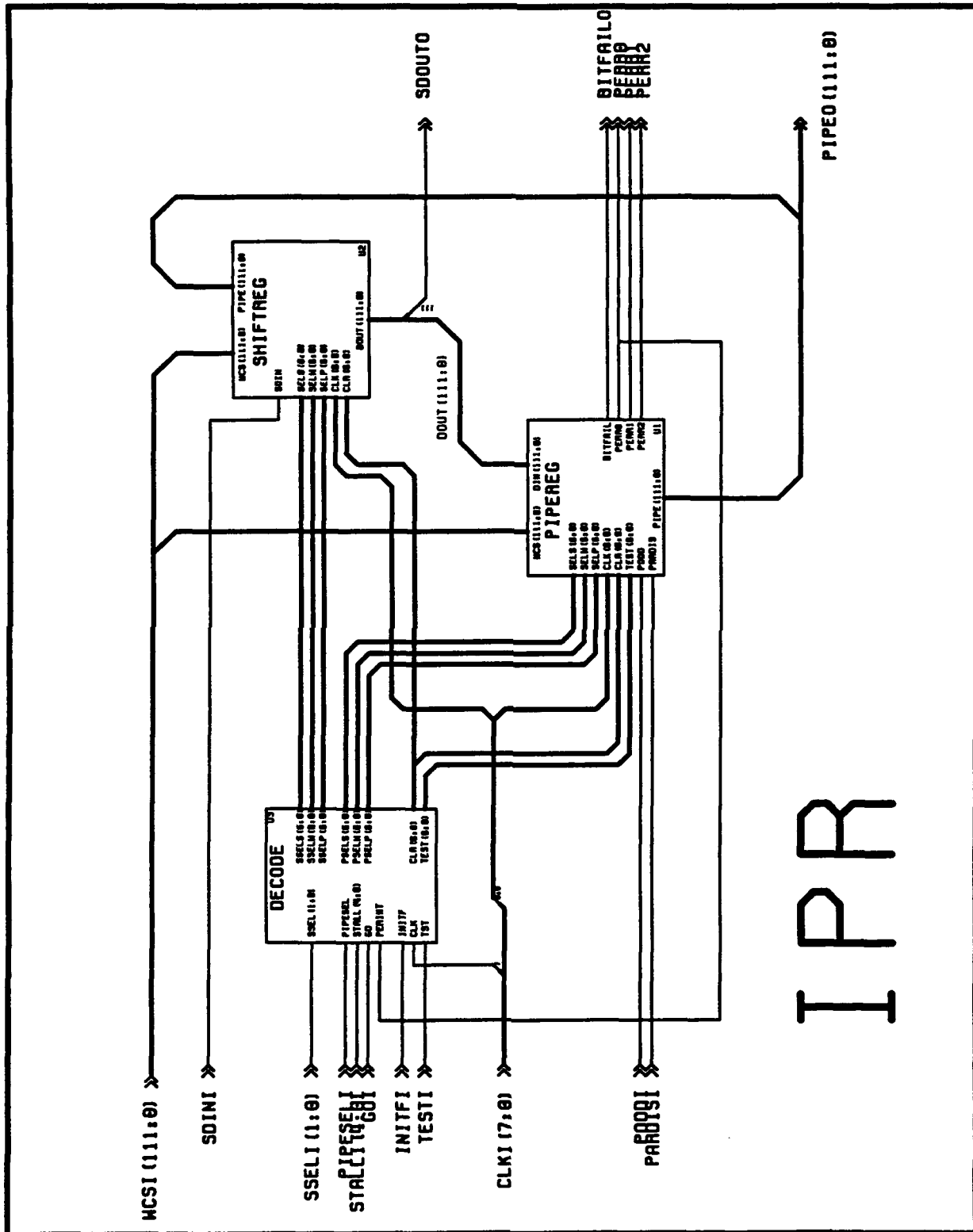




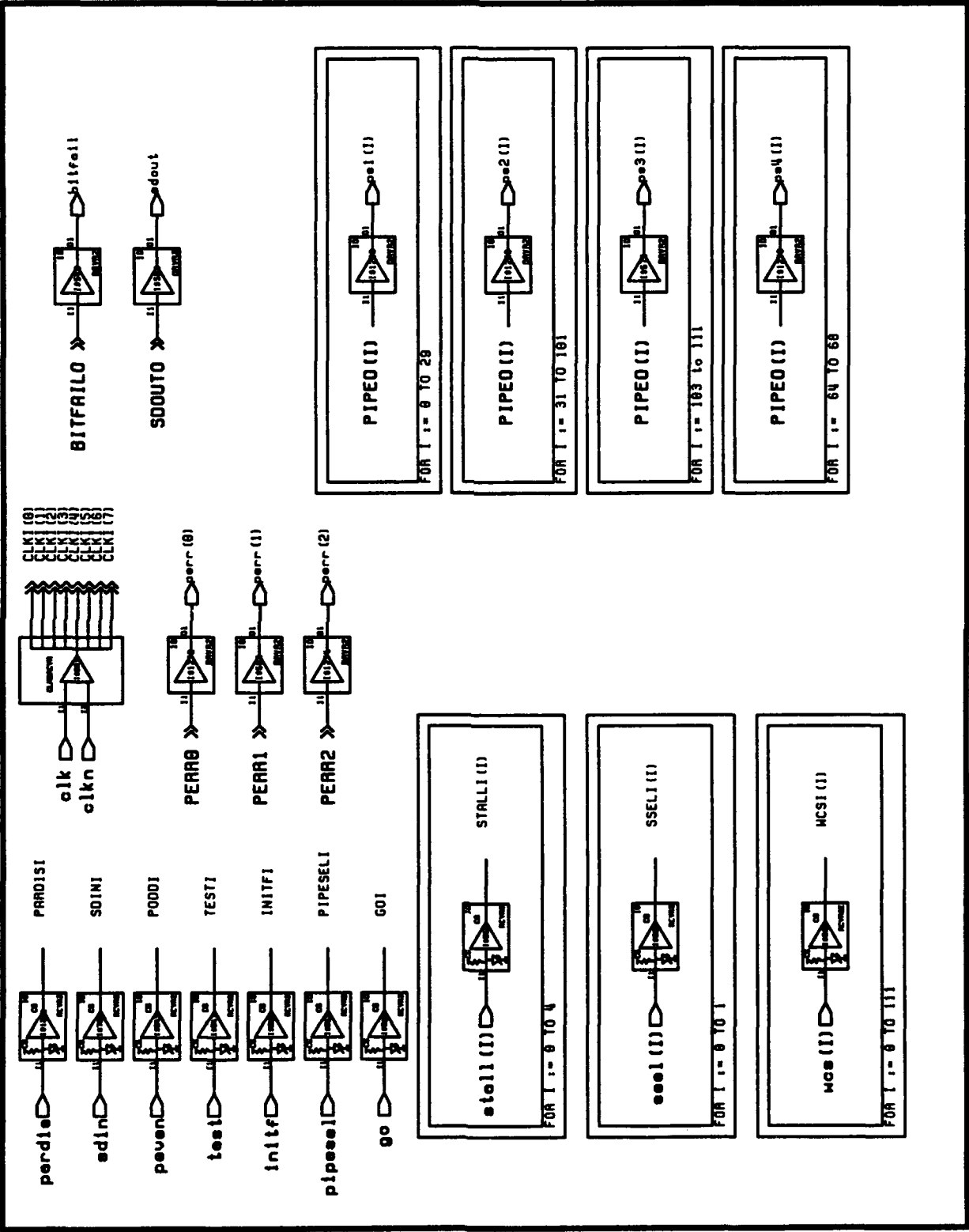


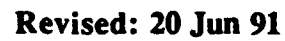


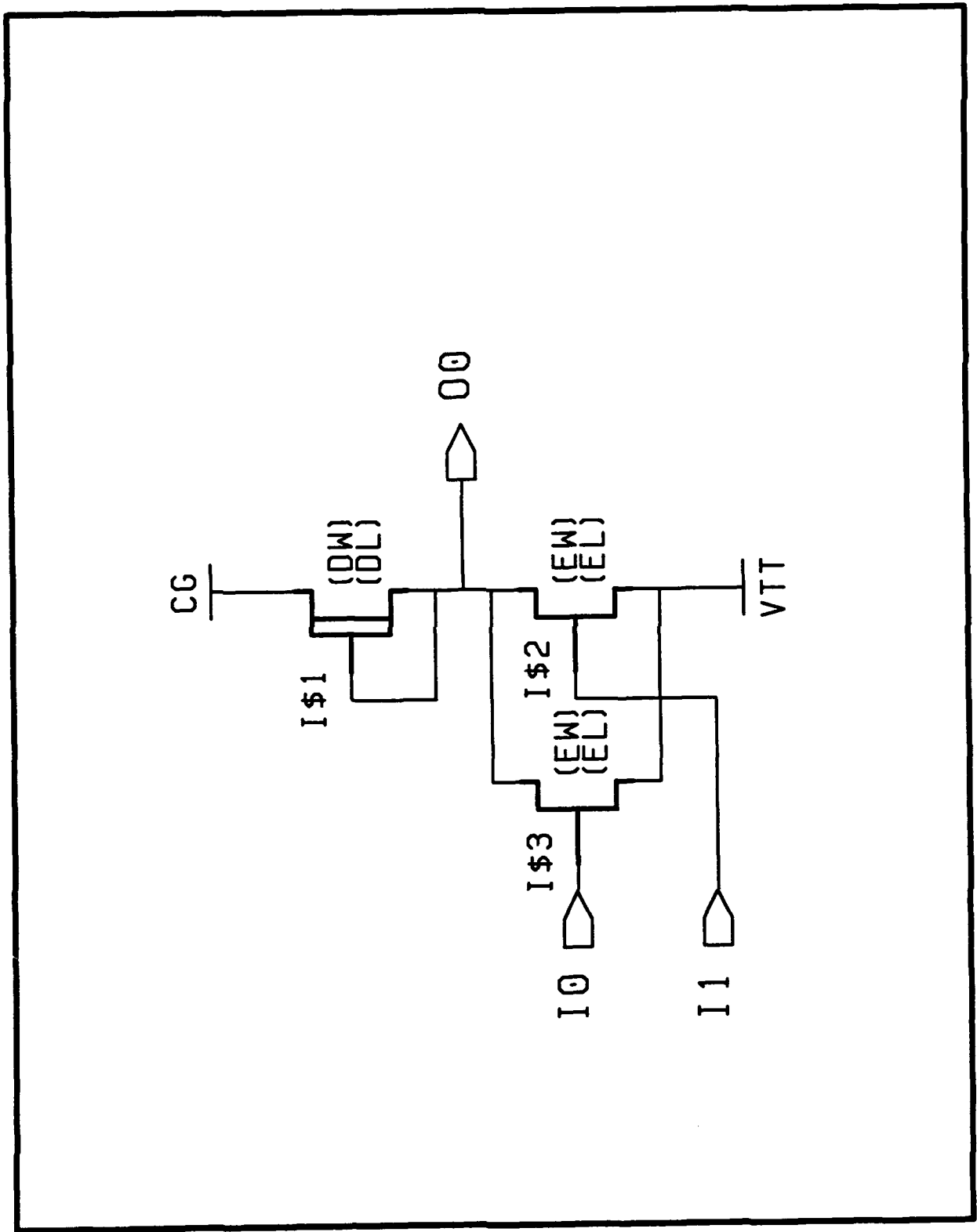


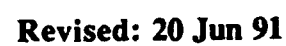


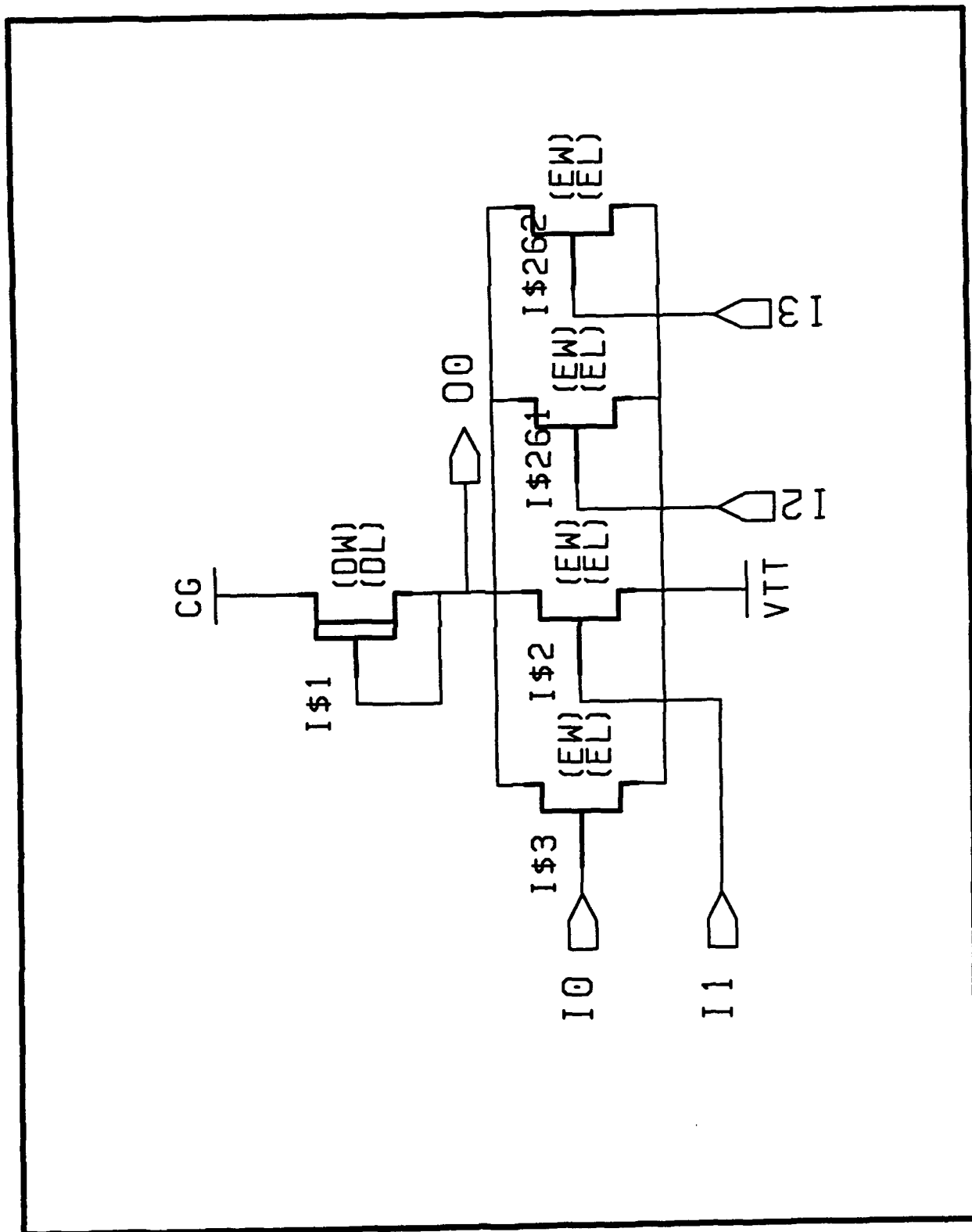


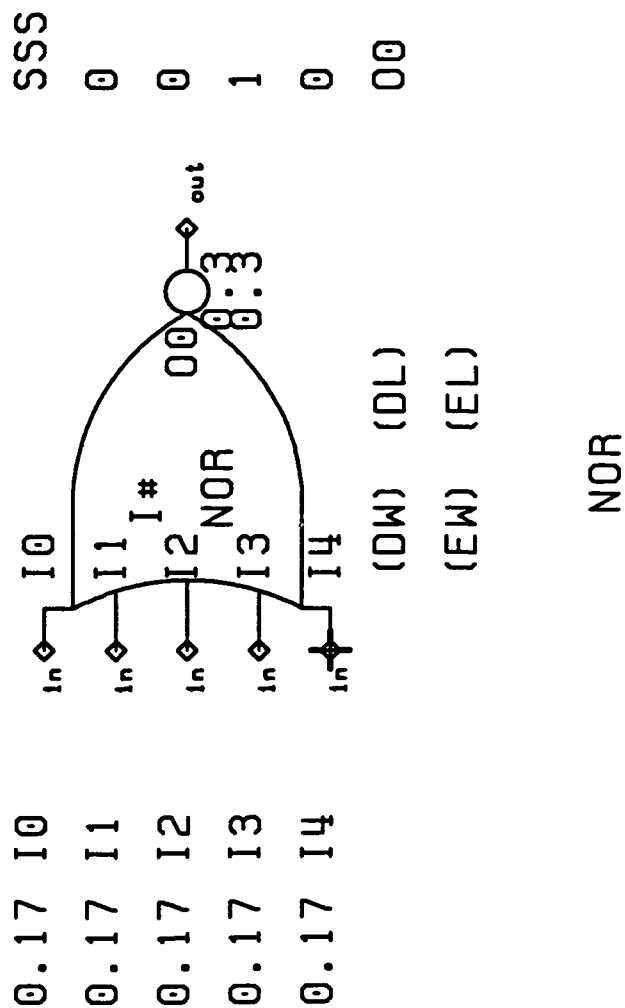


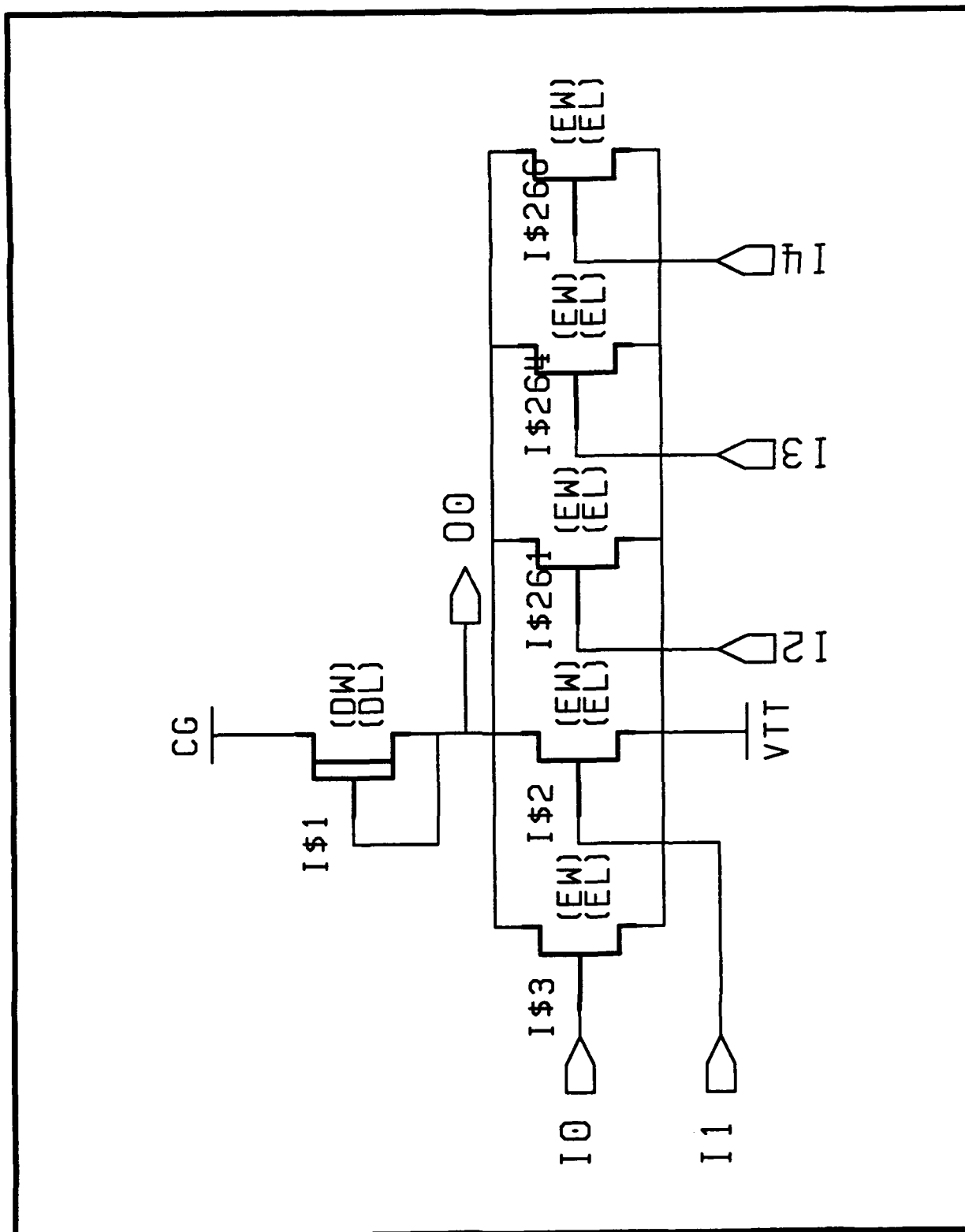


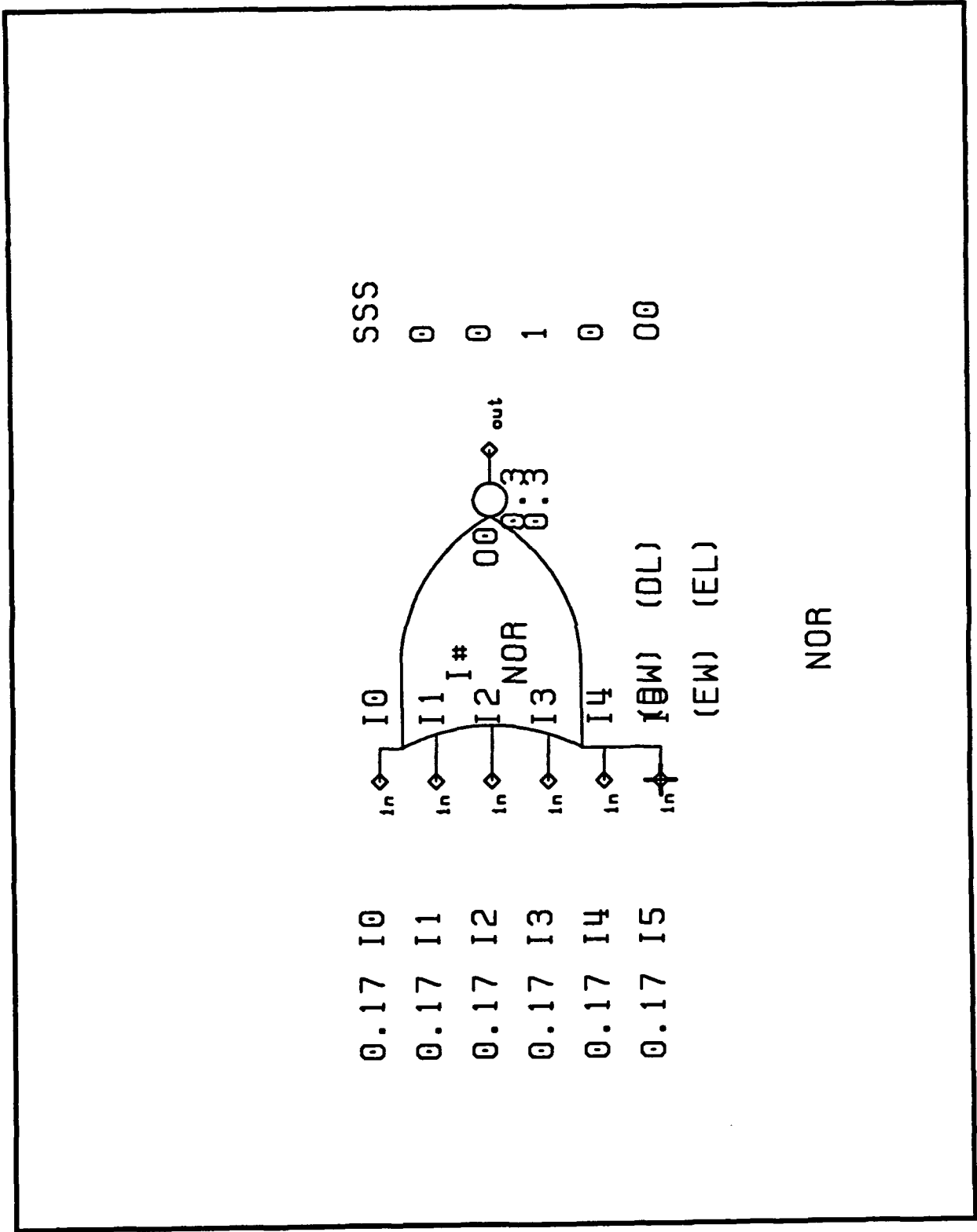




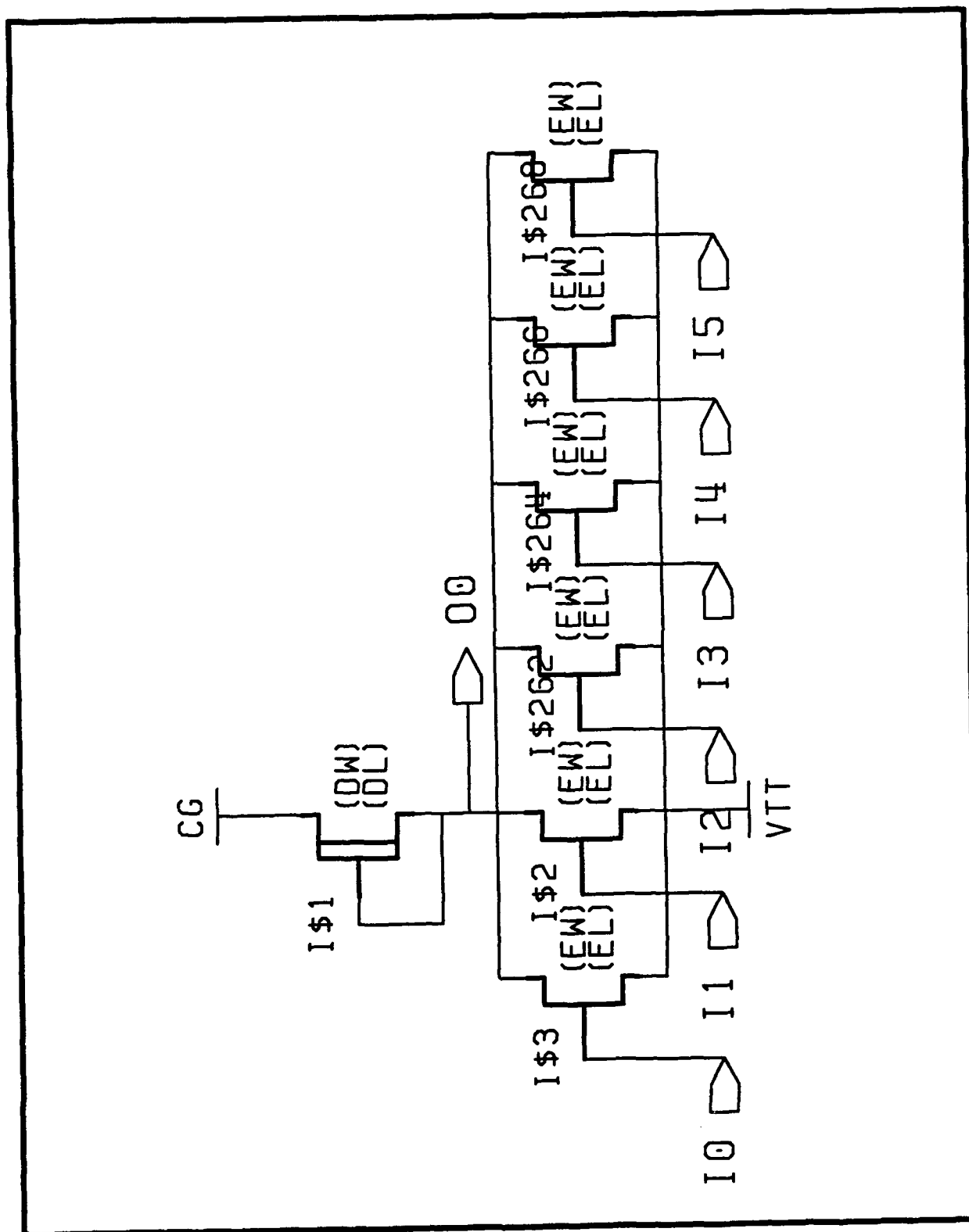


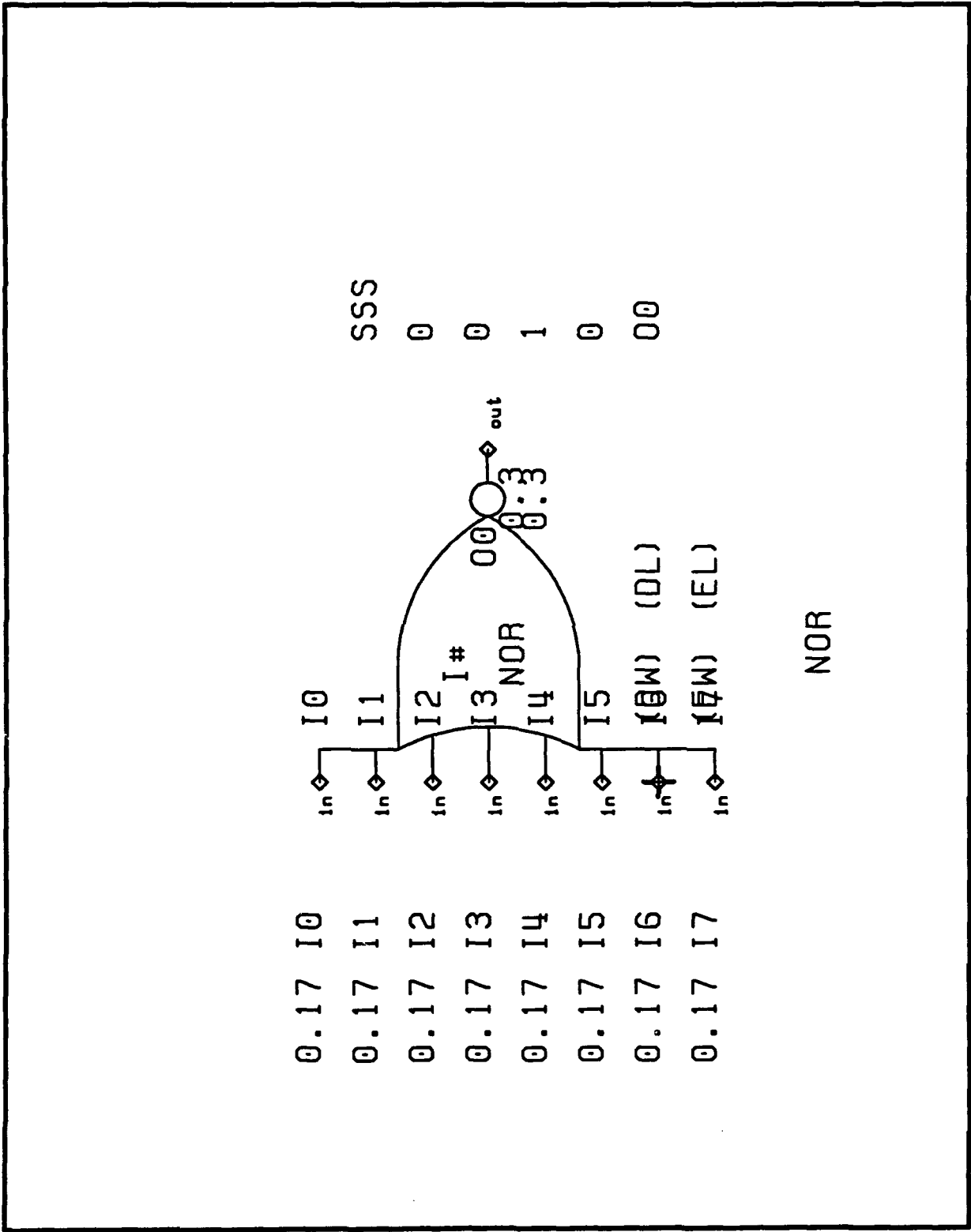


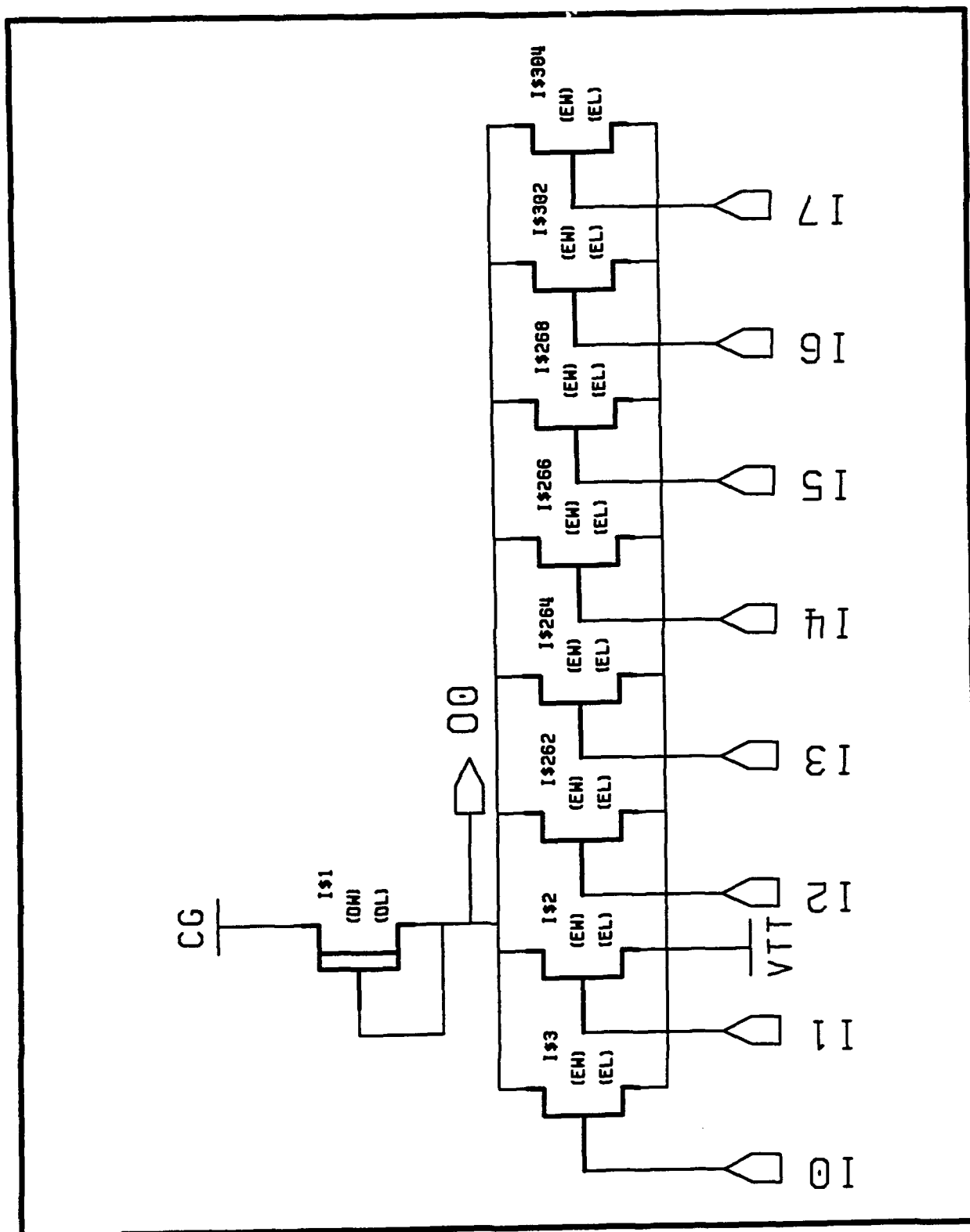


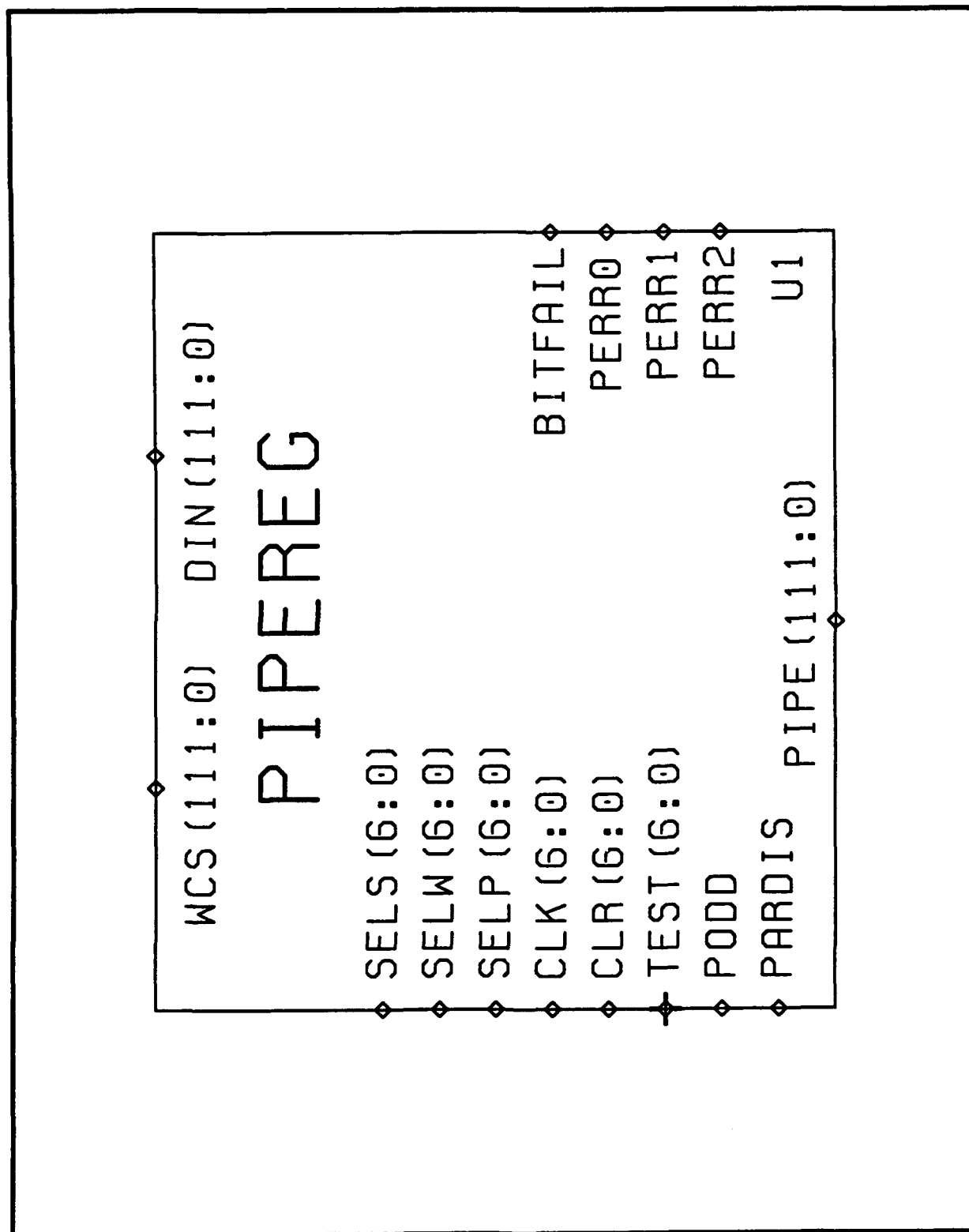


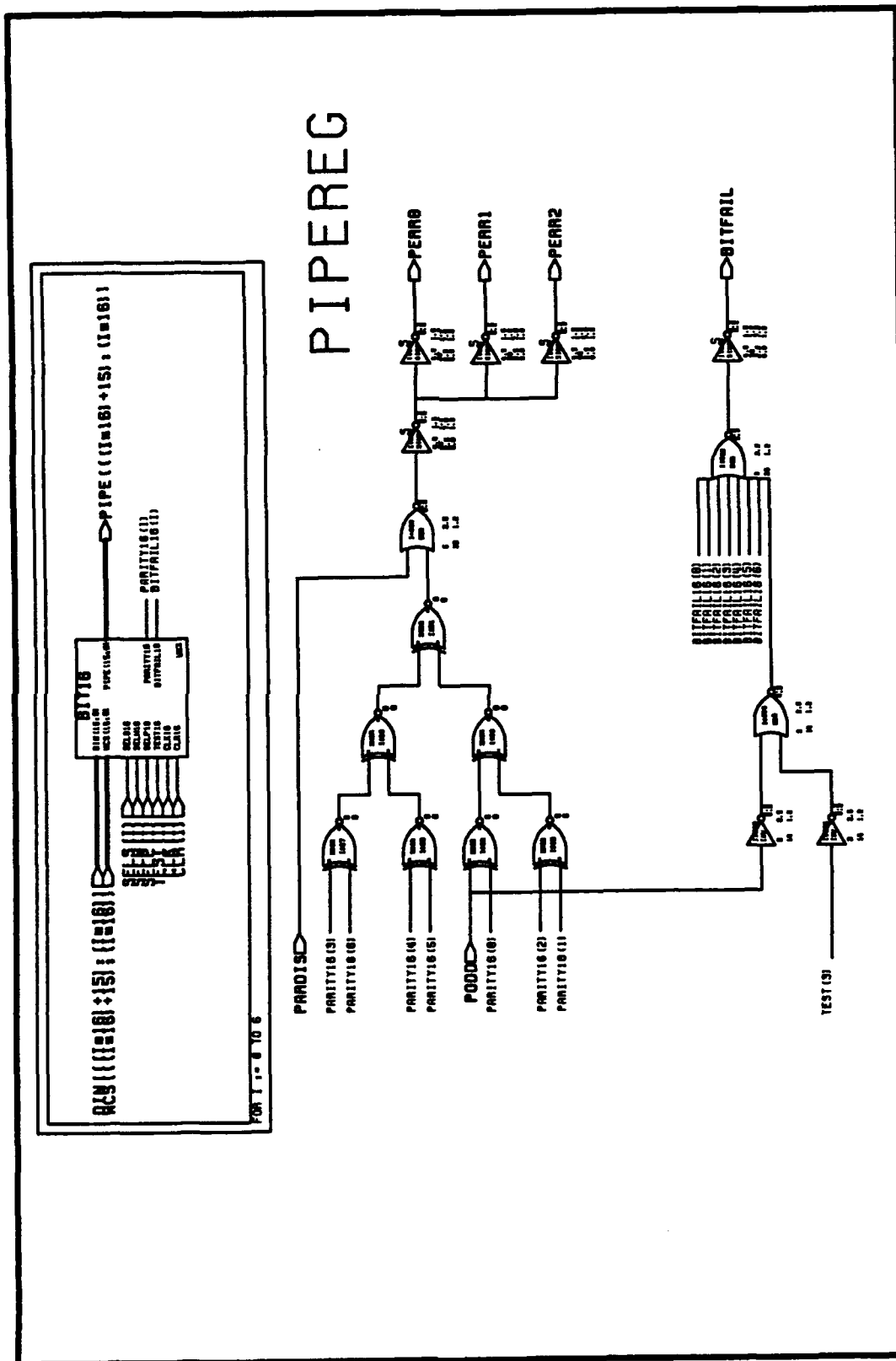






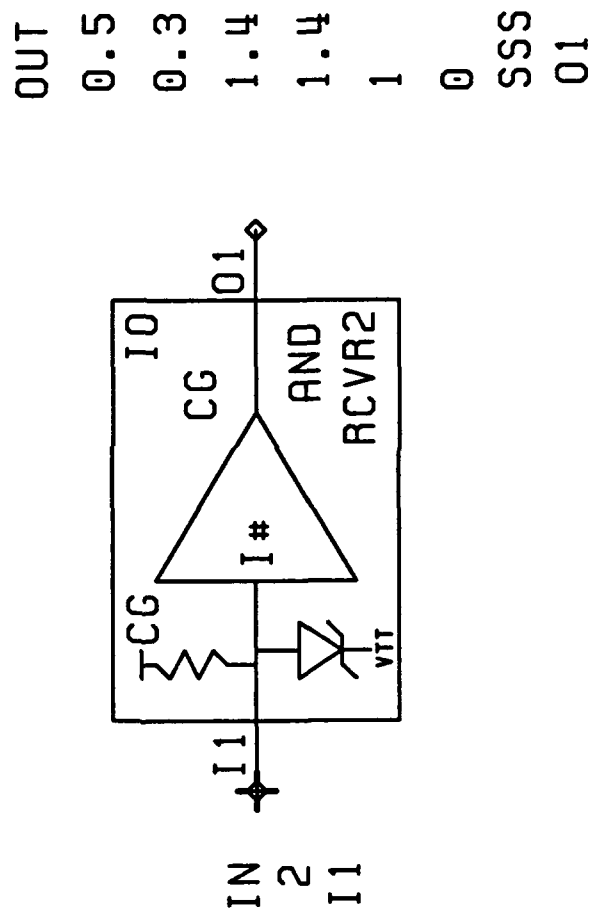


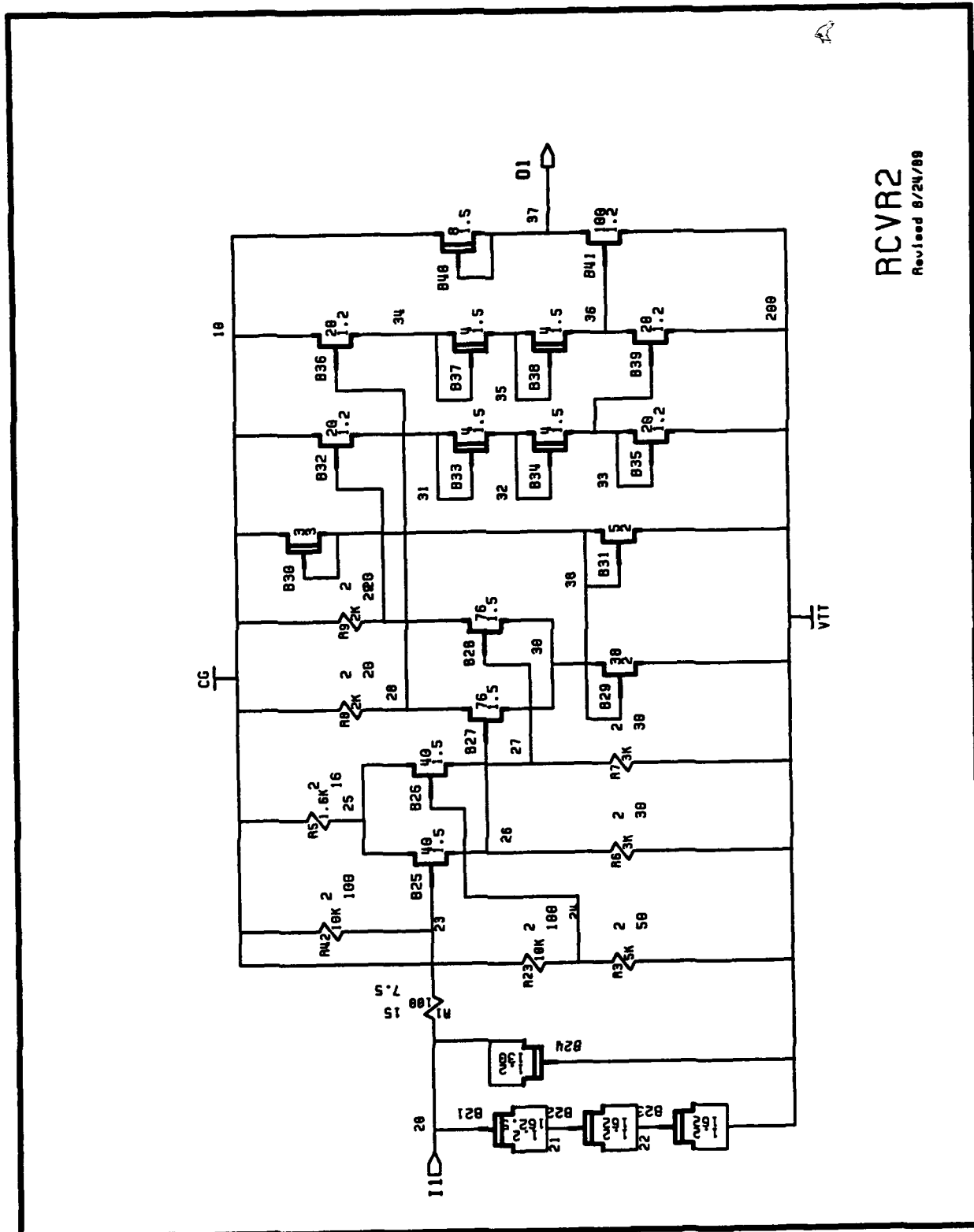




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Version 0.8

NAME: RCVR2  
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD

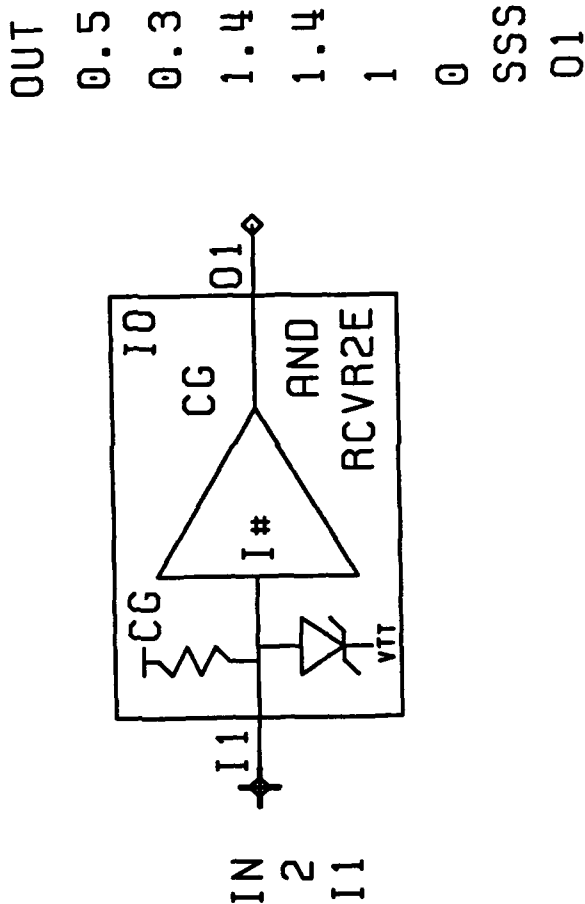




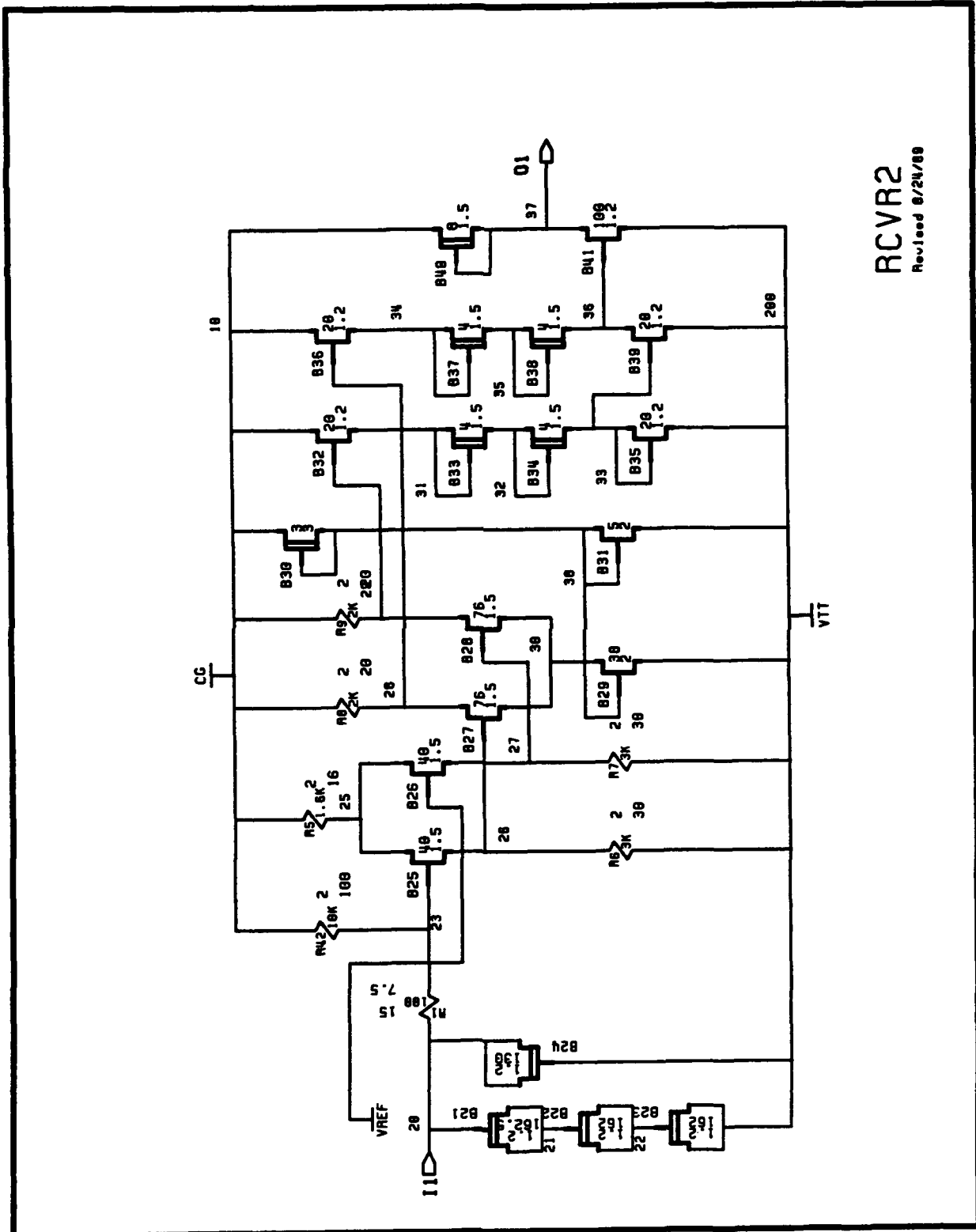
VITESSE GAAS CELL LIBRARY  
Version 0.8

NAME: RCVR2E

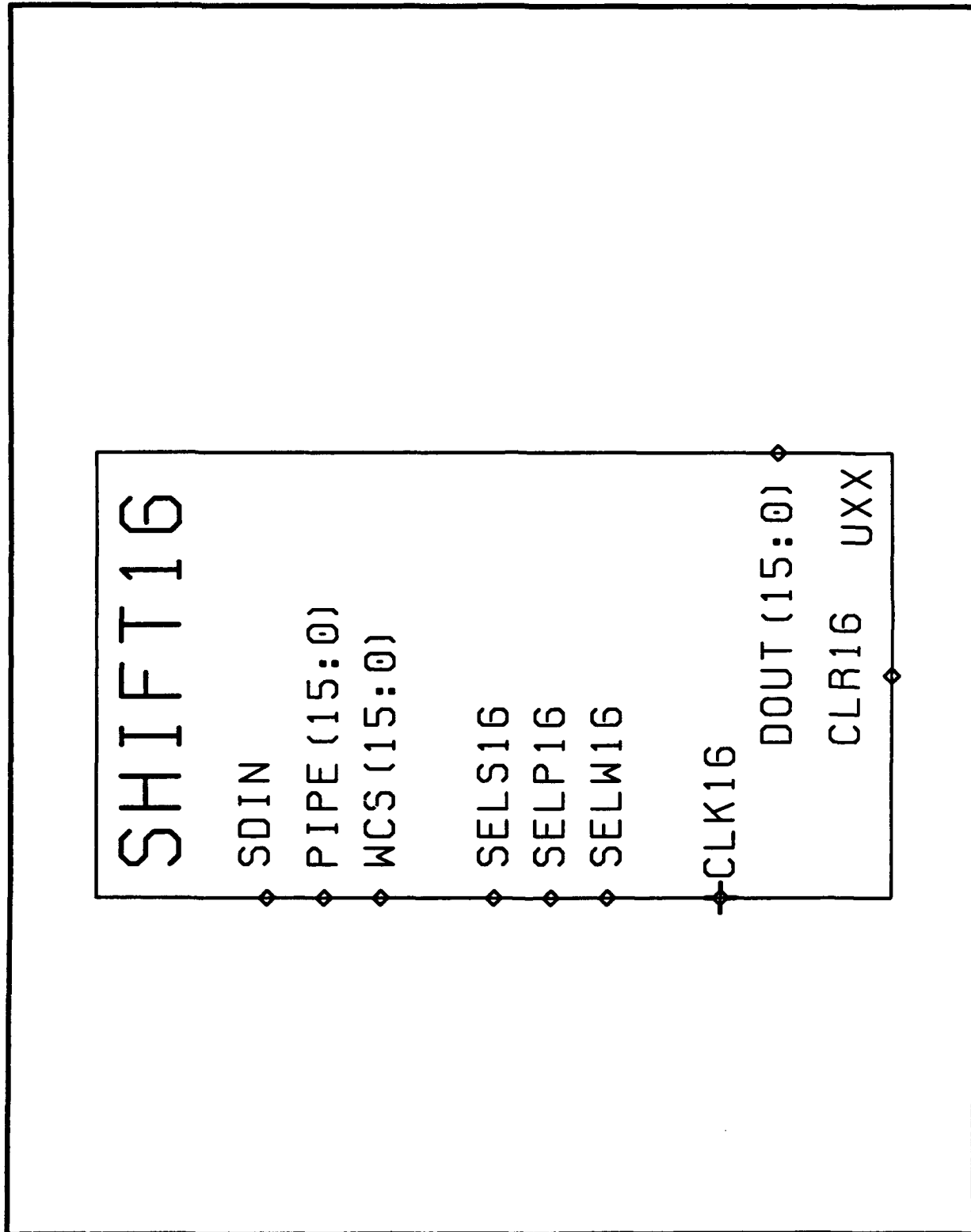
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD

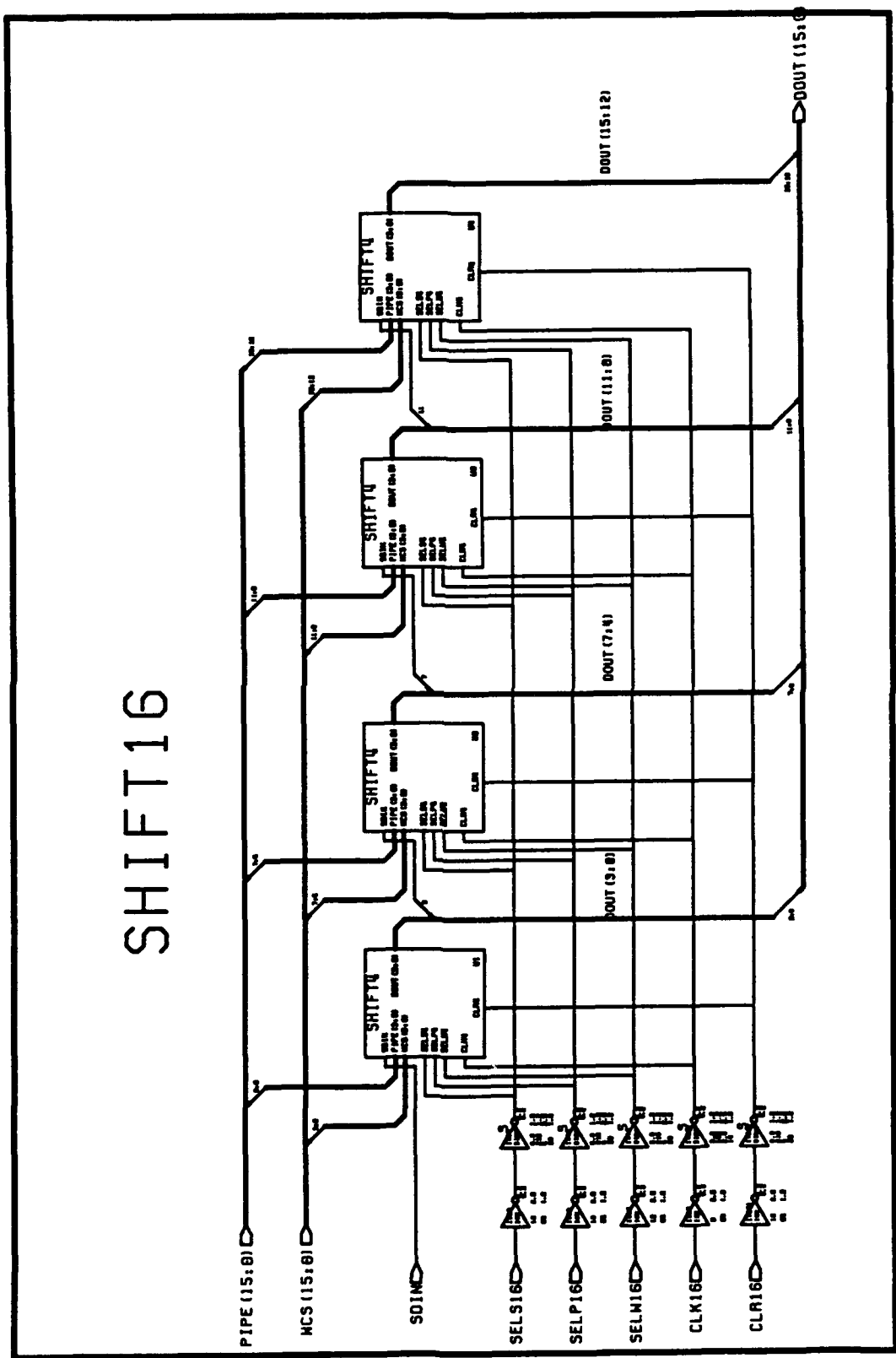


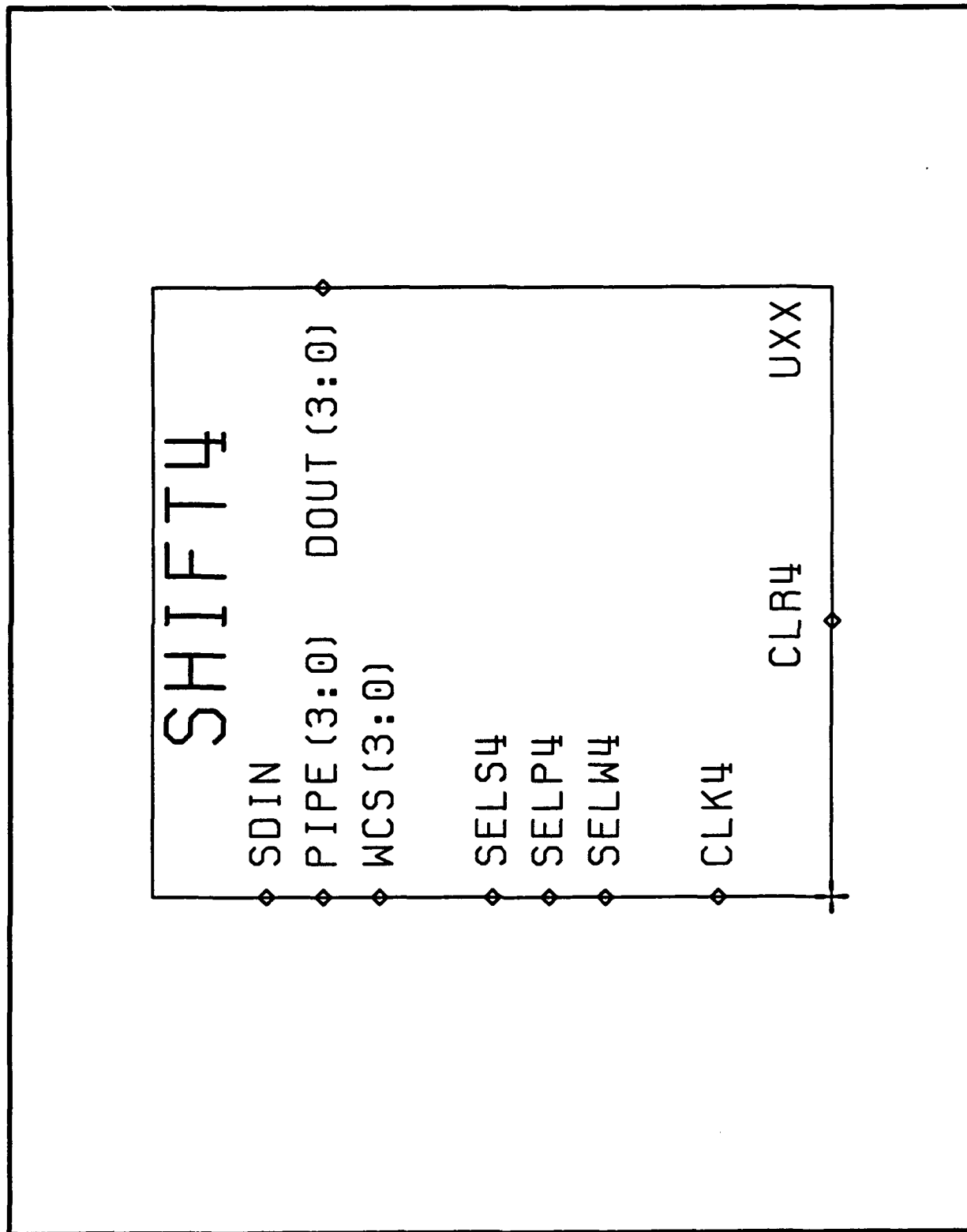


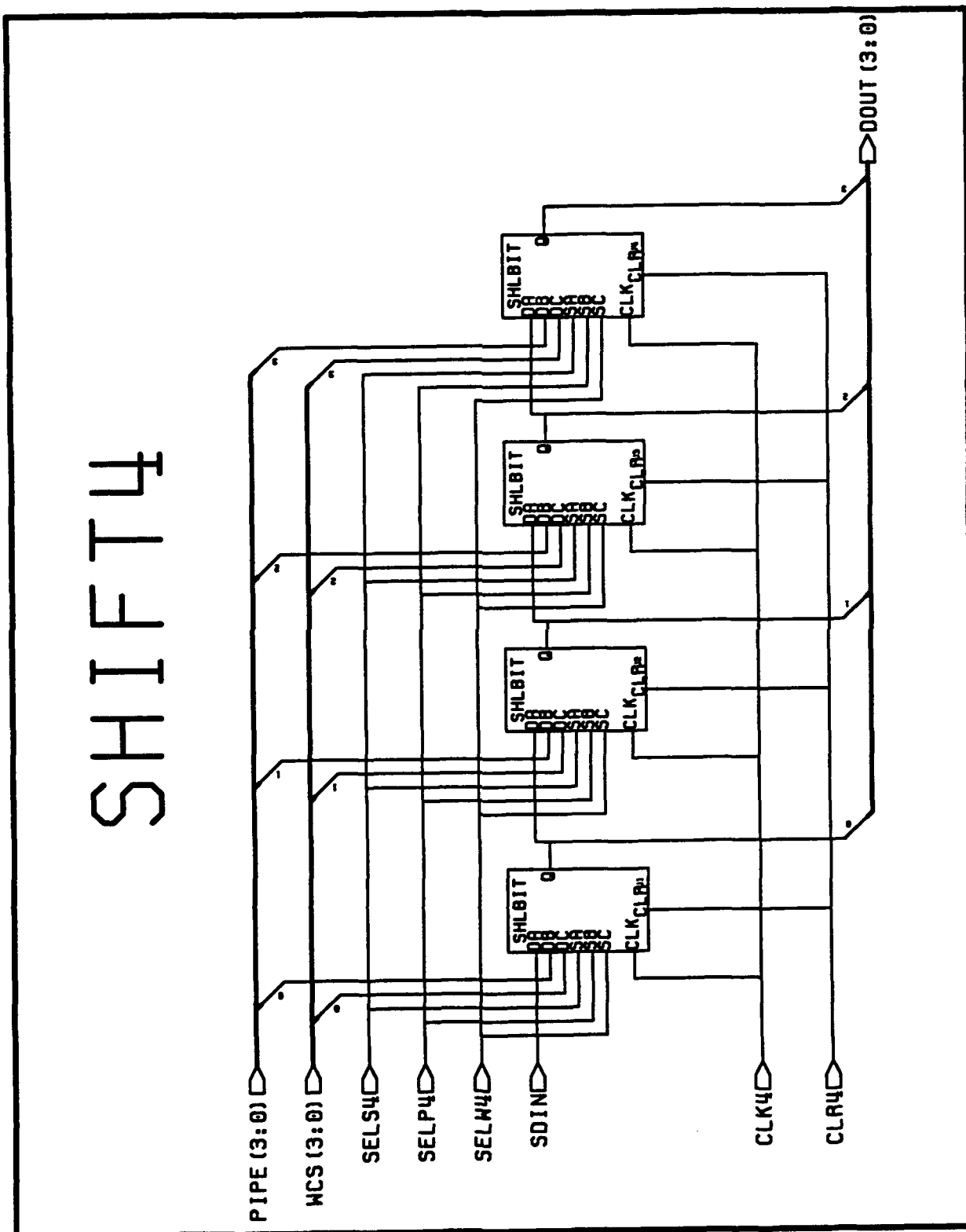


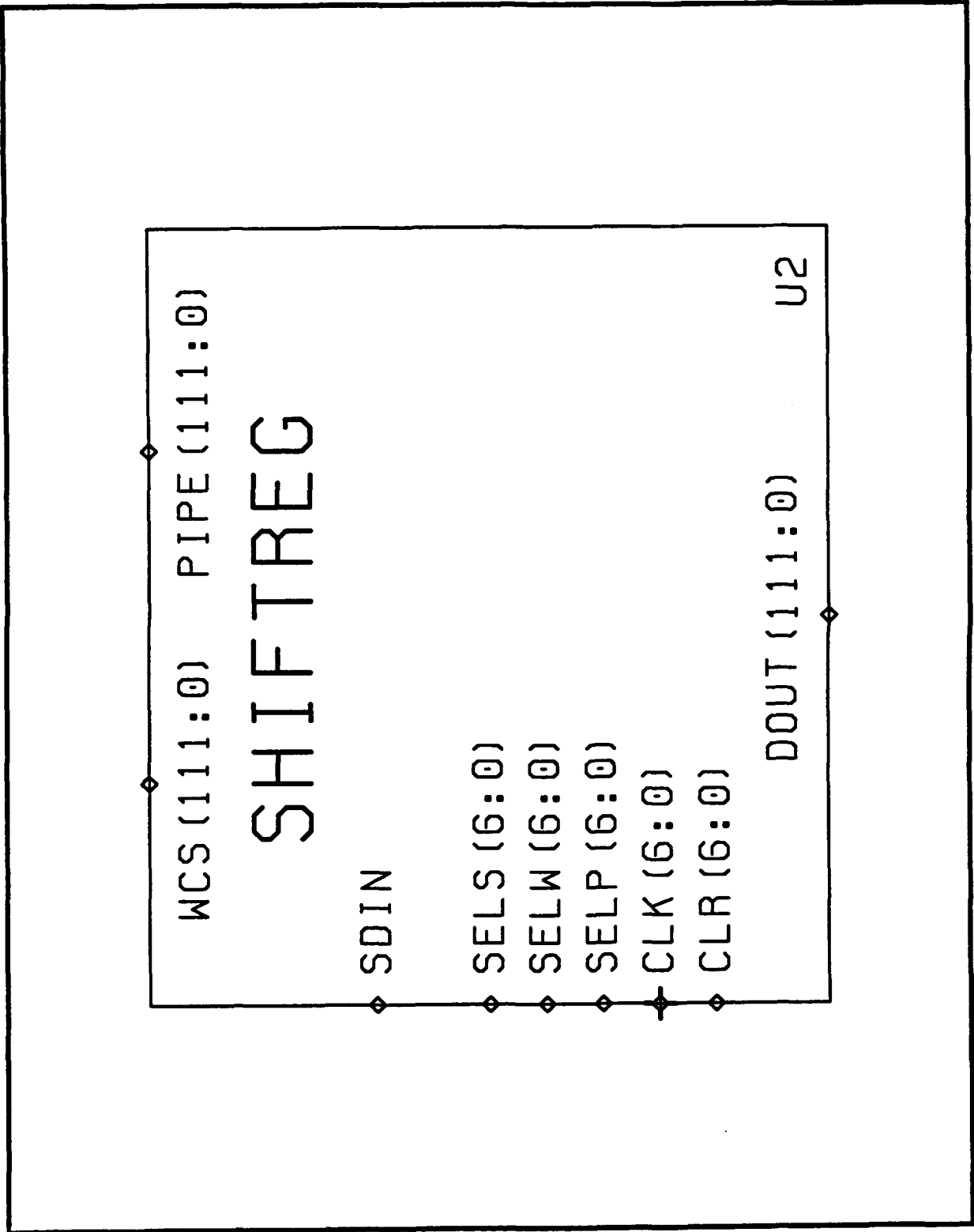
RCVR2  
Revised 8/24/88

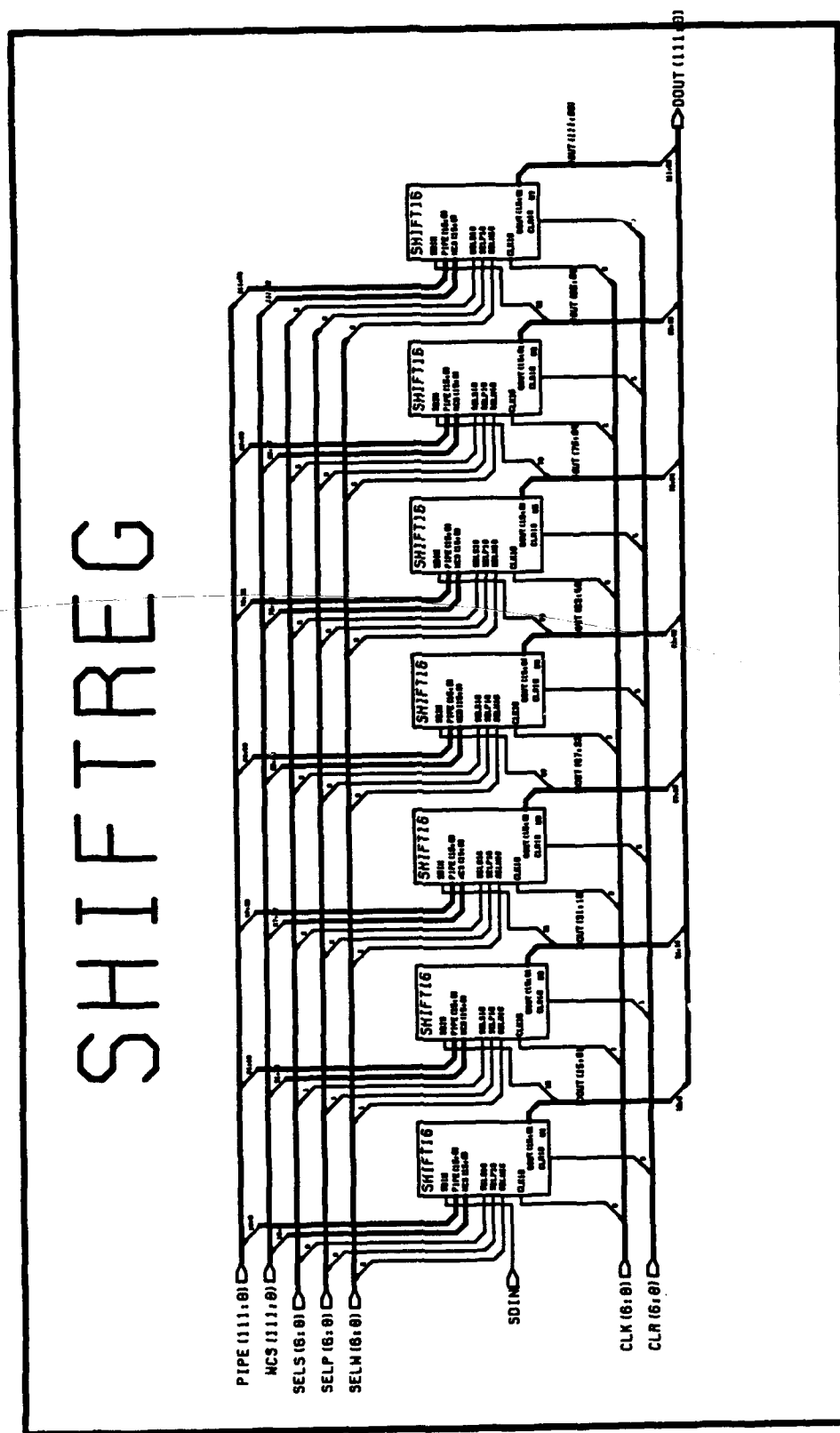


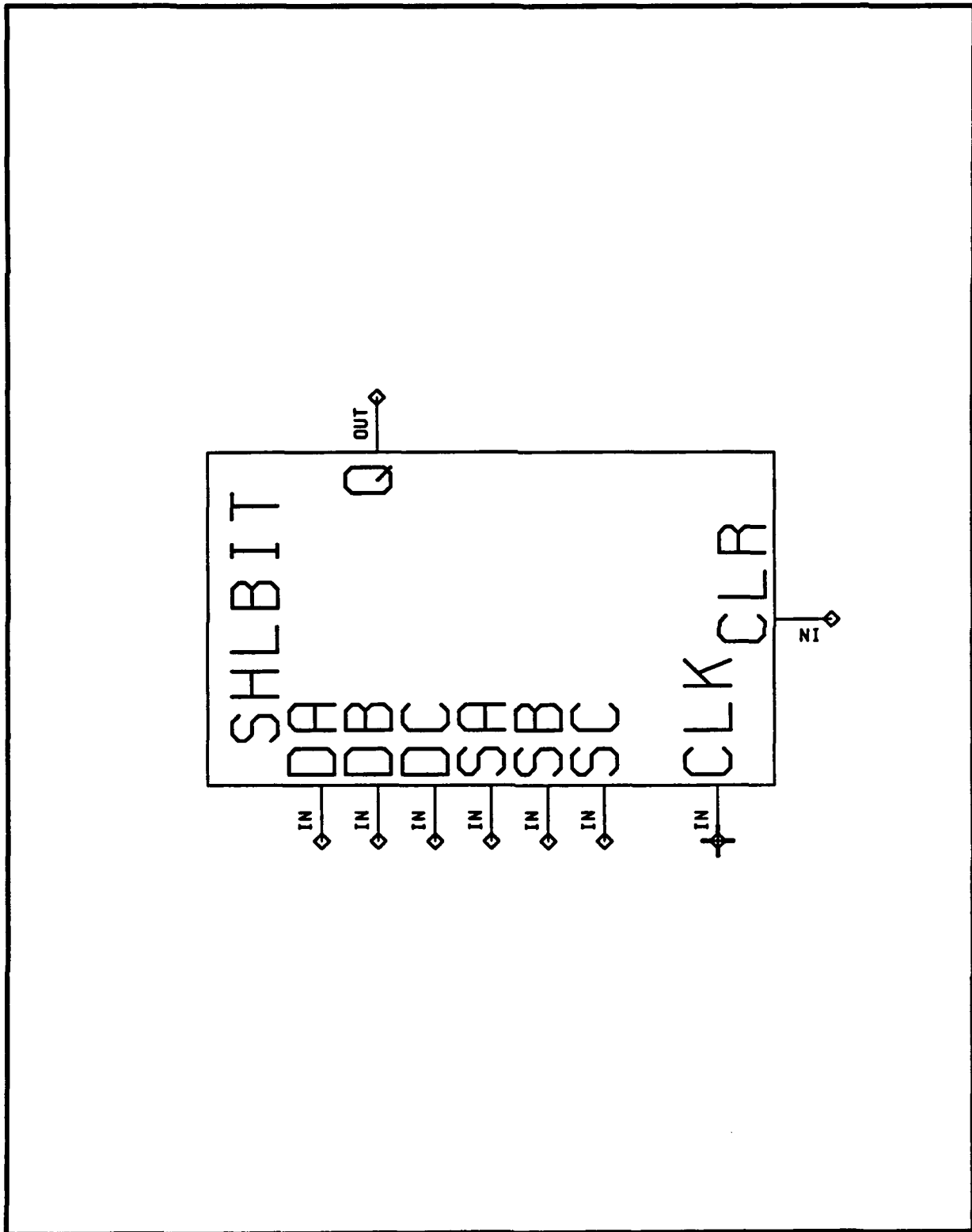




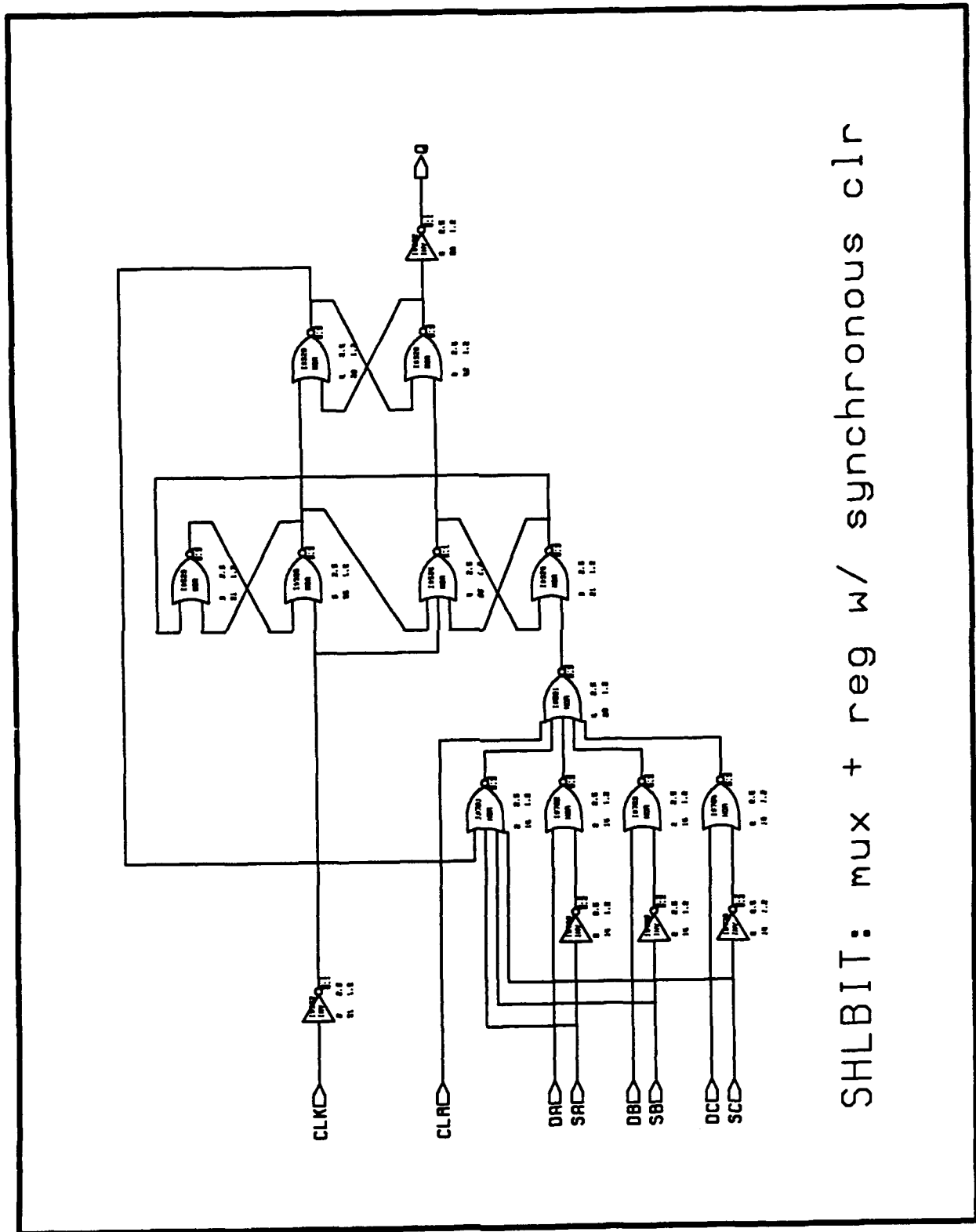


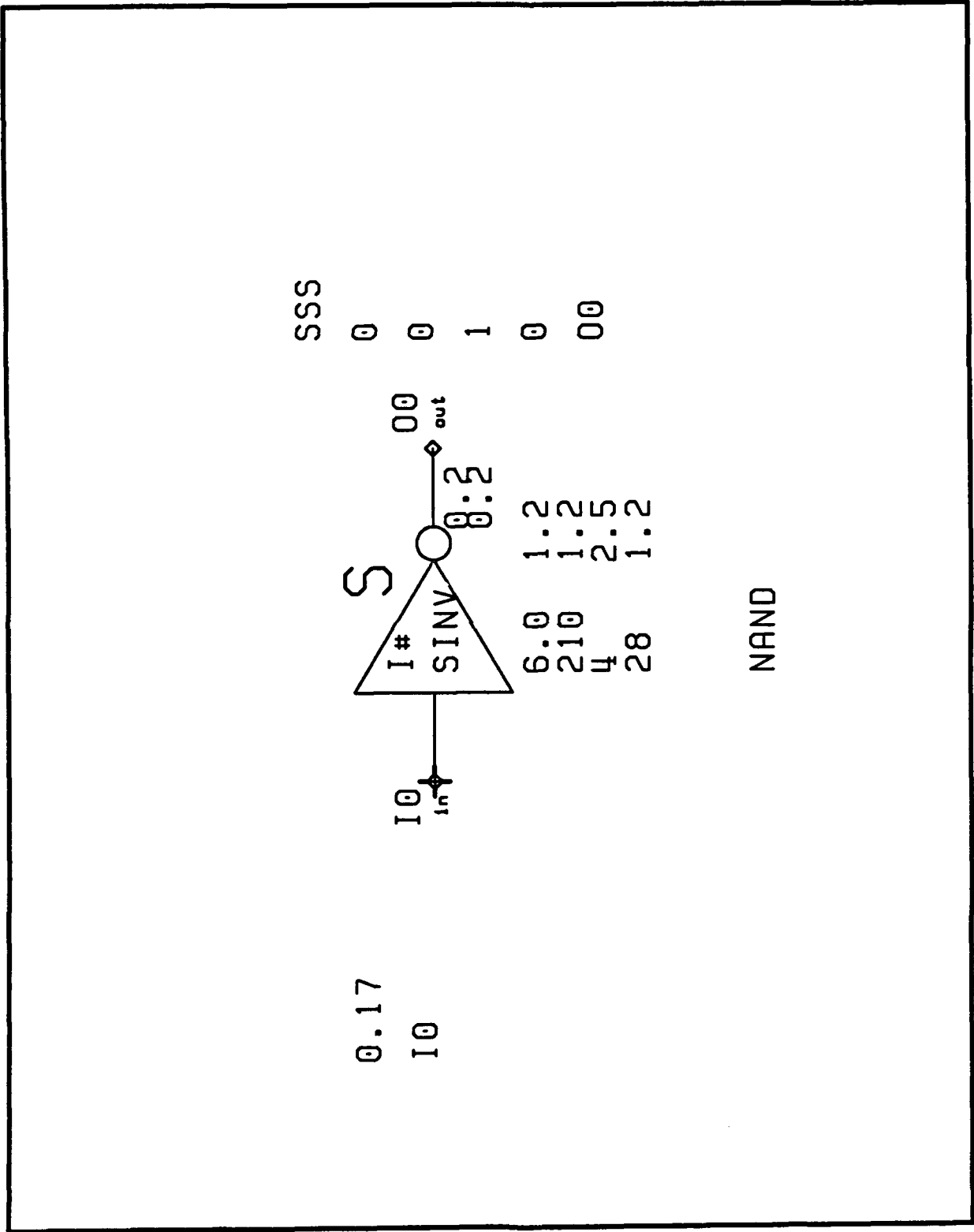


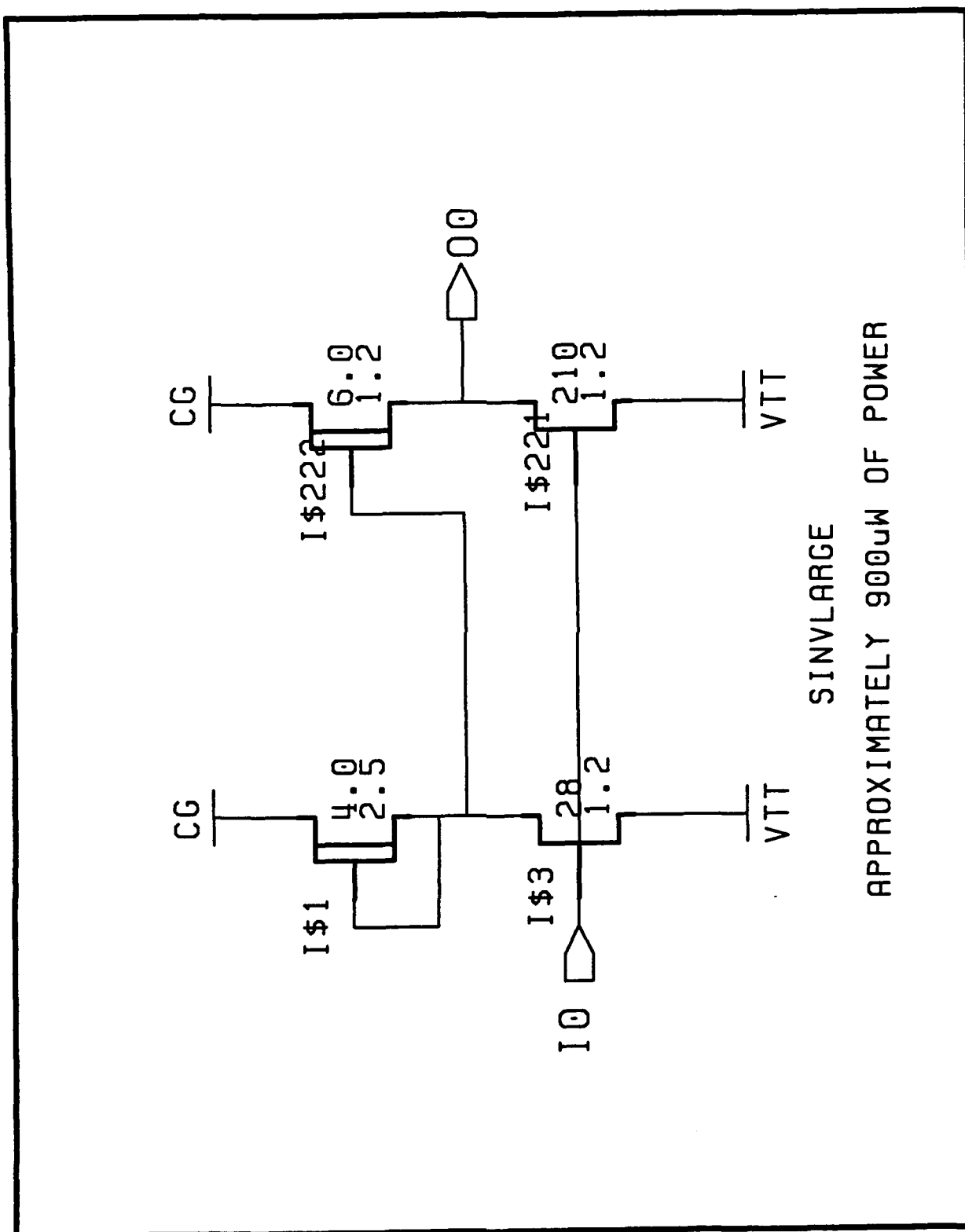


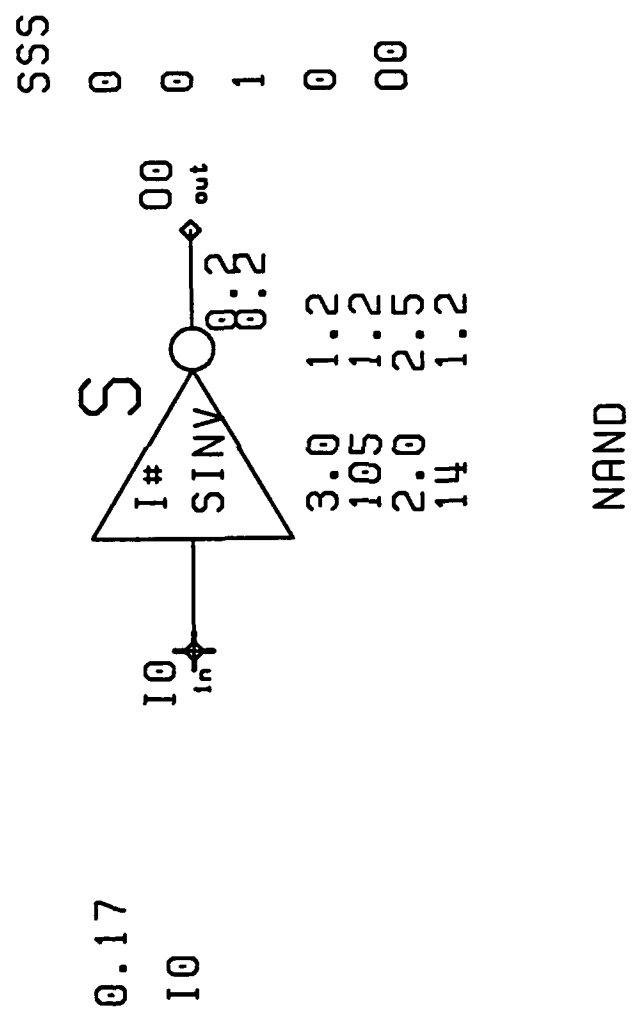


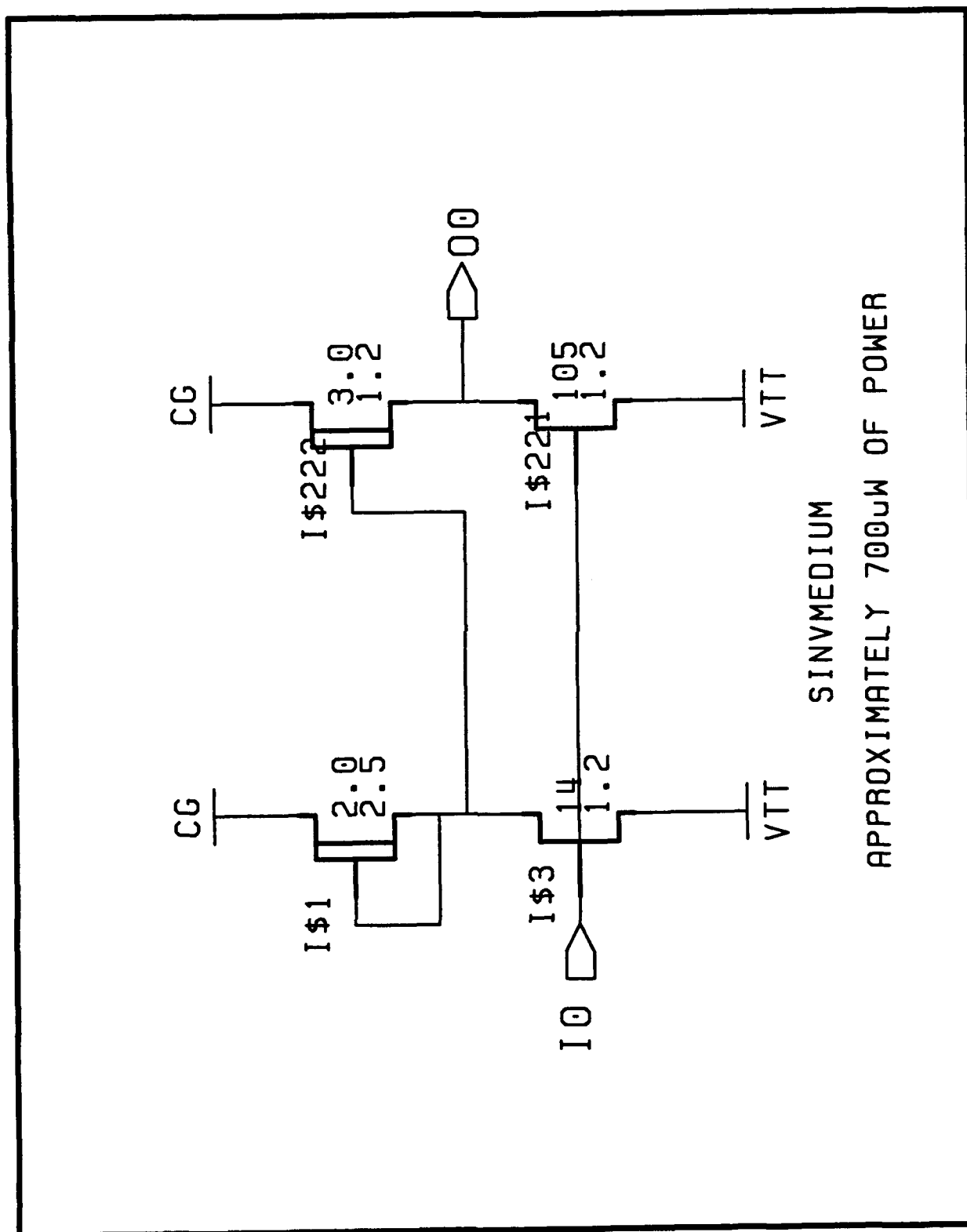


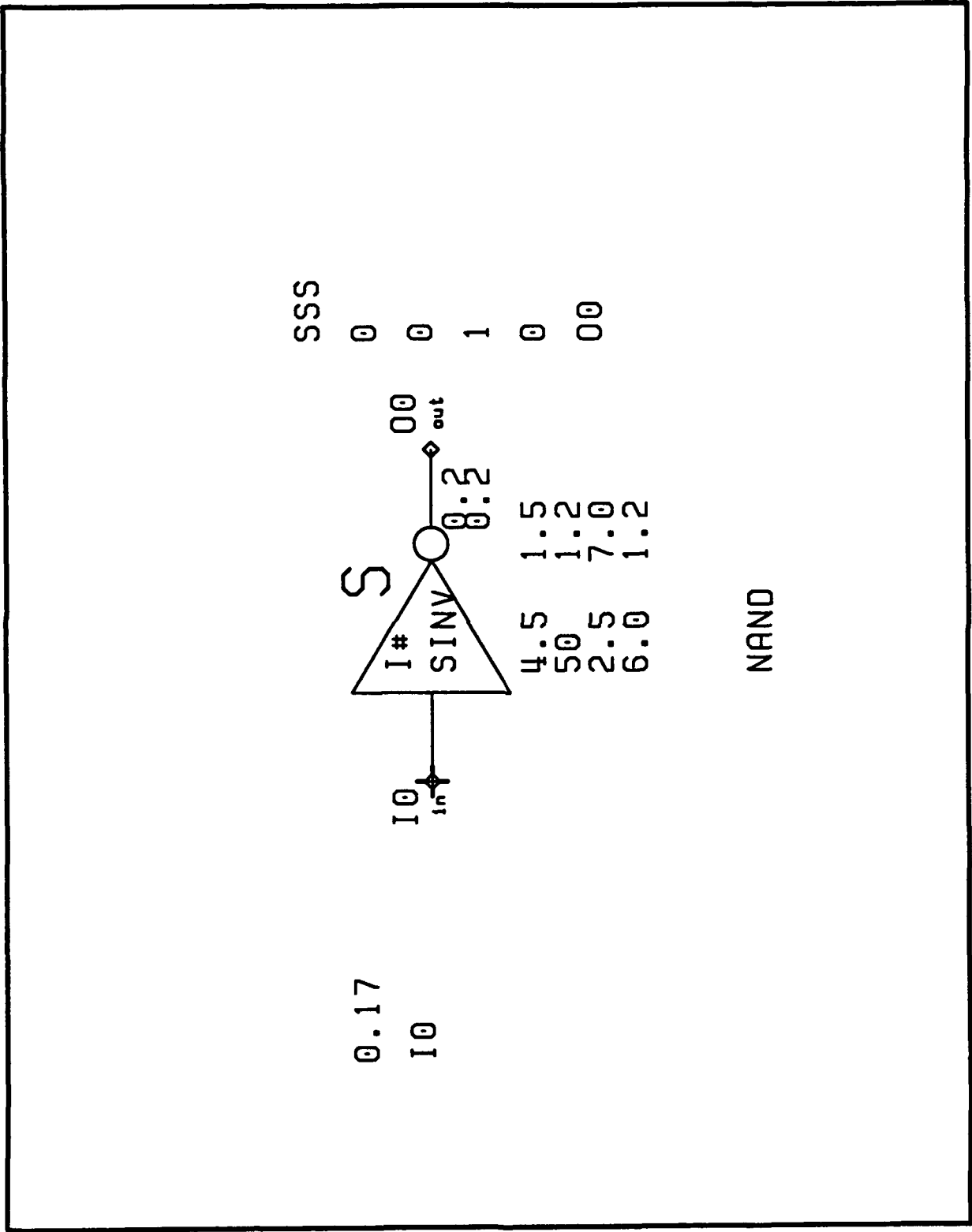


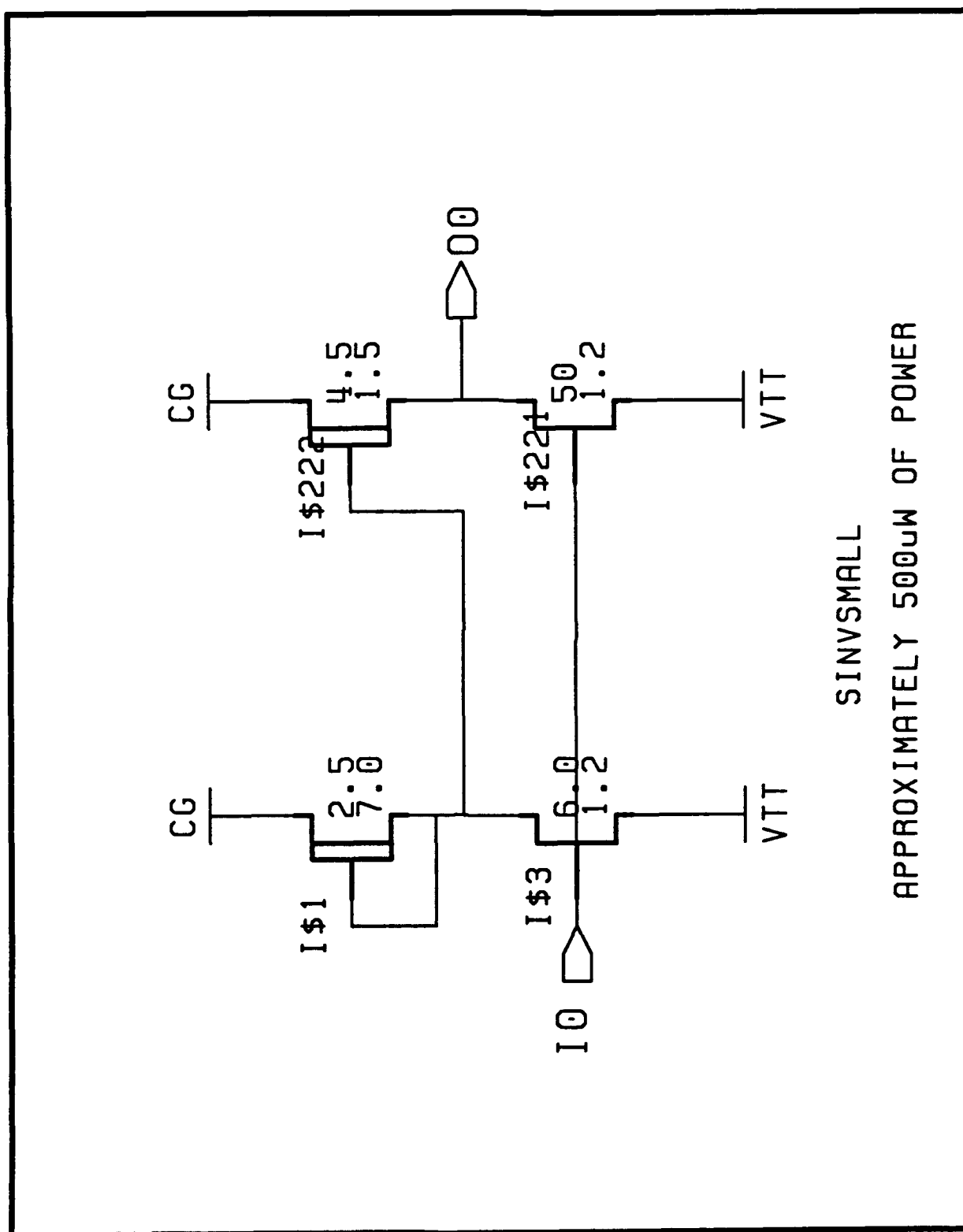


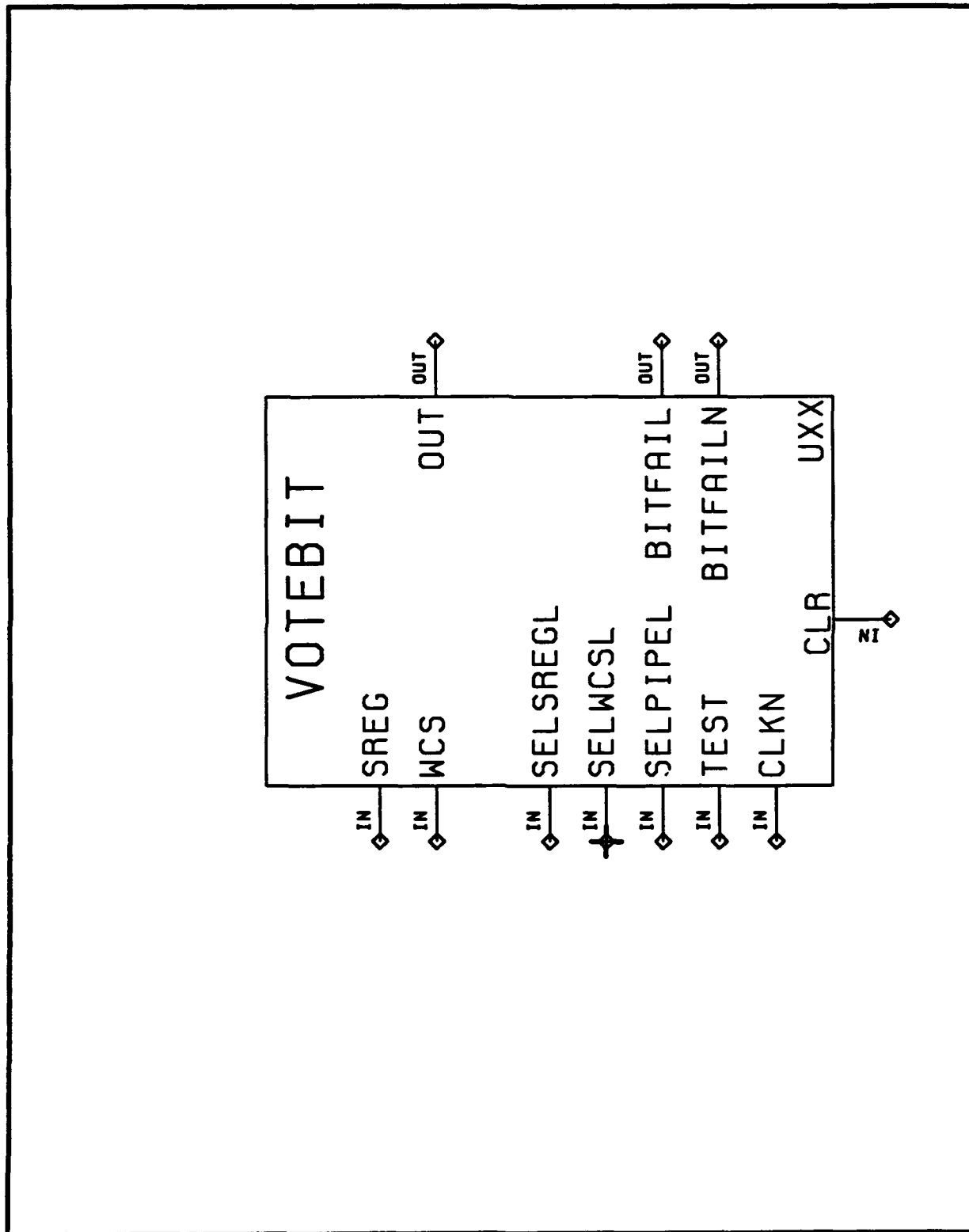




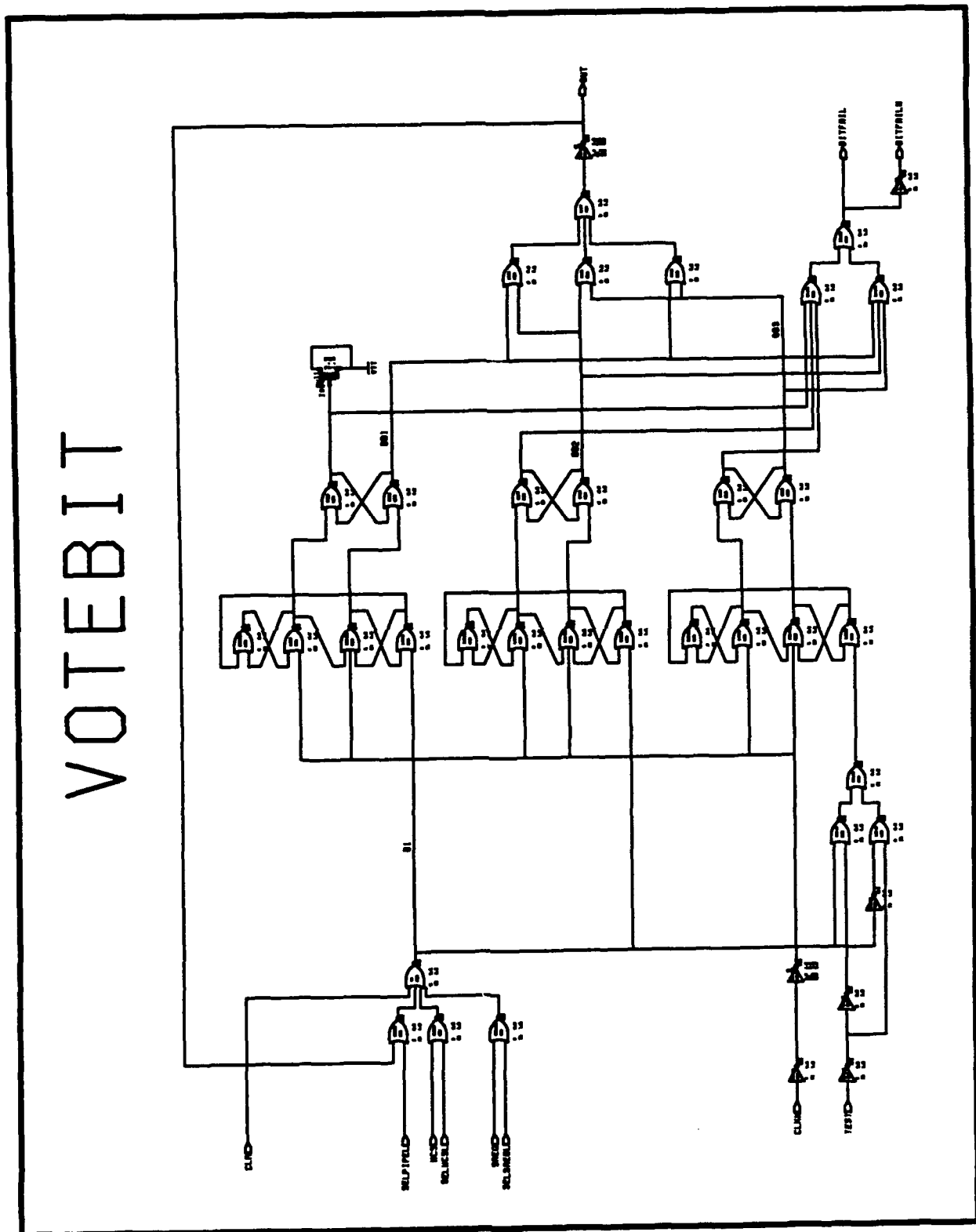


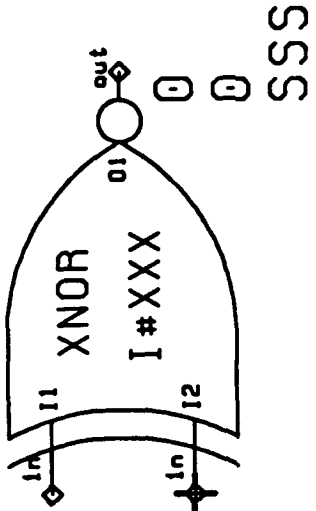


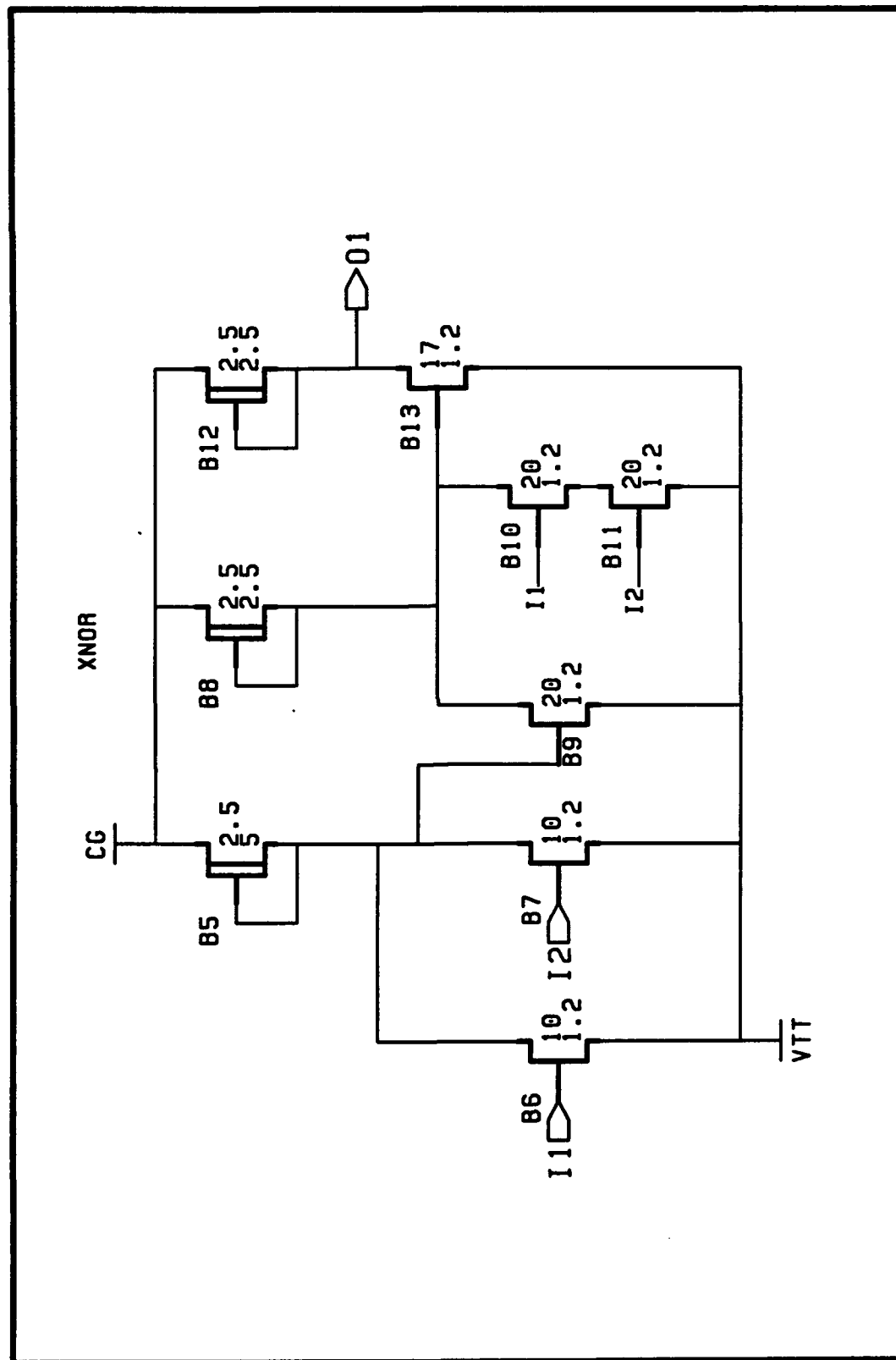


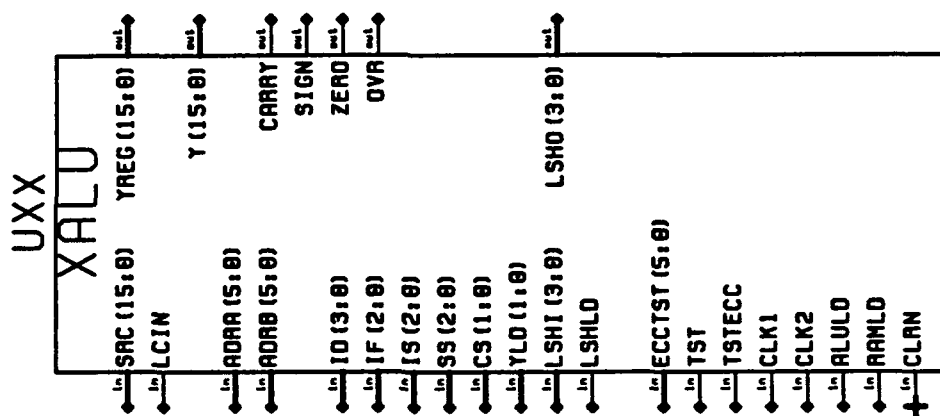




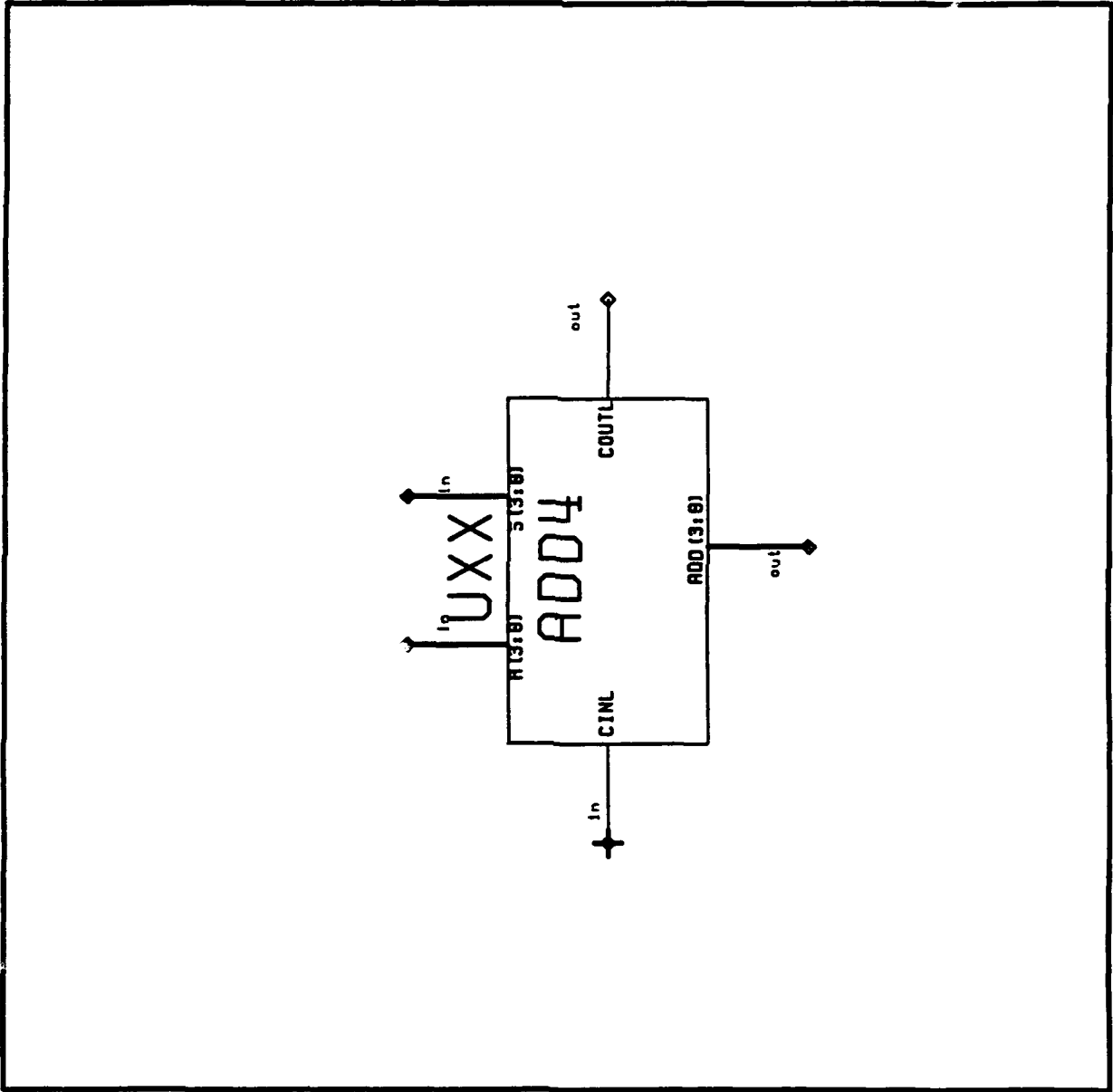


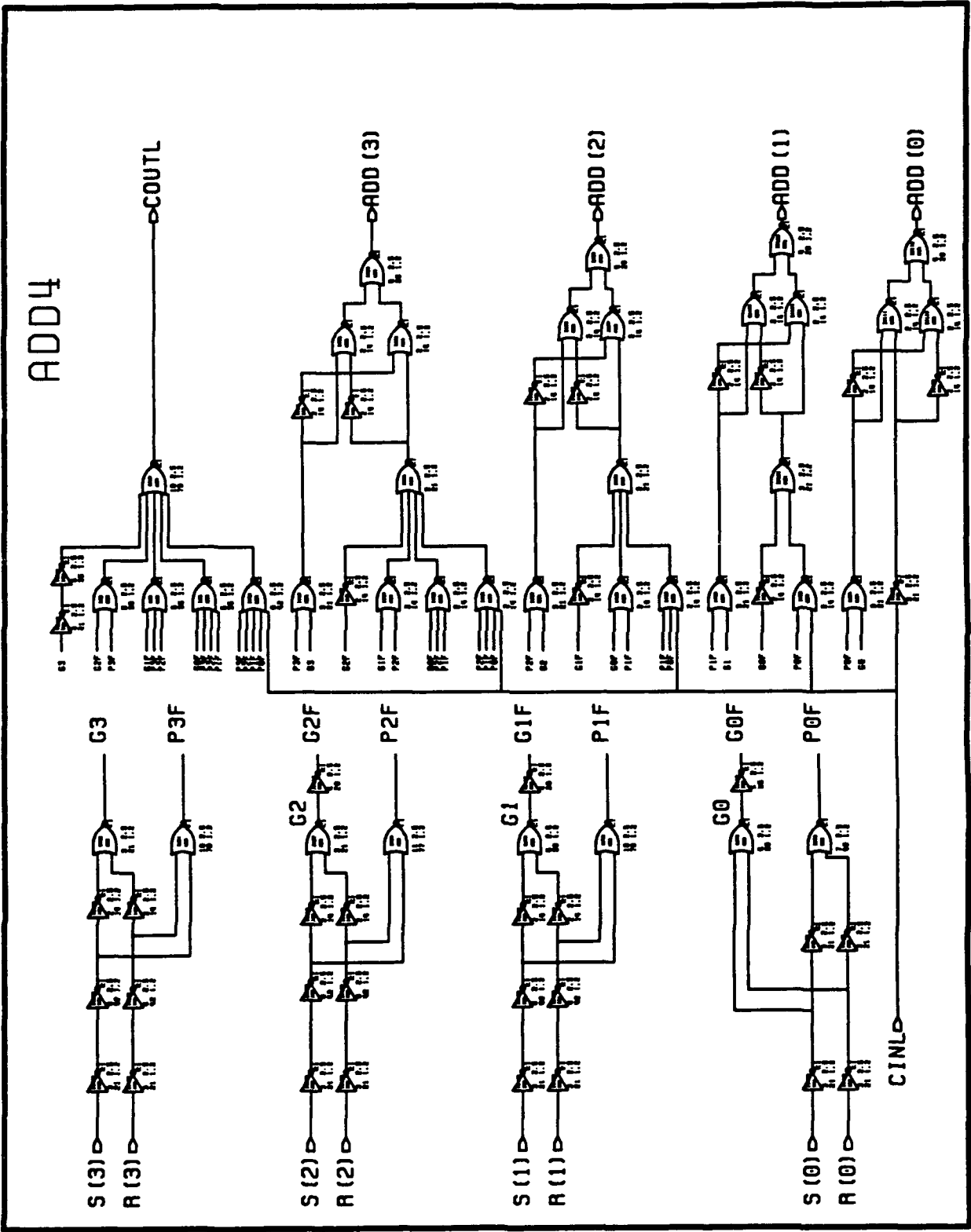


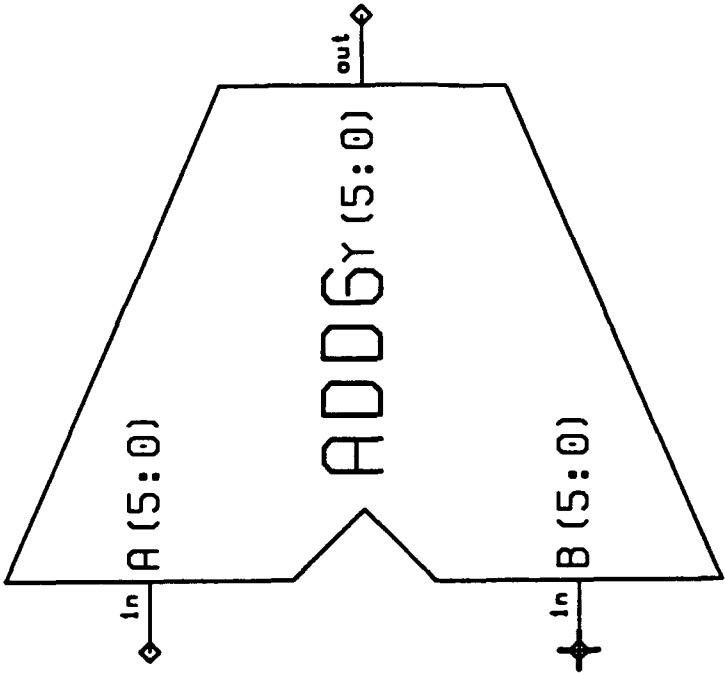




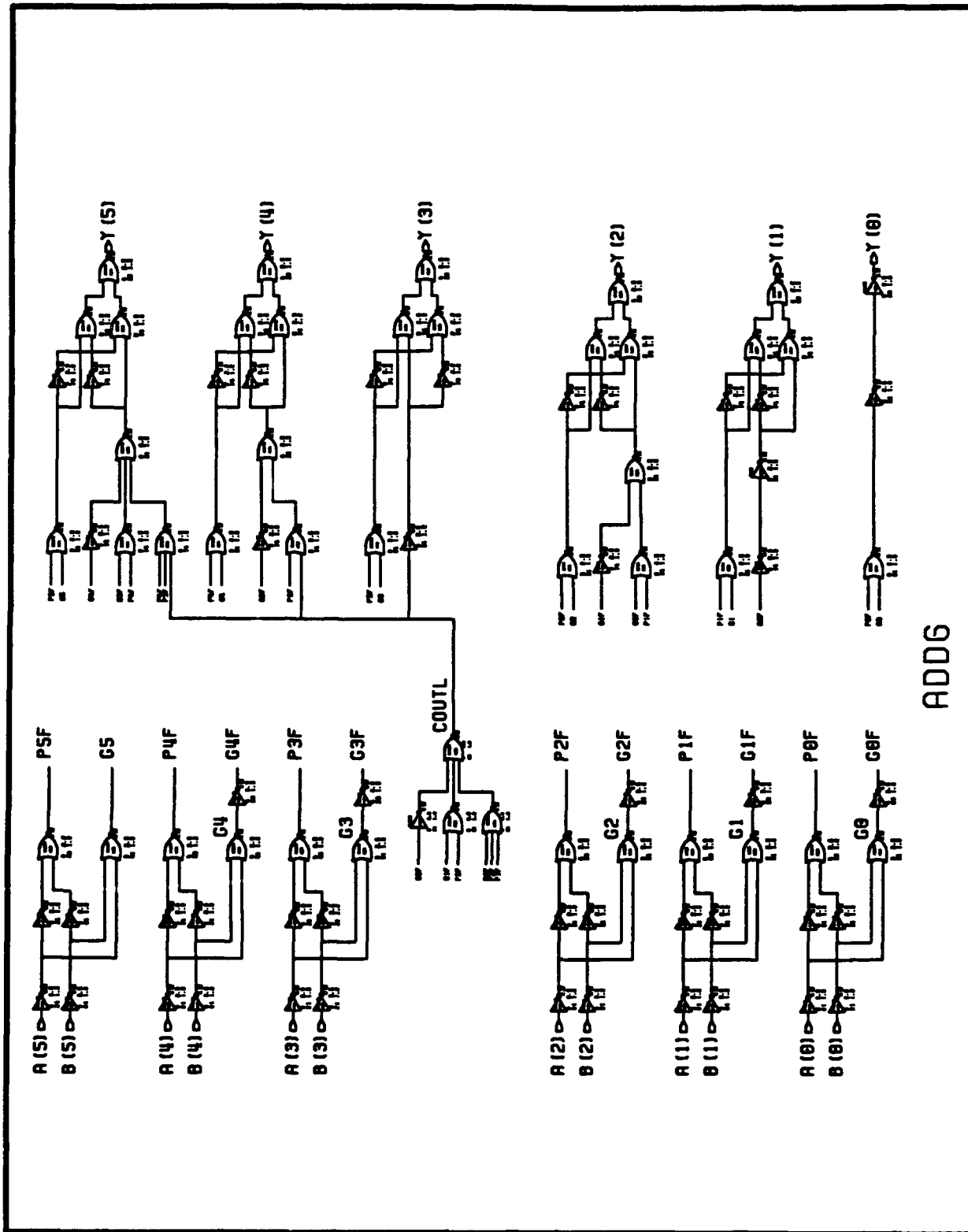


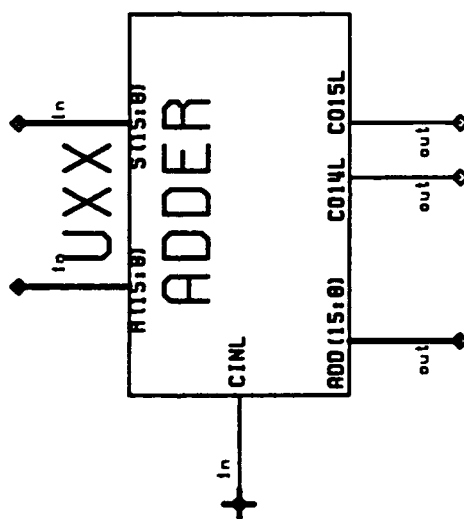


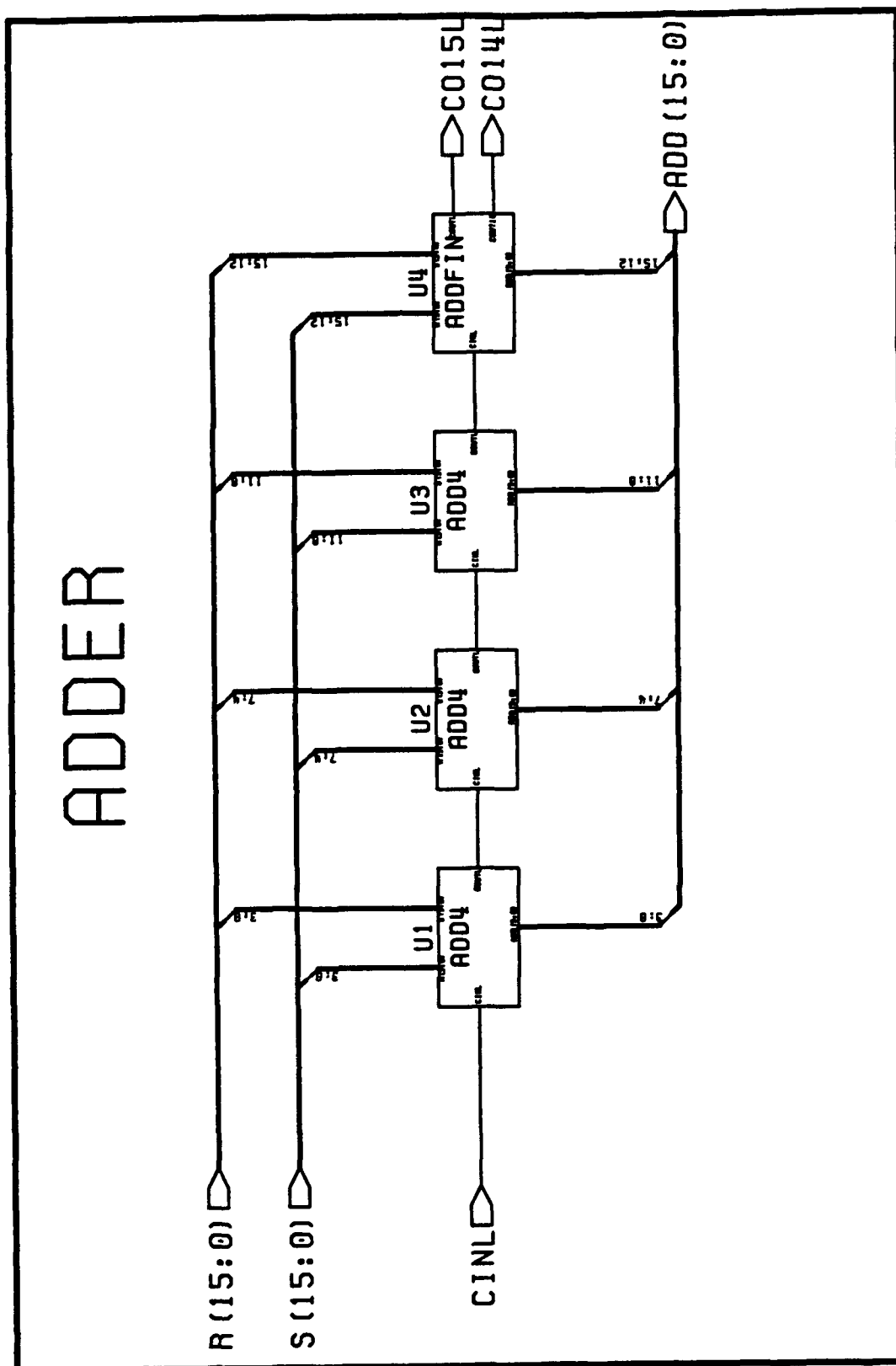


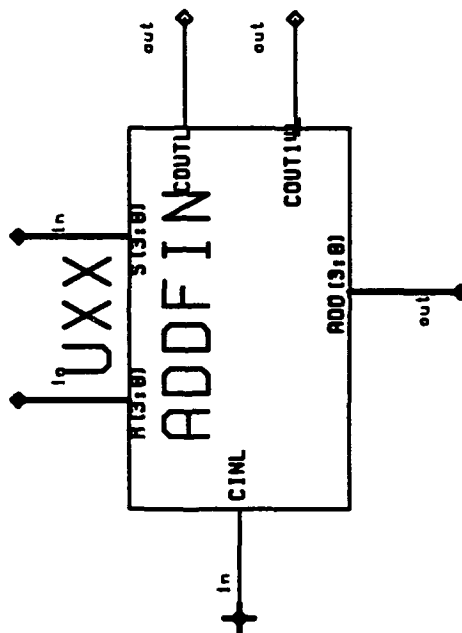


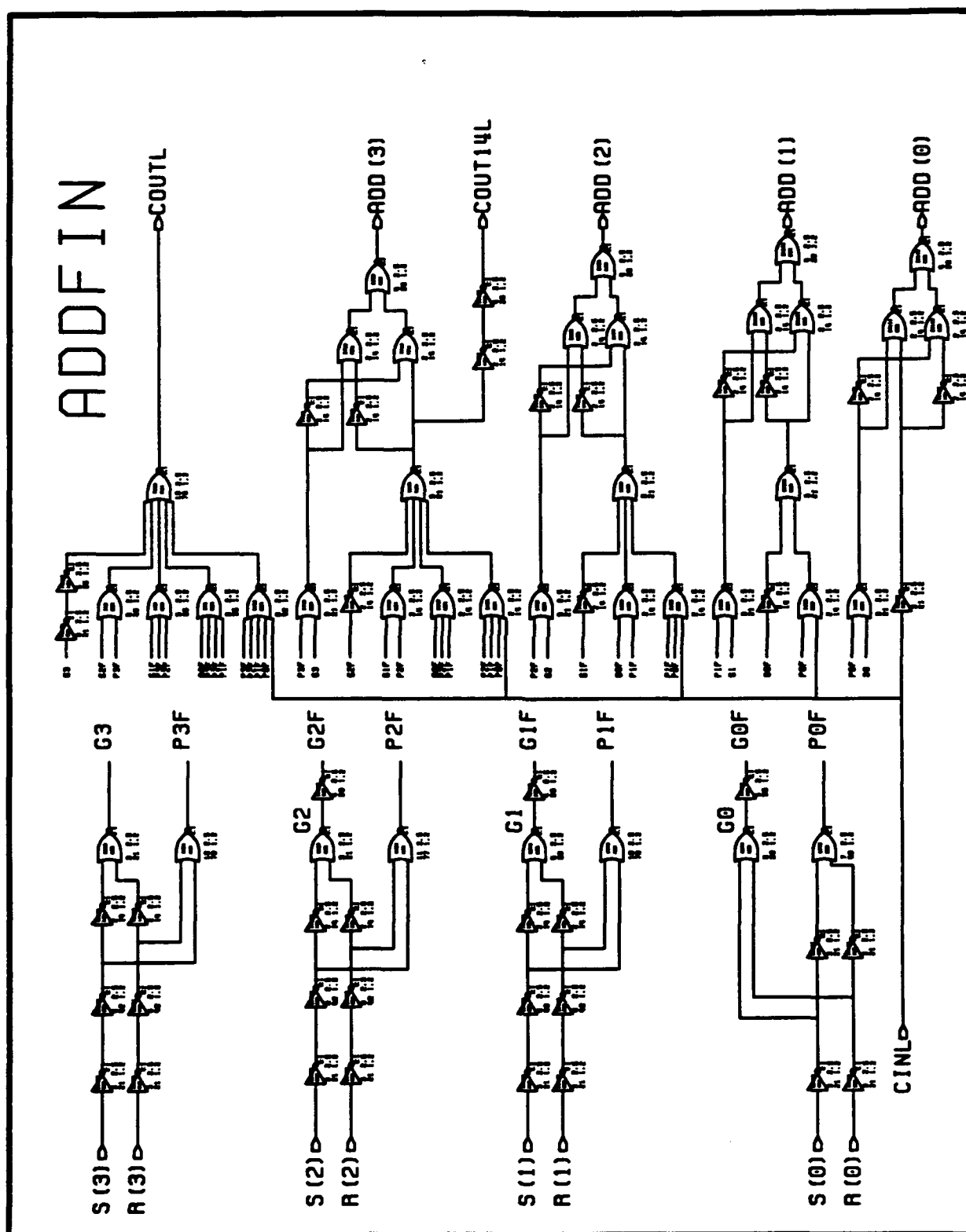


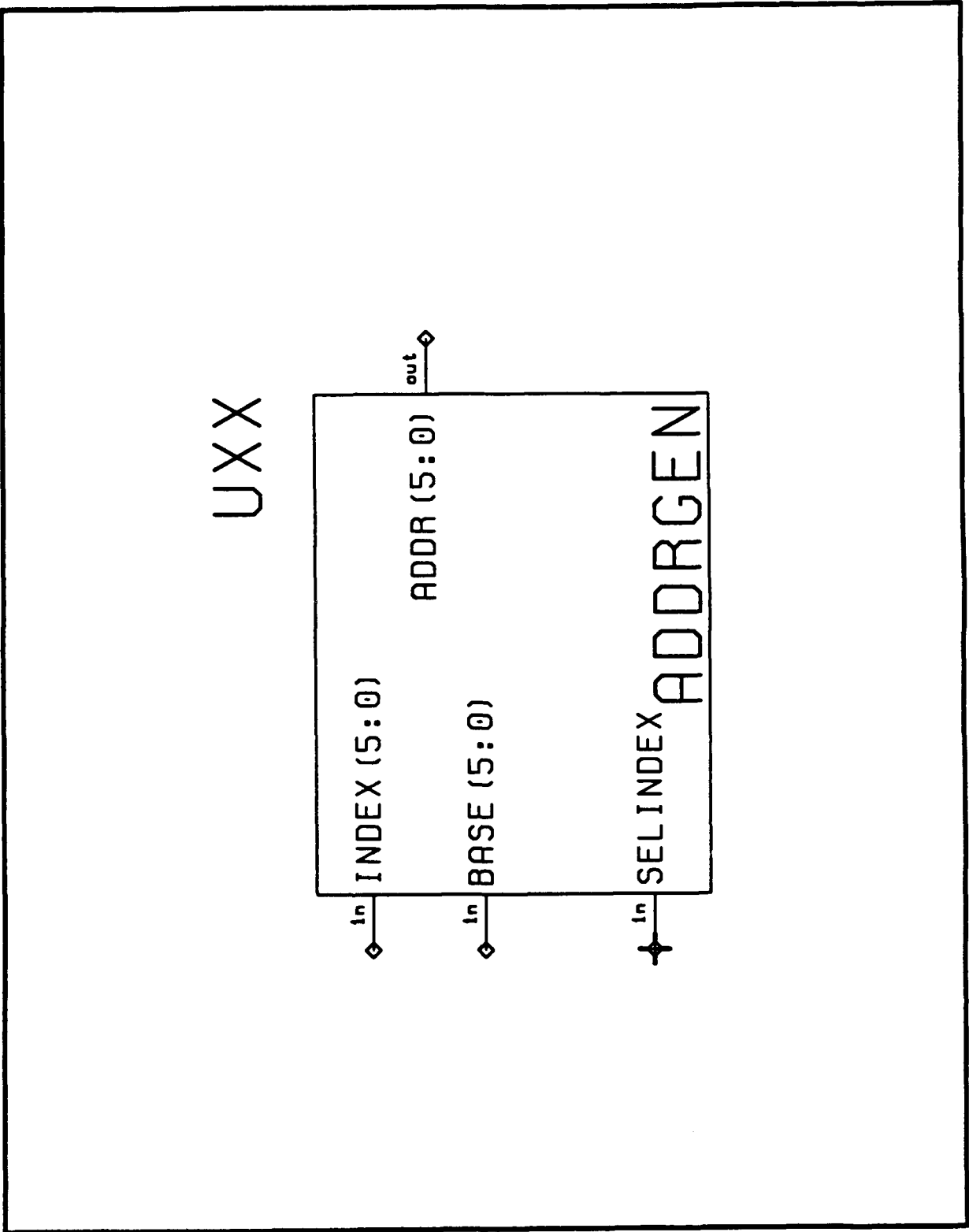


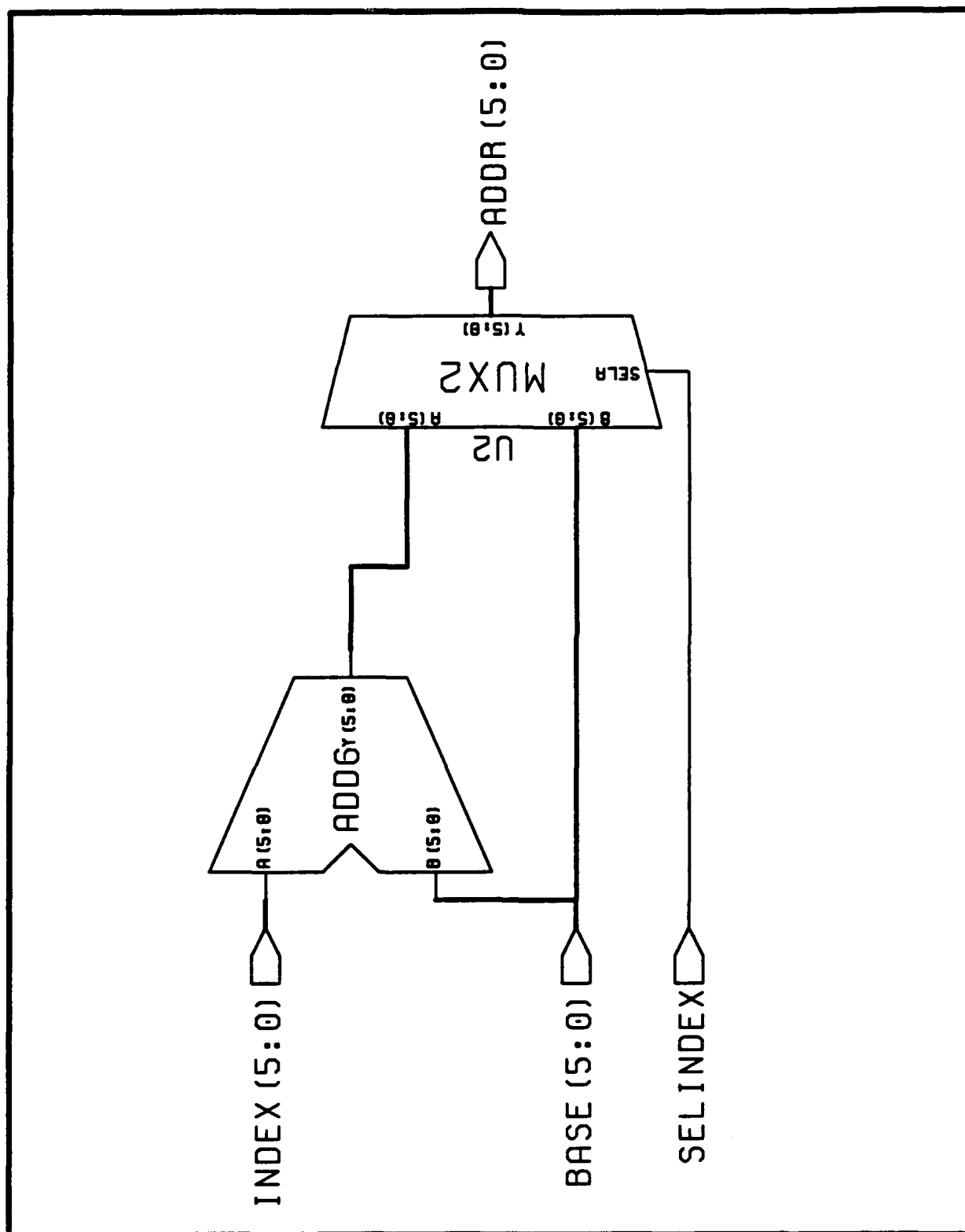


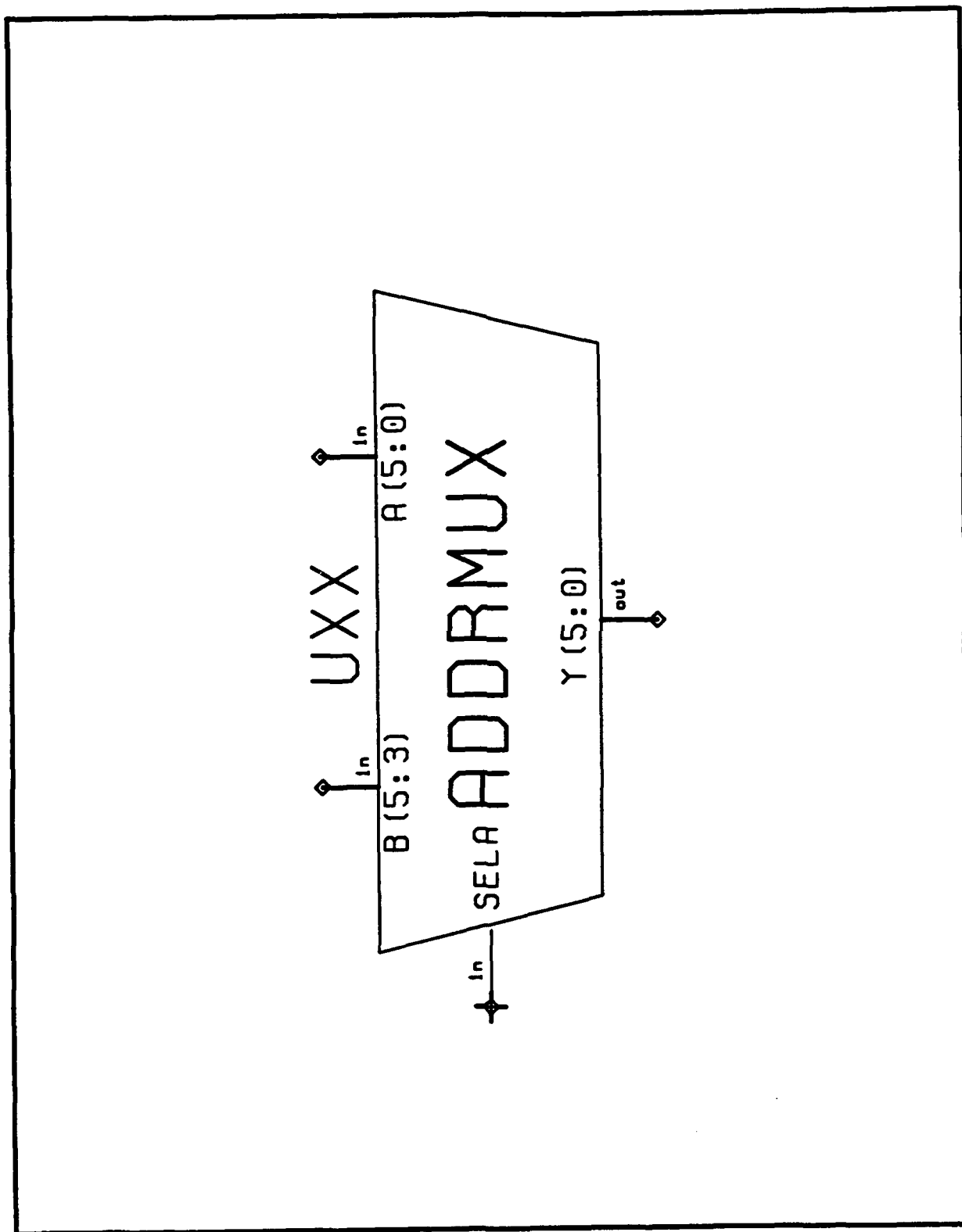






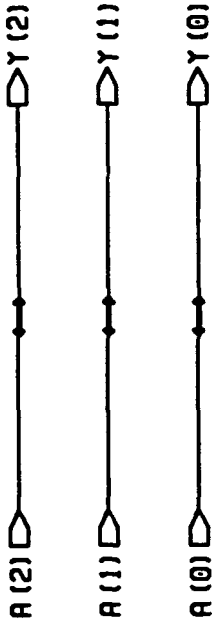
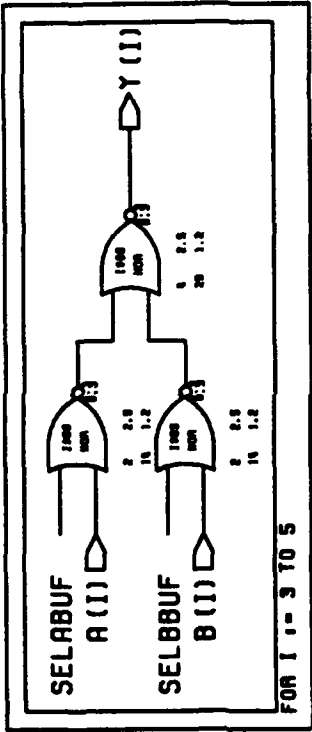
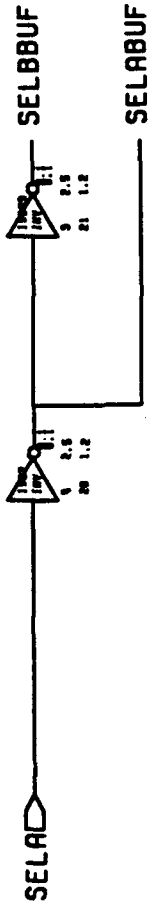


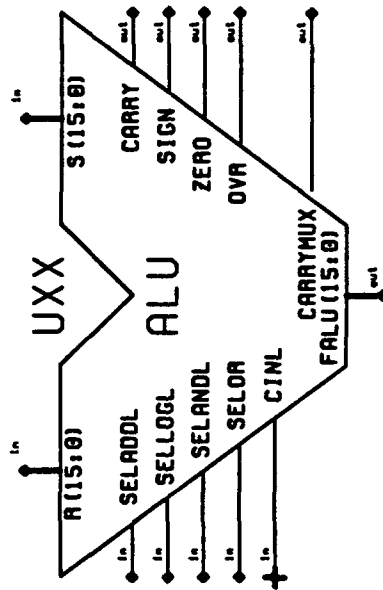


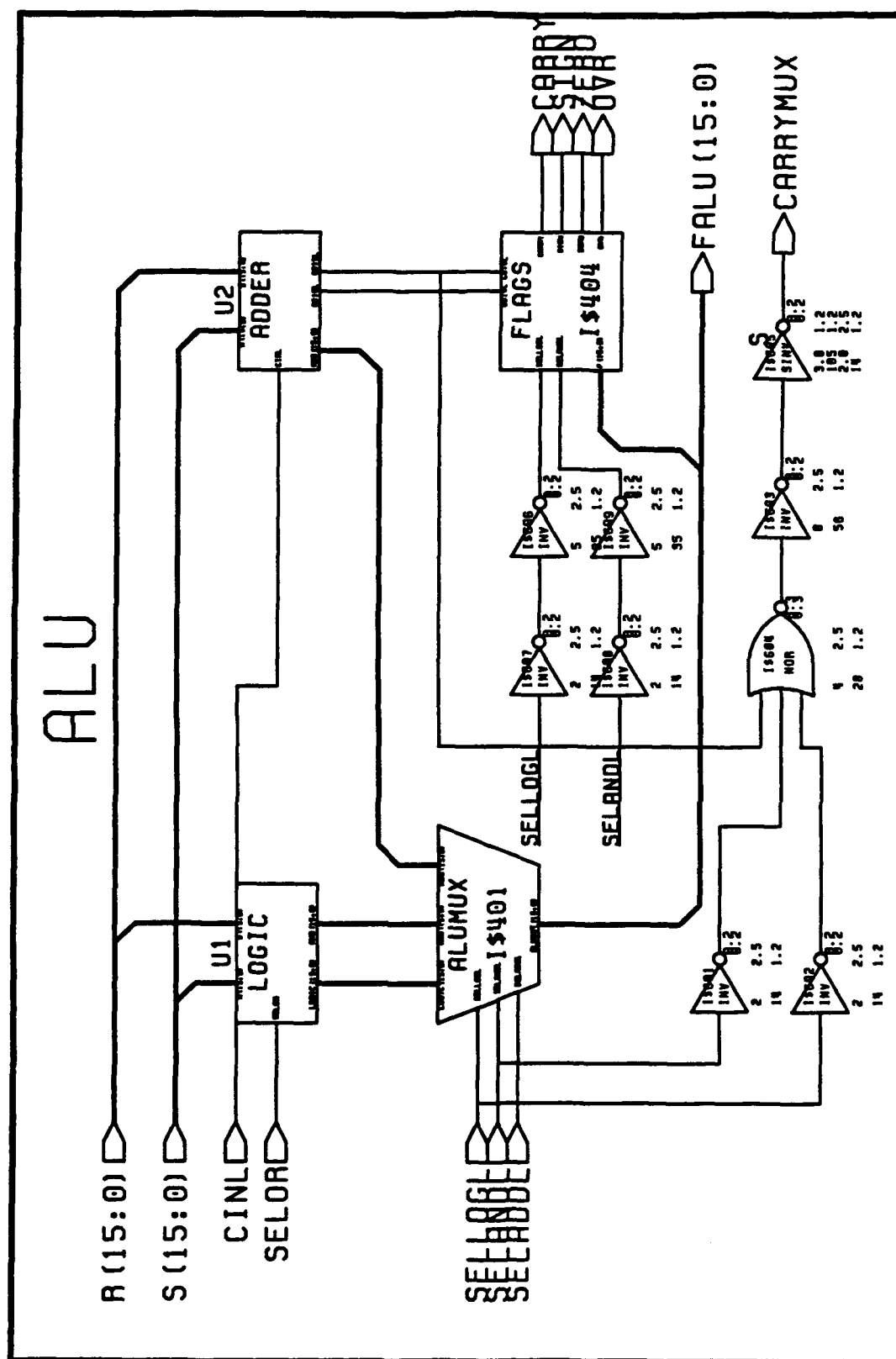


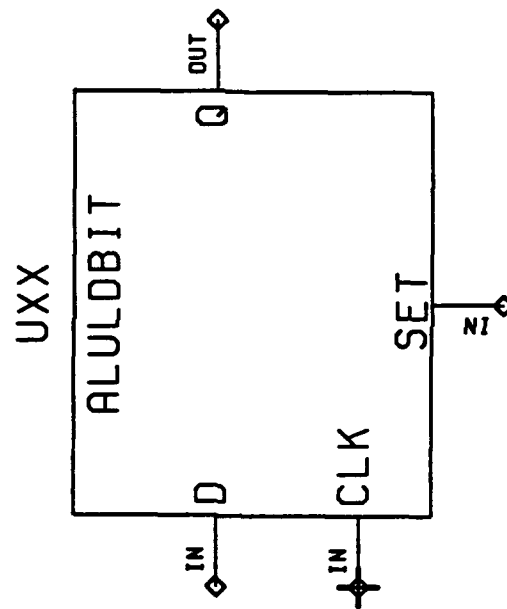


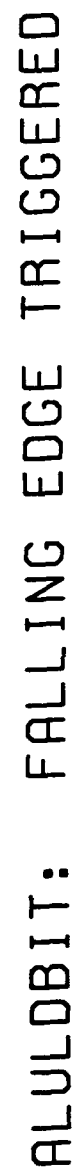
ADDRMUX

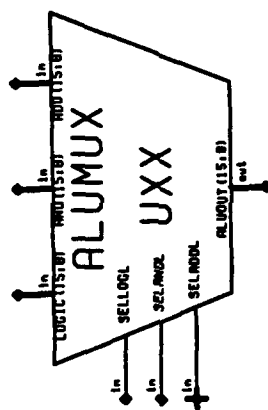


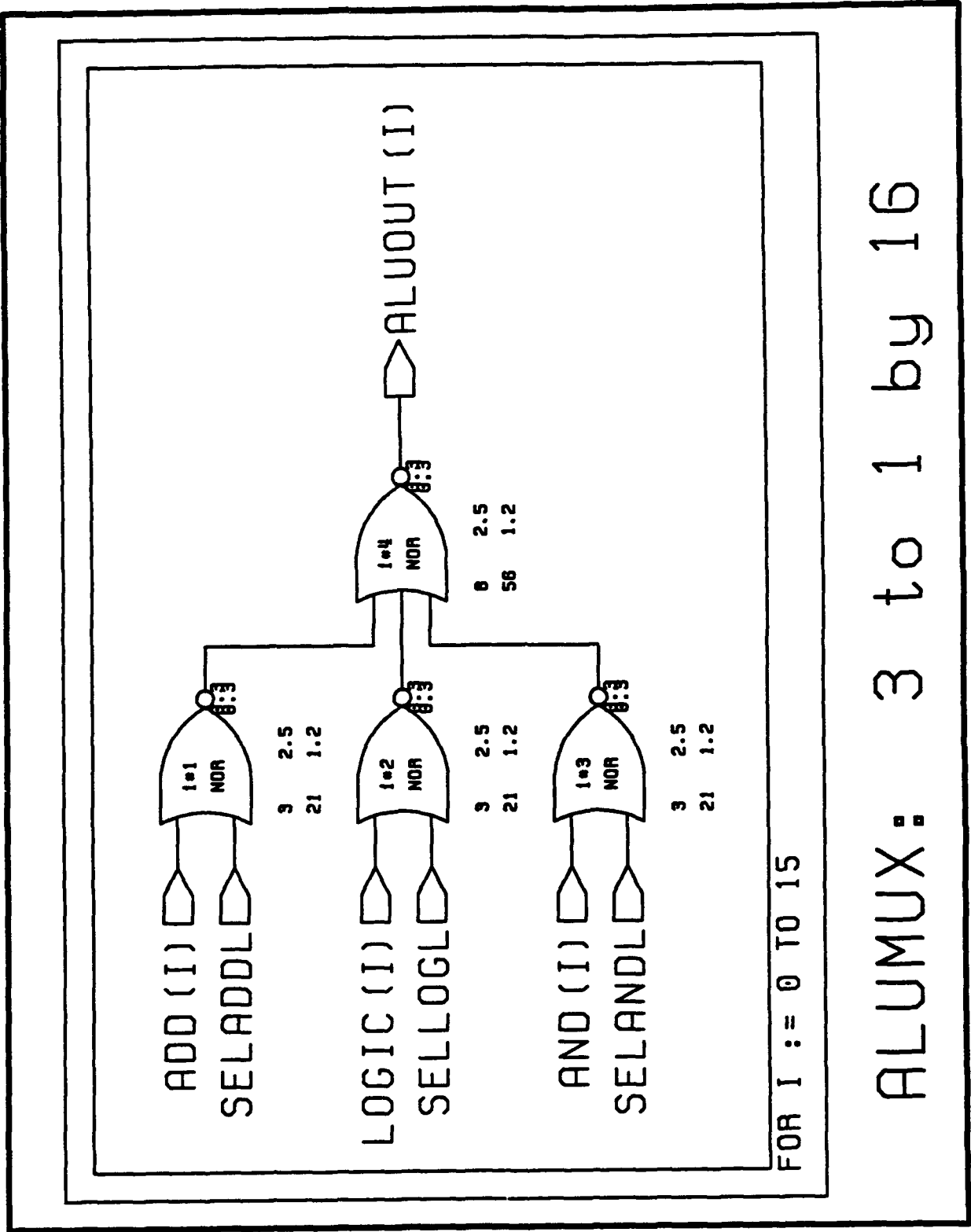


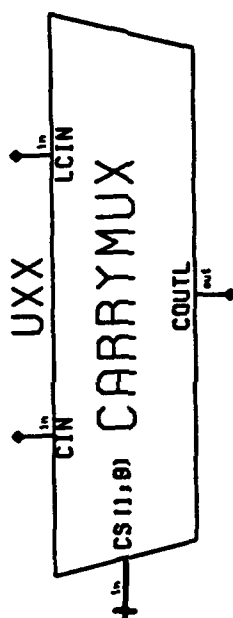




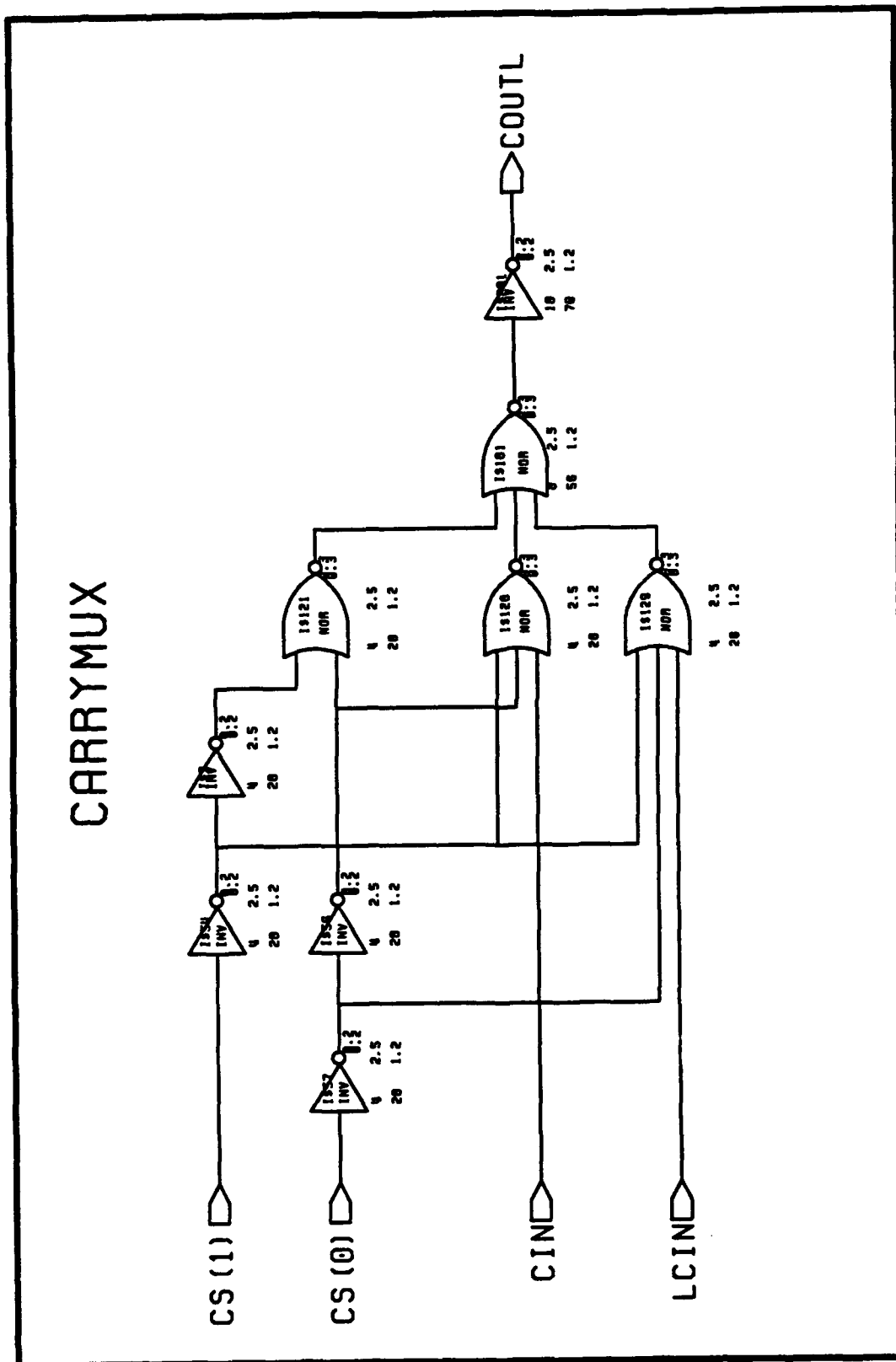






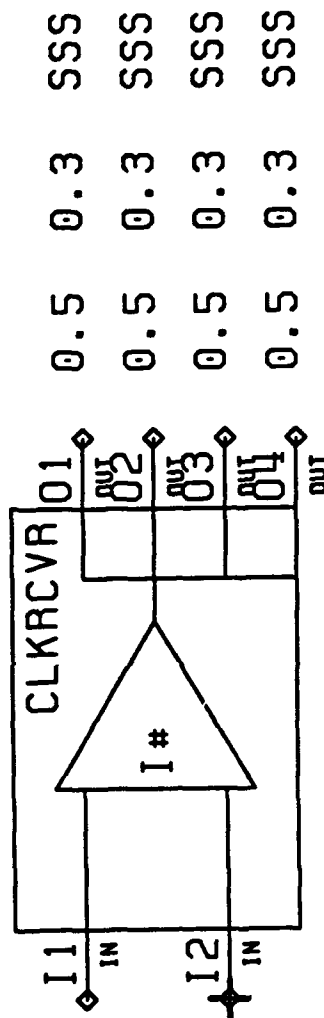






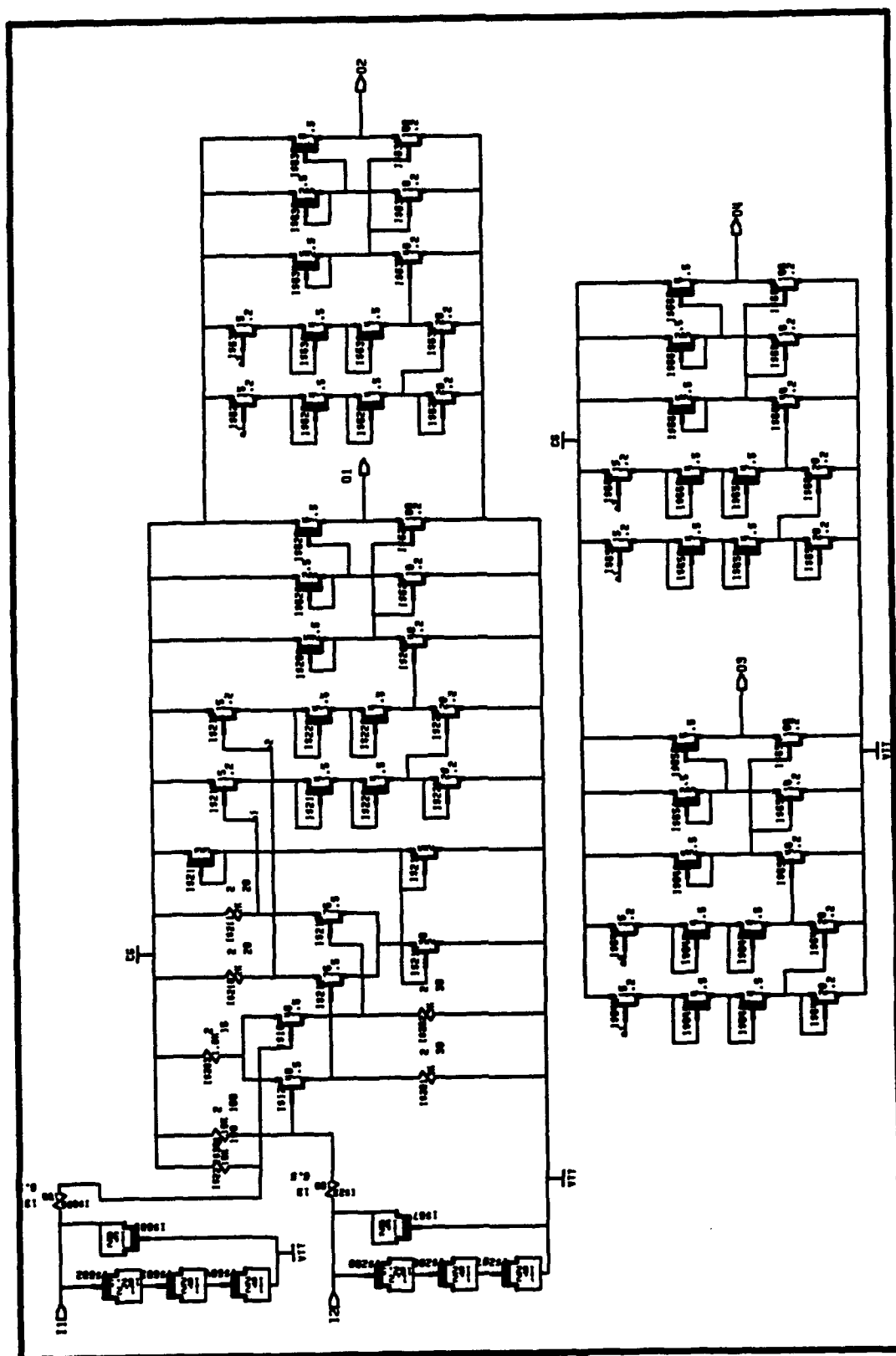
VITESSE GAAS CELL LIBRARY  
Version 0.8

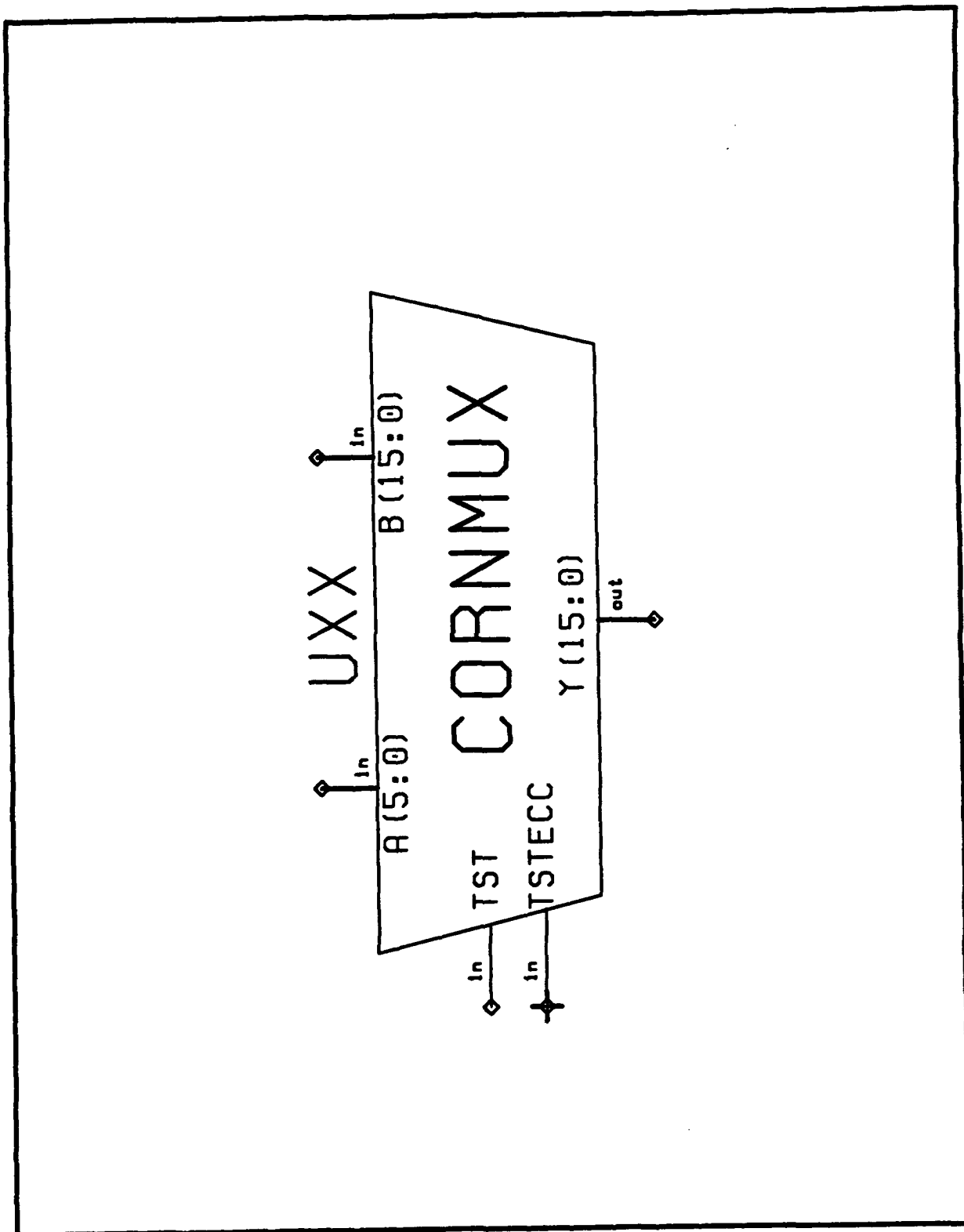
NAME: CLKRCVR  
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER



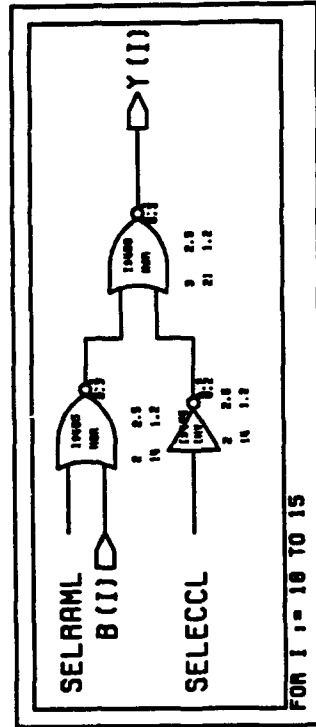
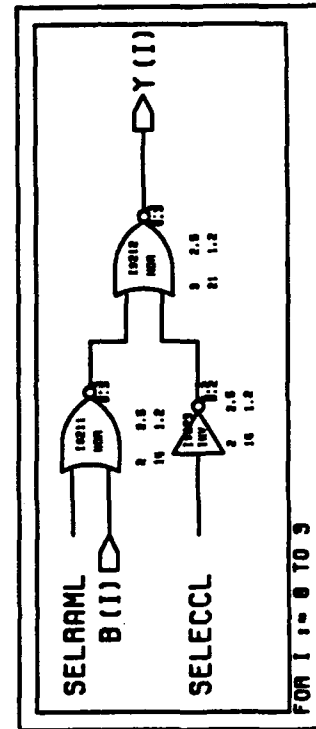
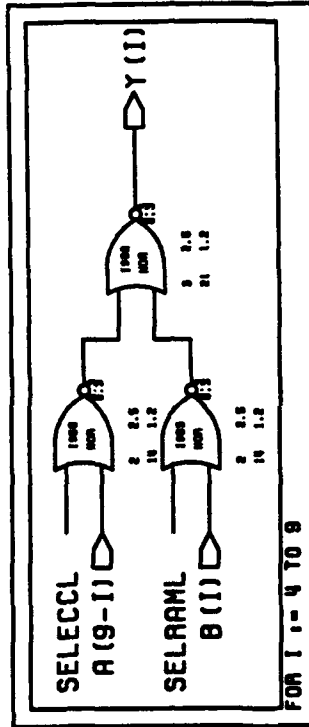
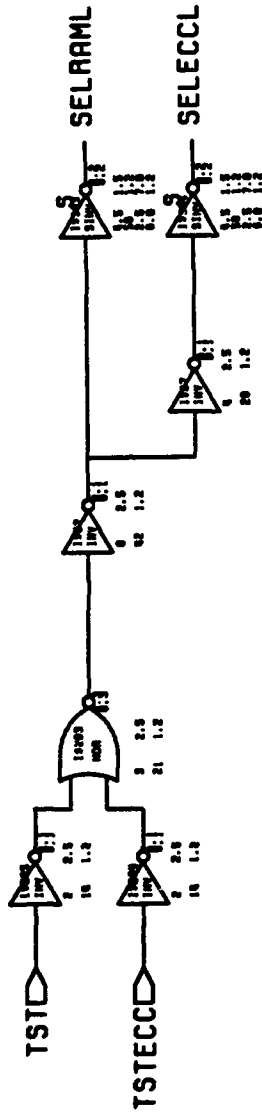
0.5	0.3	SSS
0.5	0.3	SSS
0.5	0.3	SSS
0.5	0.3	SSS

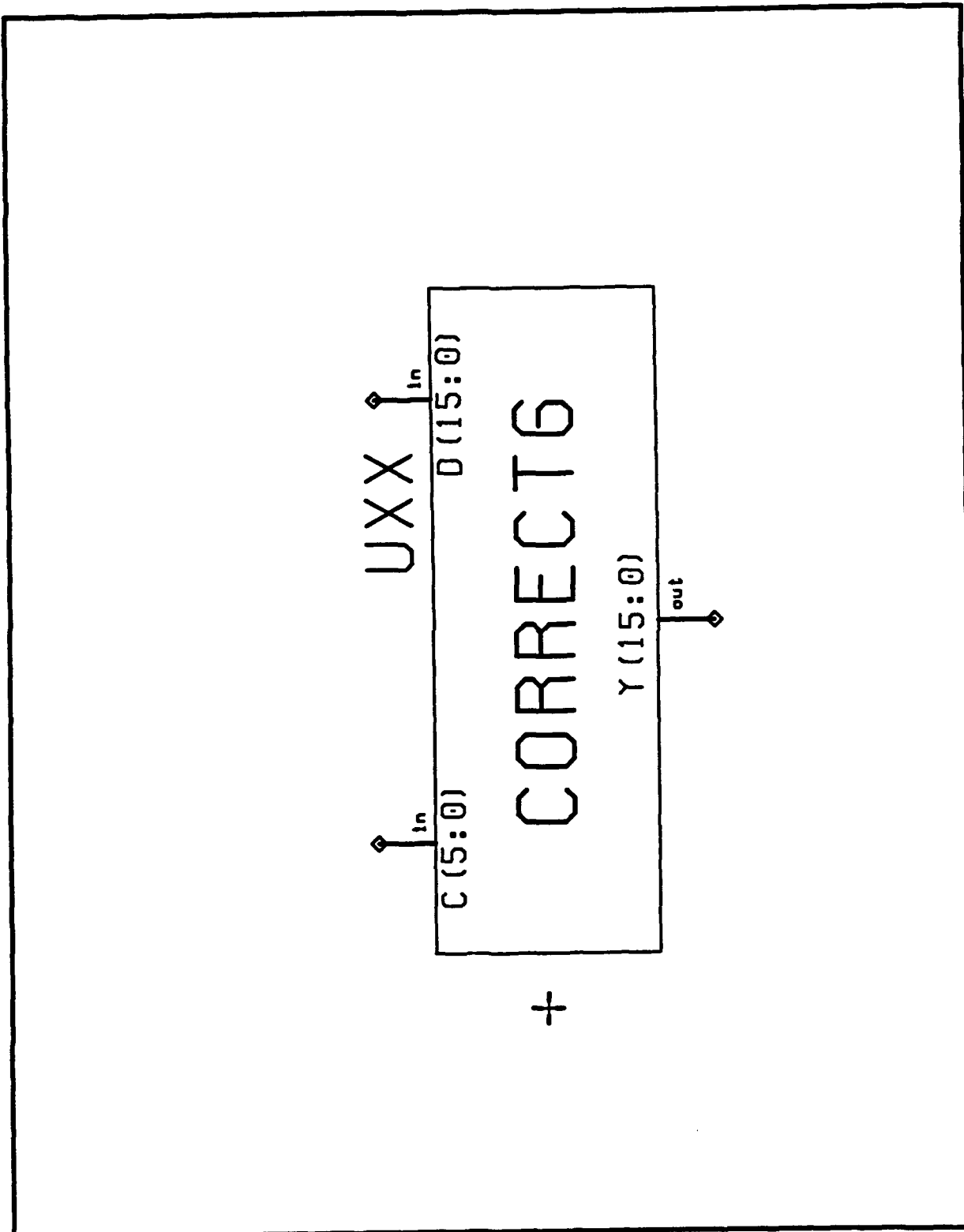
CLKRCVR  
clkrcvr.bin

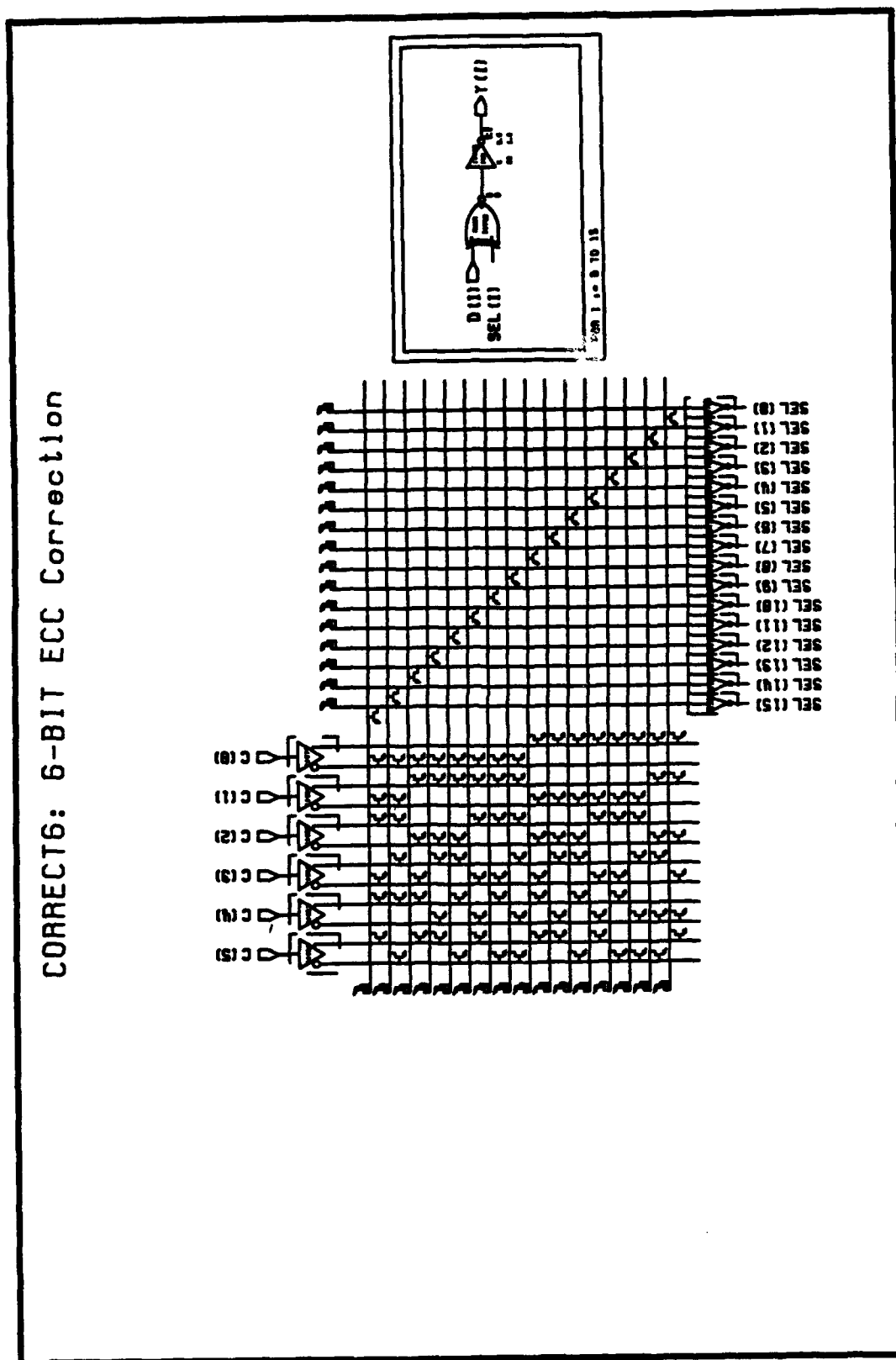


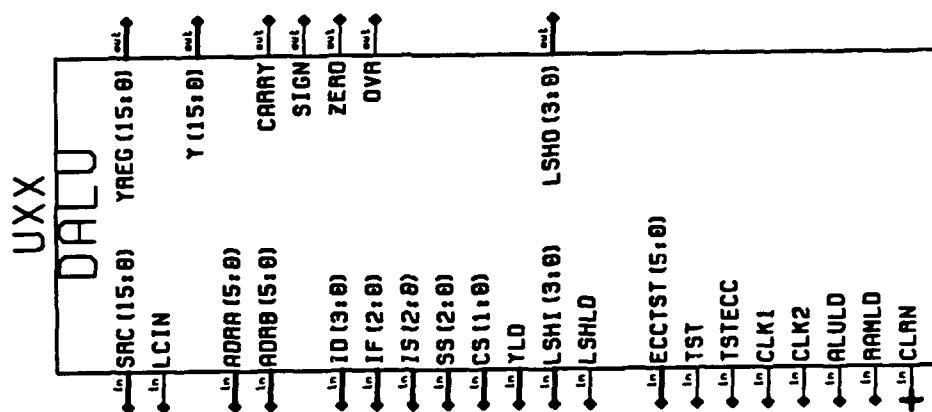


# CORNMUX: CORRECTION MUX

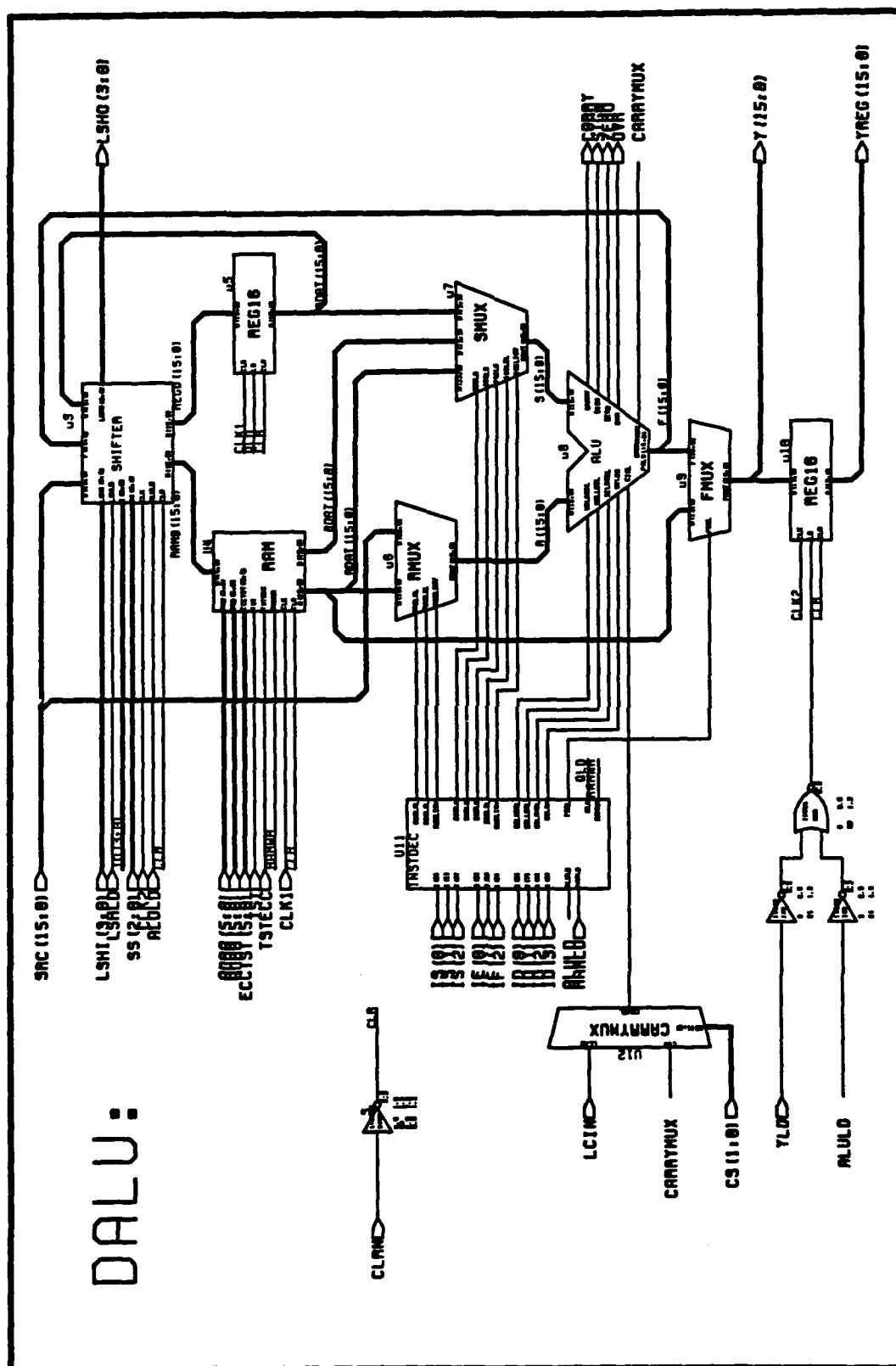


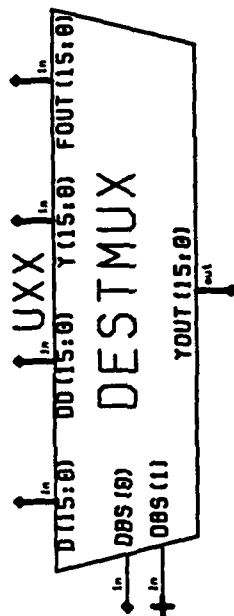


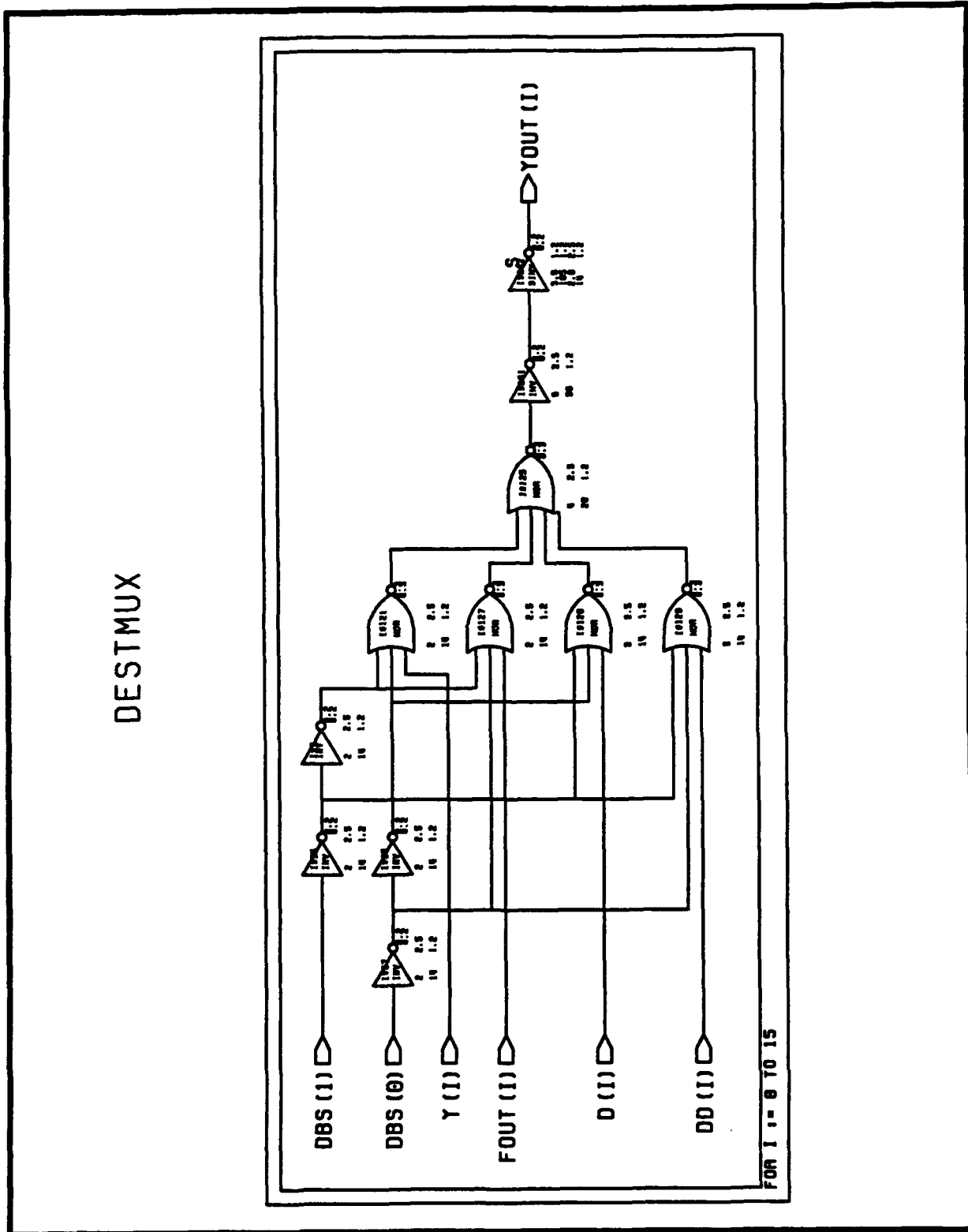










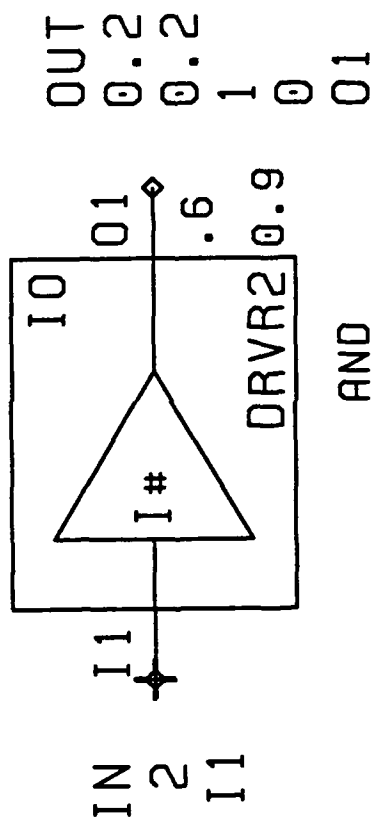


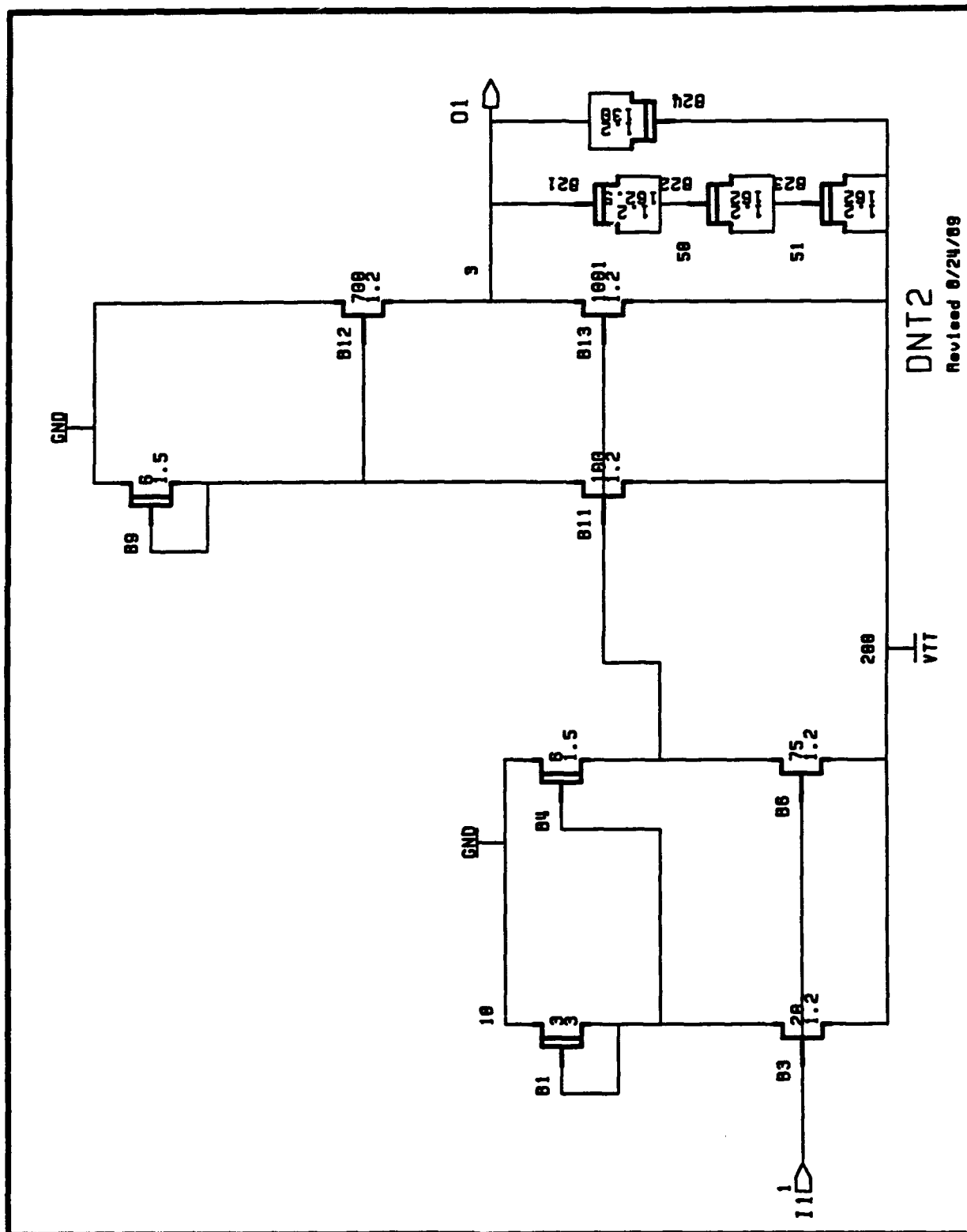
# VITESSE GAAS CELL LIBRARY

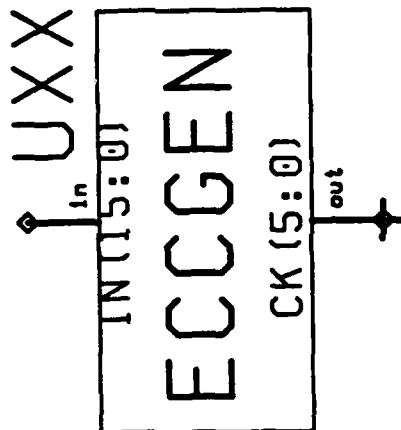
Version 0.8

NAME: DRVR2

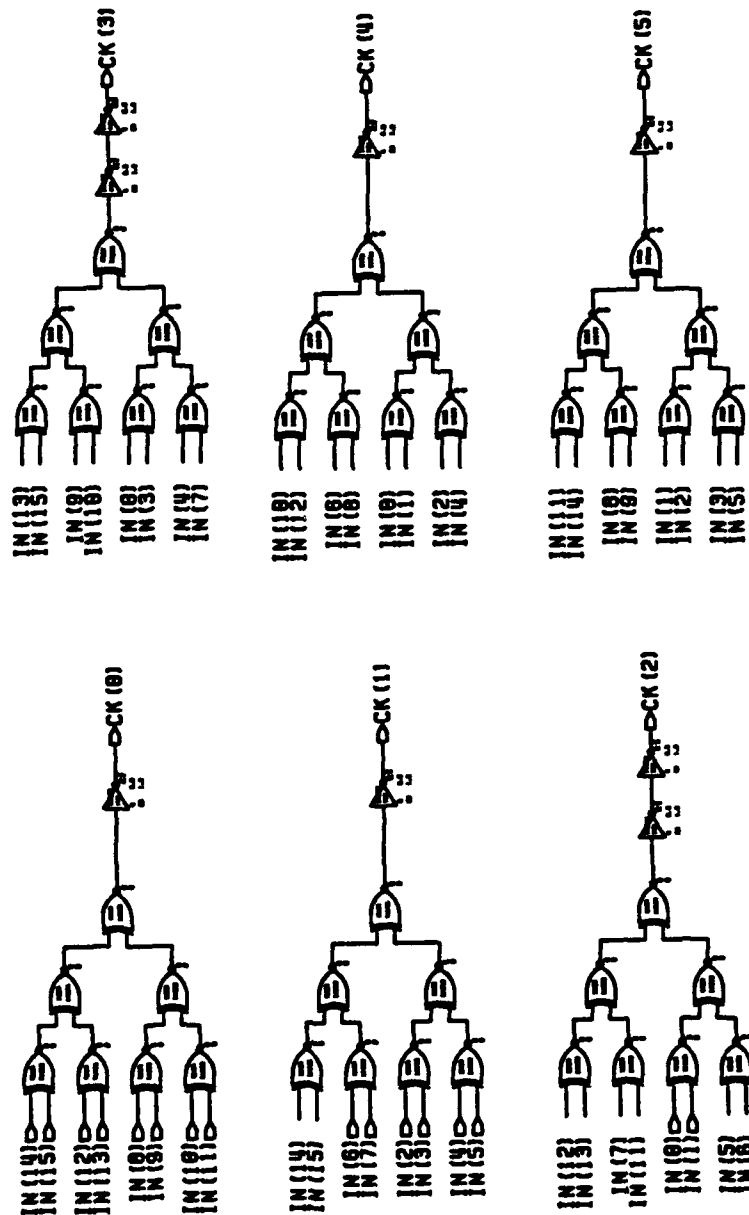
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD

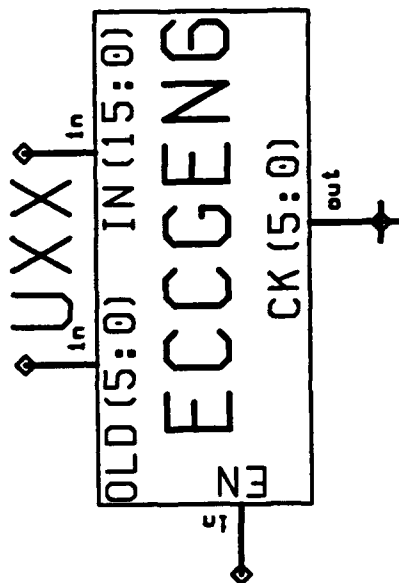






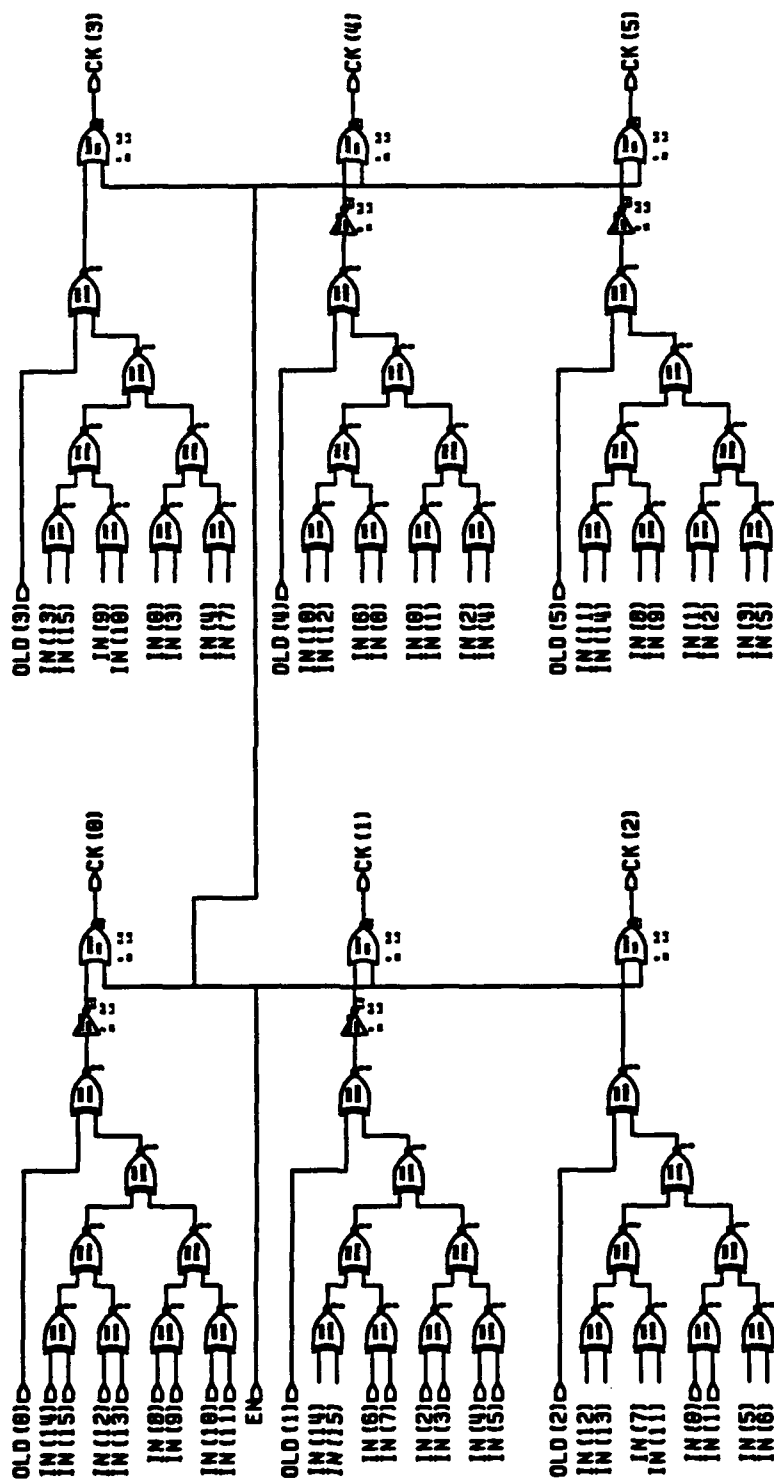
ECCGEN6: ECC CHECK BIT GENERATION

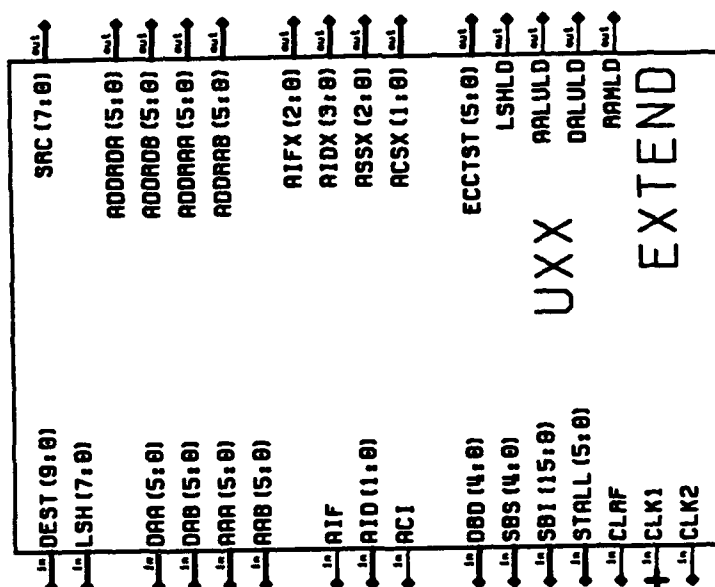


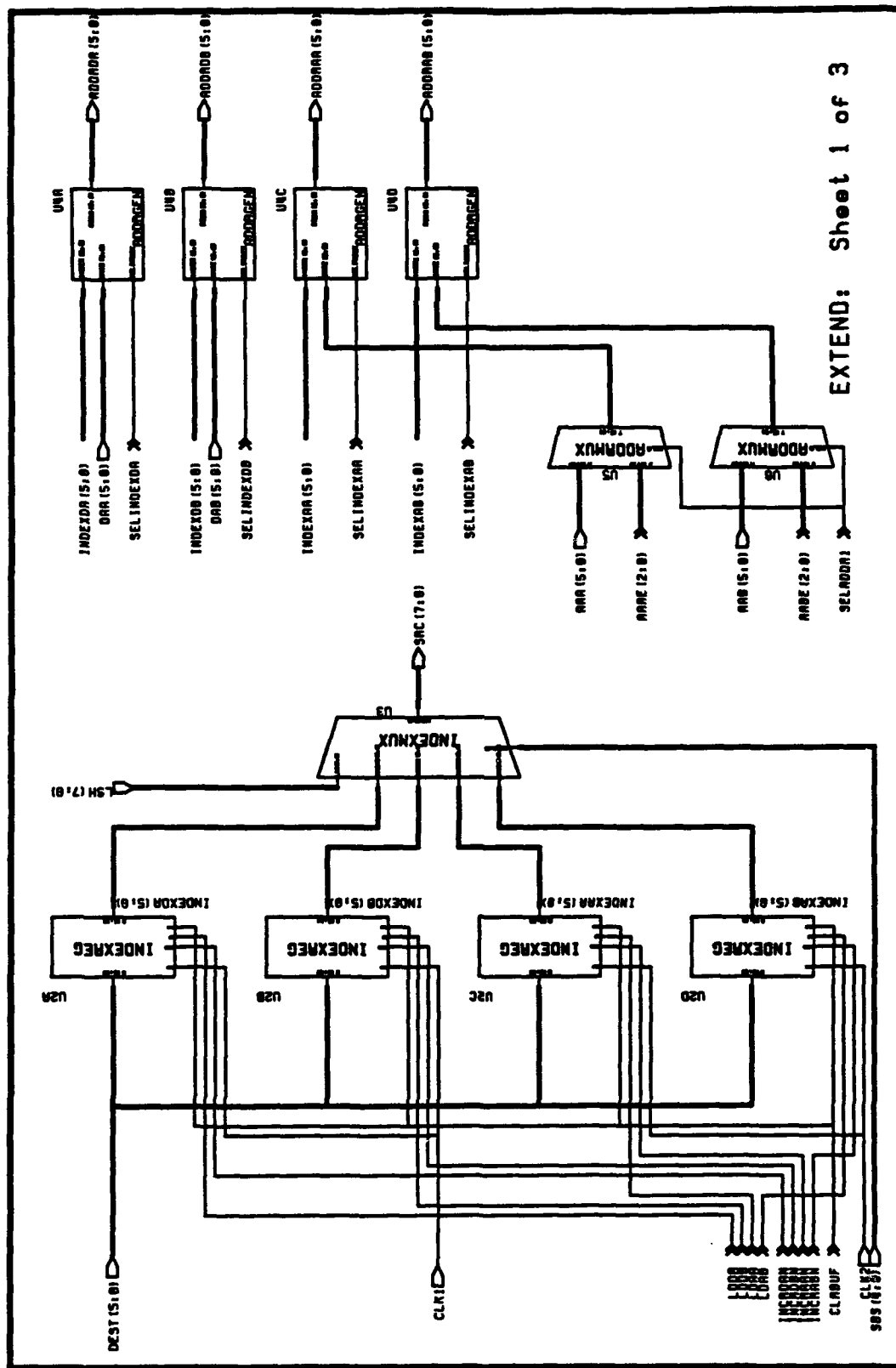




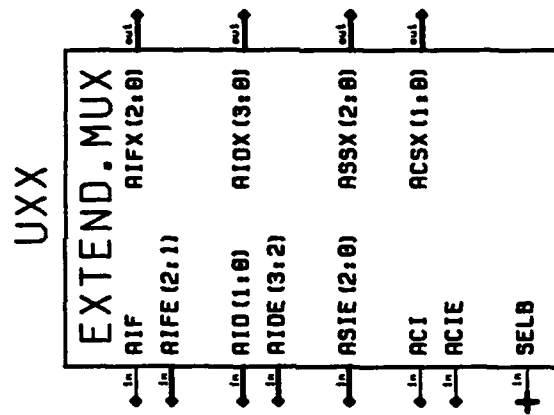
ECCGEN6: ECC CHECK BIT GENERATION

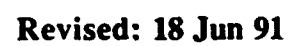


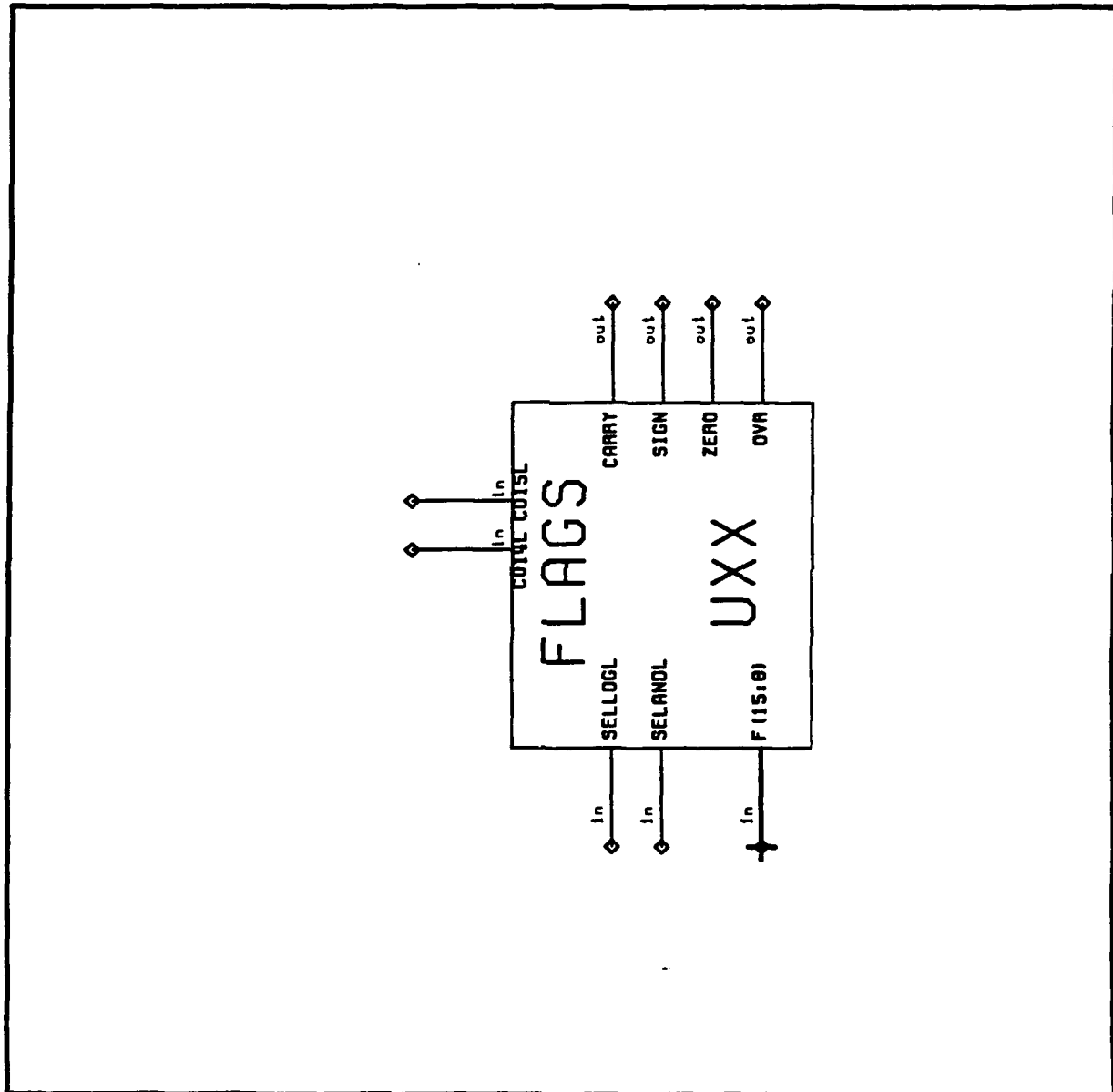


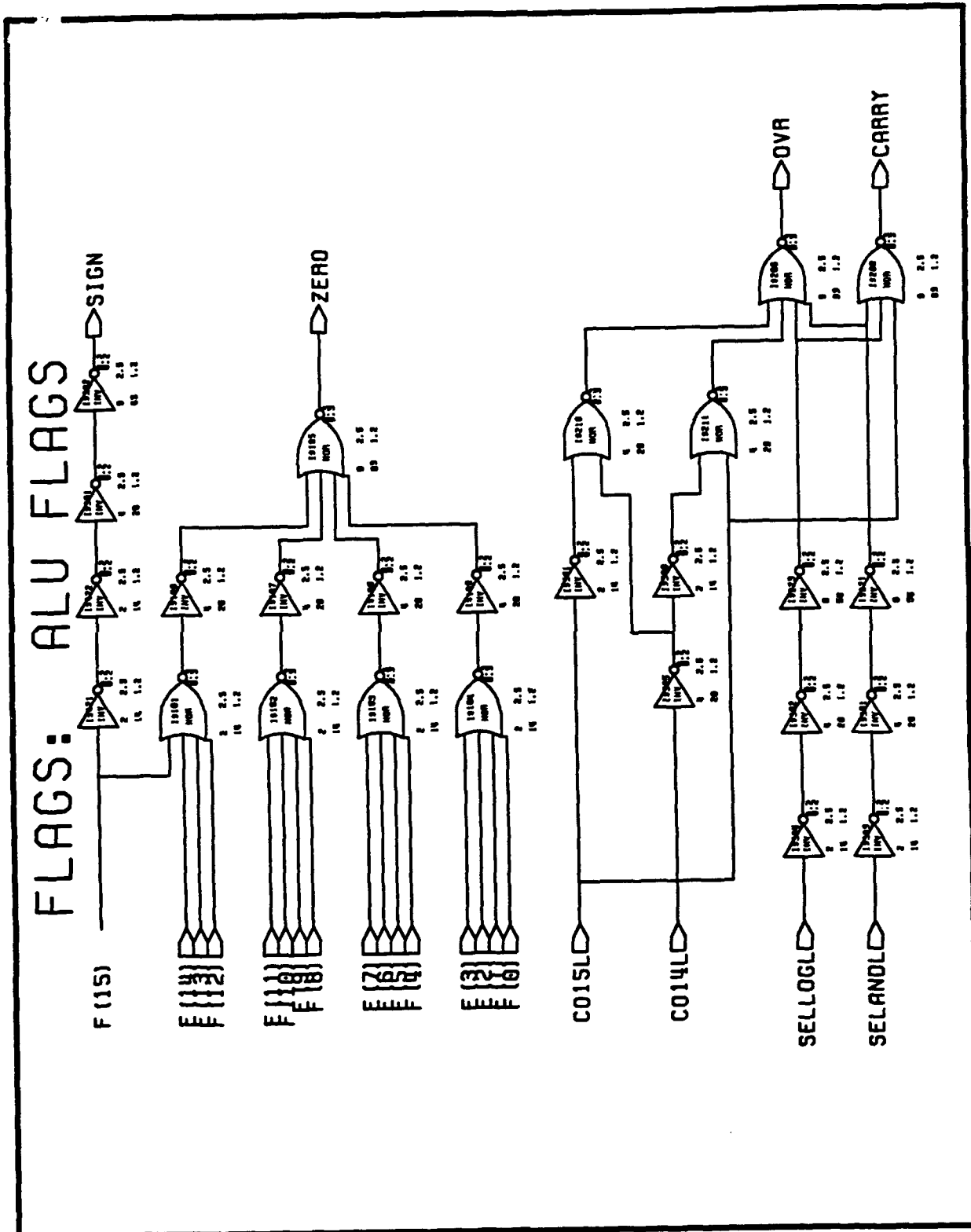


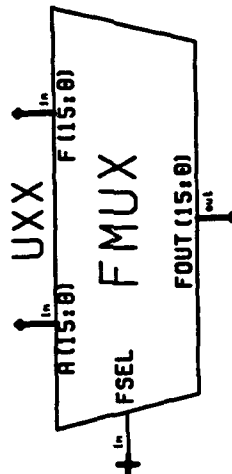
EXTEND: Sheet 1 of 3





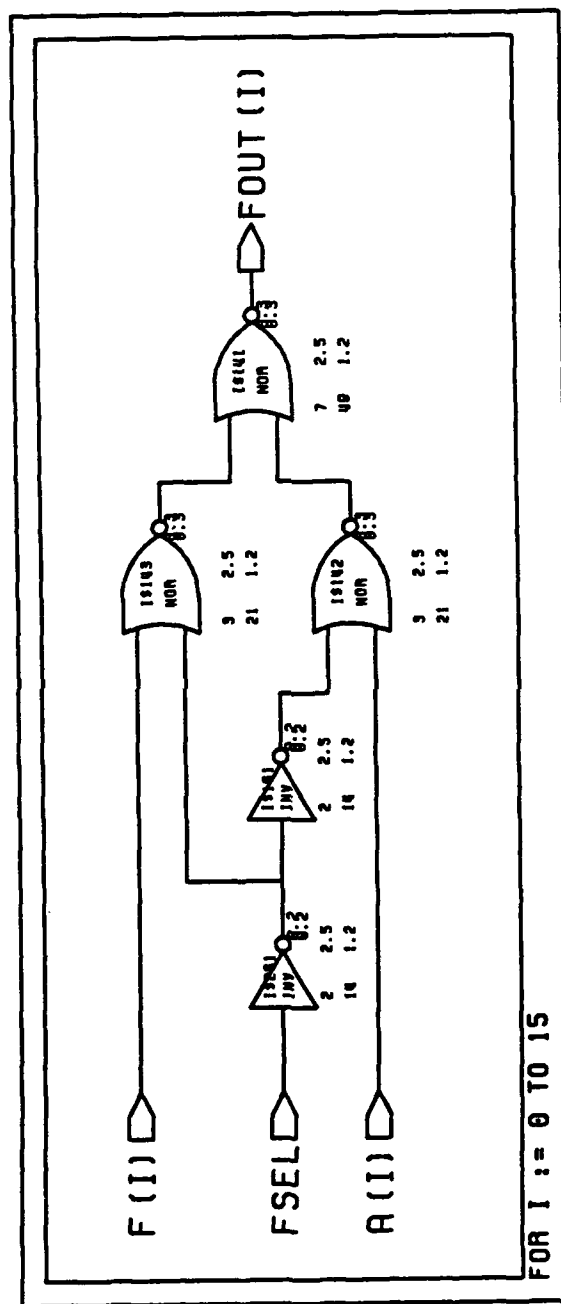


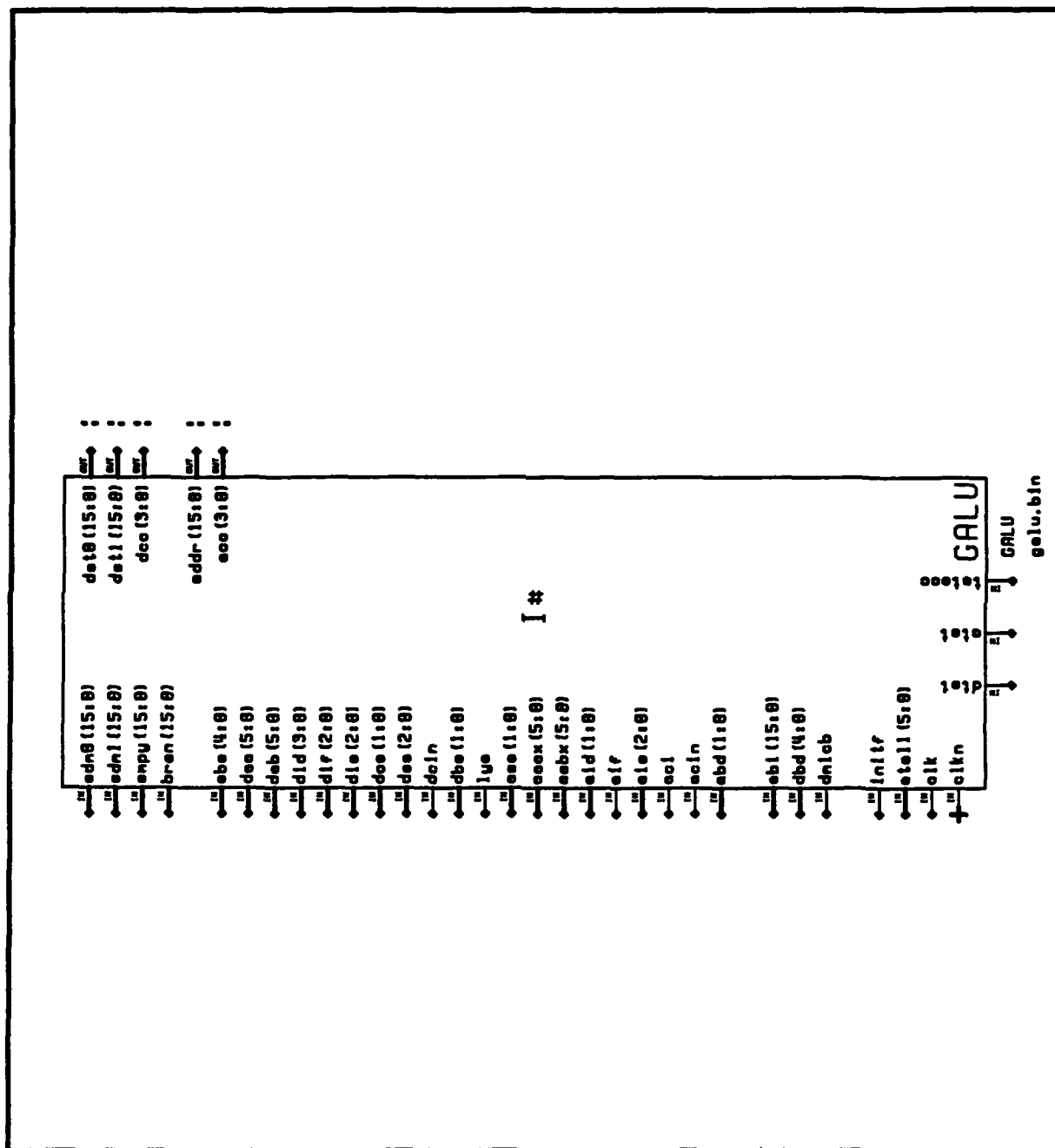


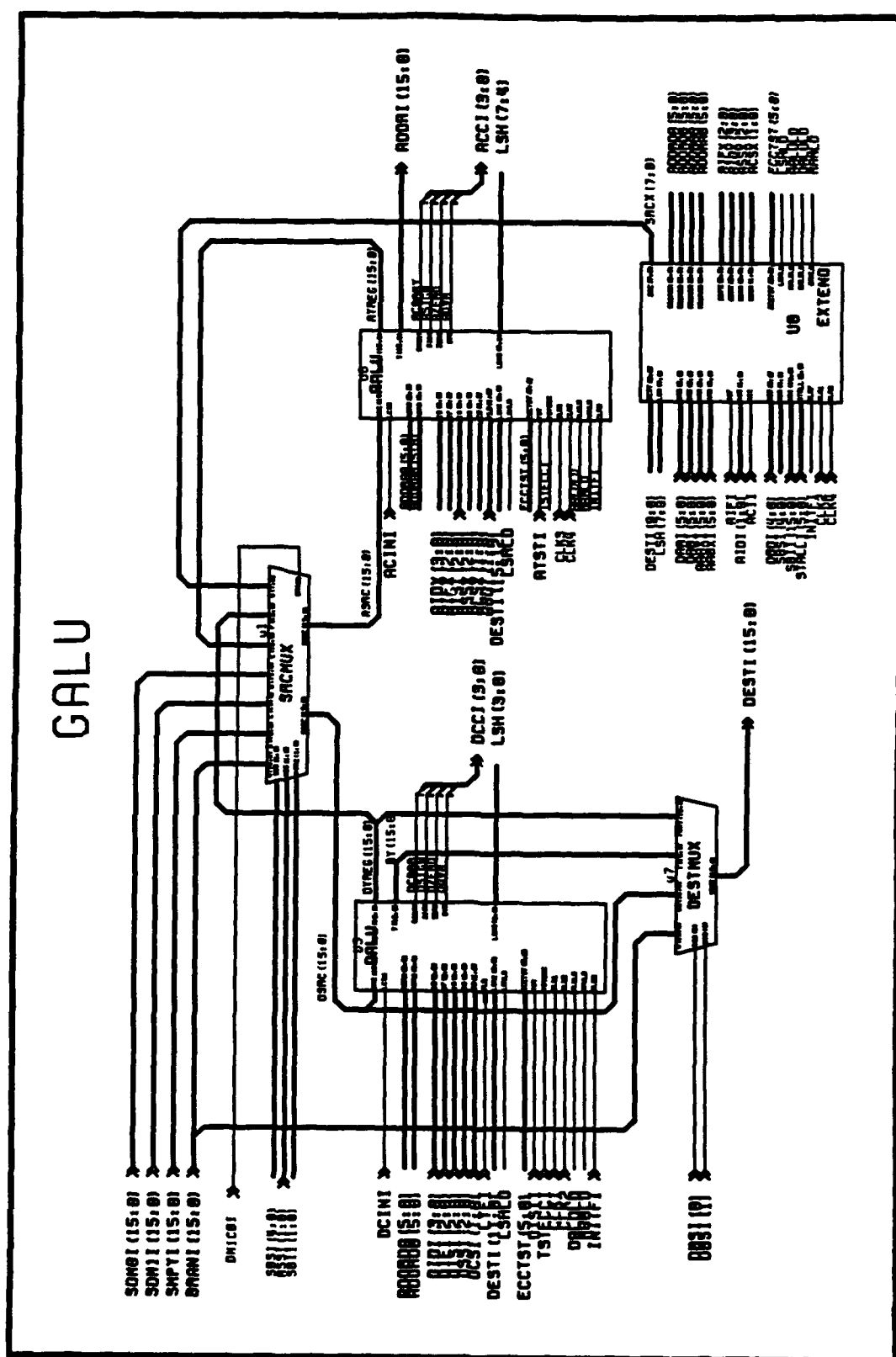


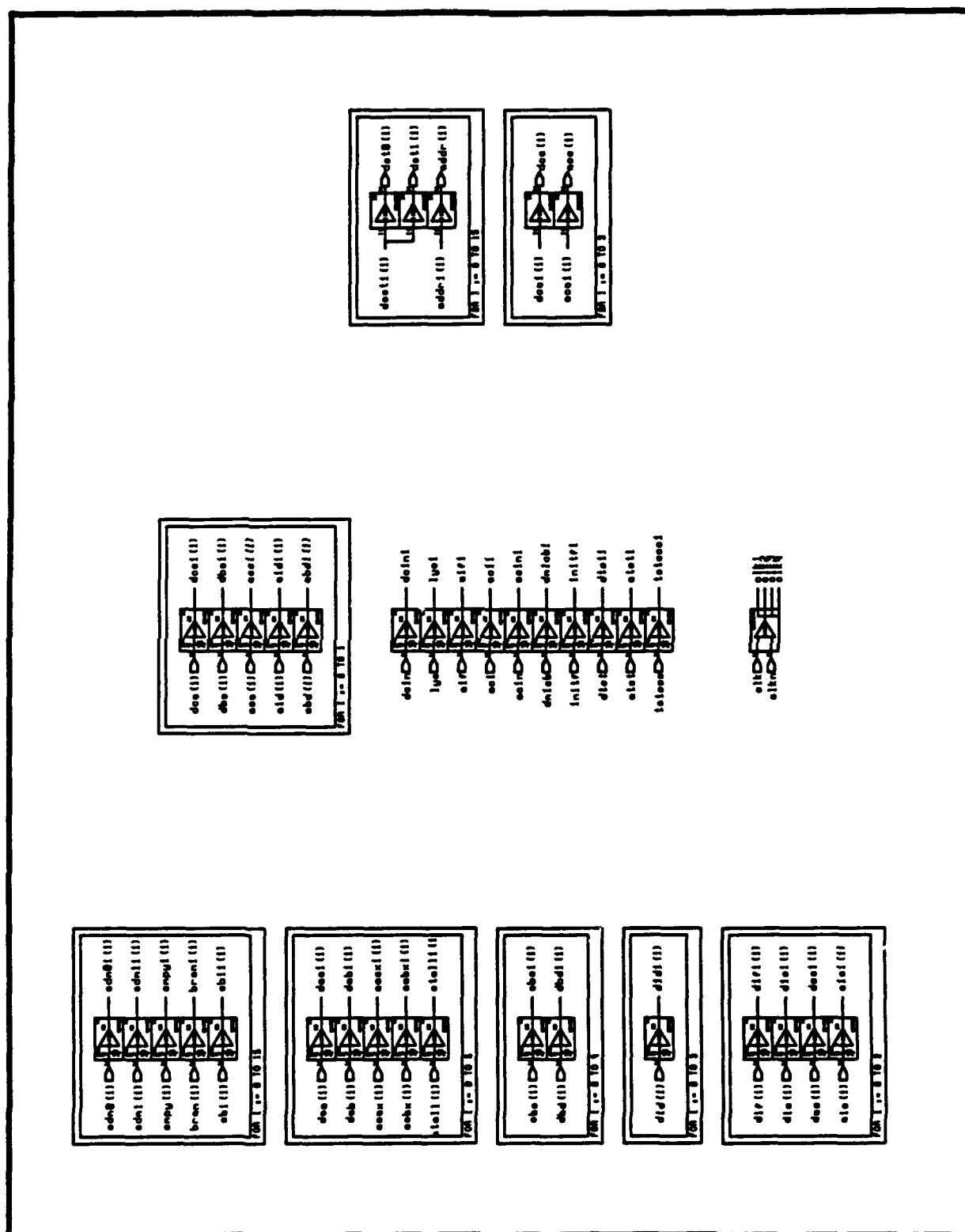


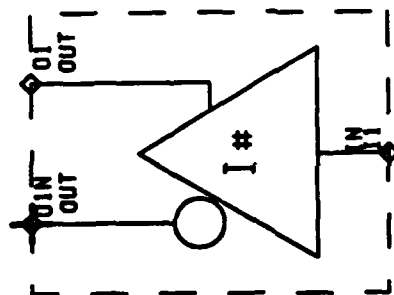
# FMUX



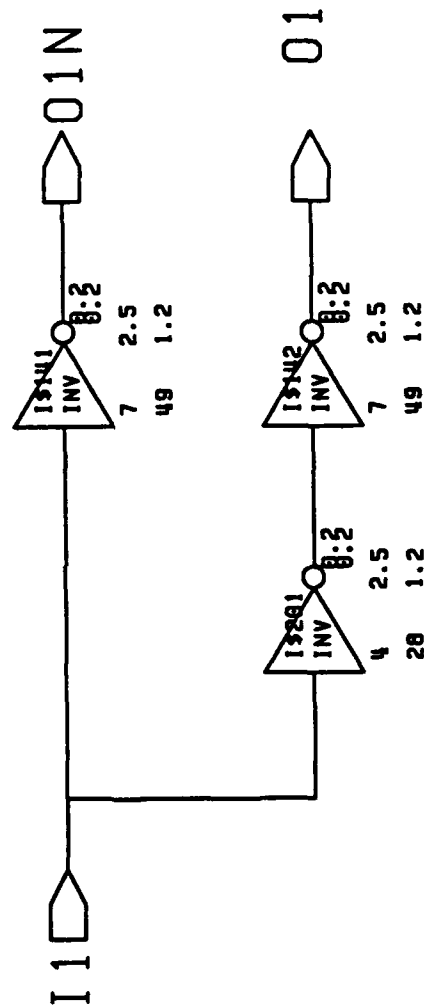








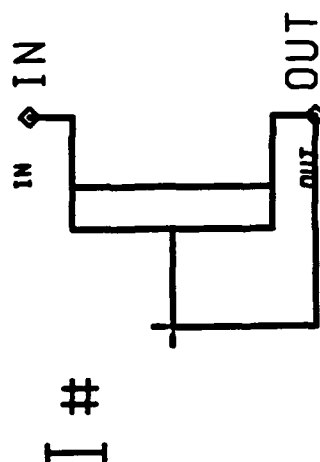
# IBUFSMALL

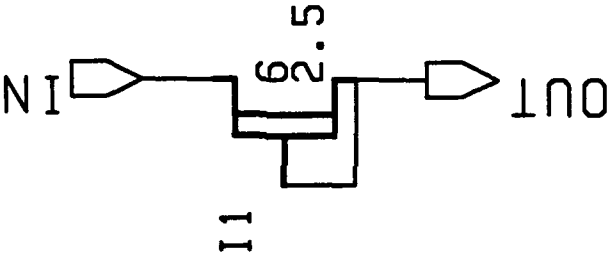


VITESSE GAAS LIBRARY

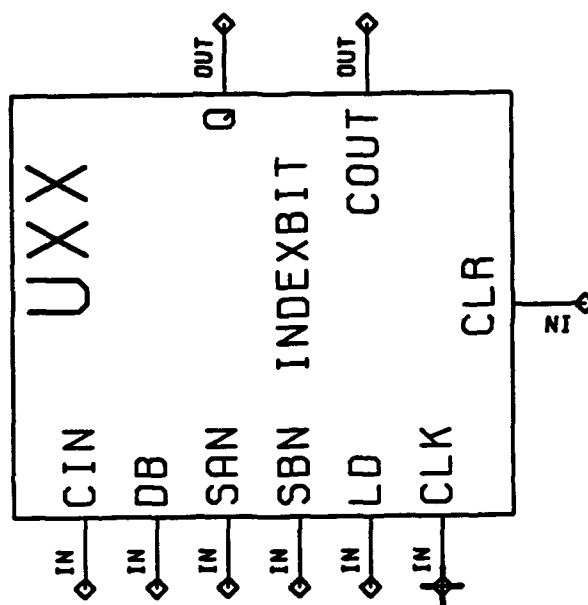
NAME: \$dep

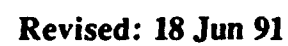
DESCRIPTION: depletion gaasfet

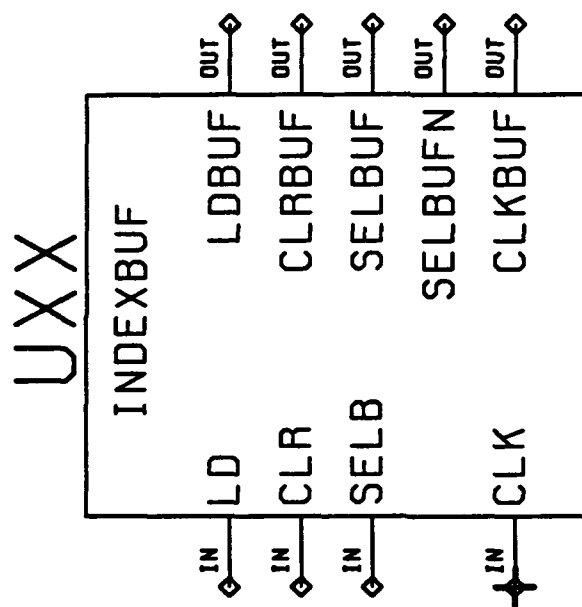


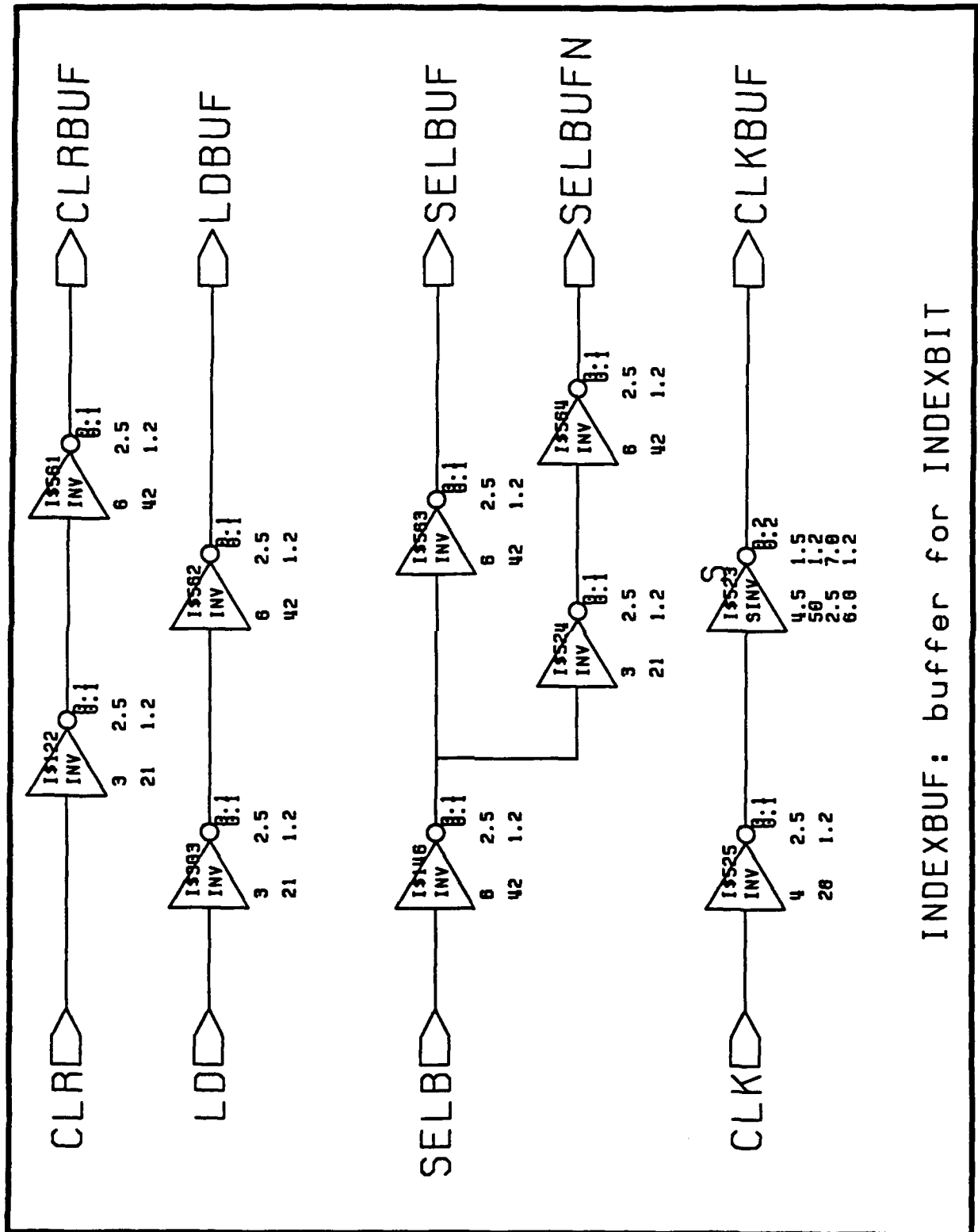




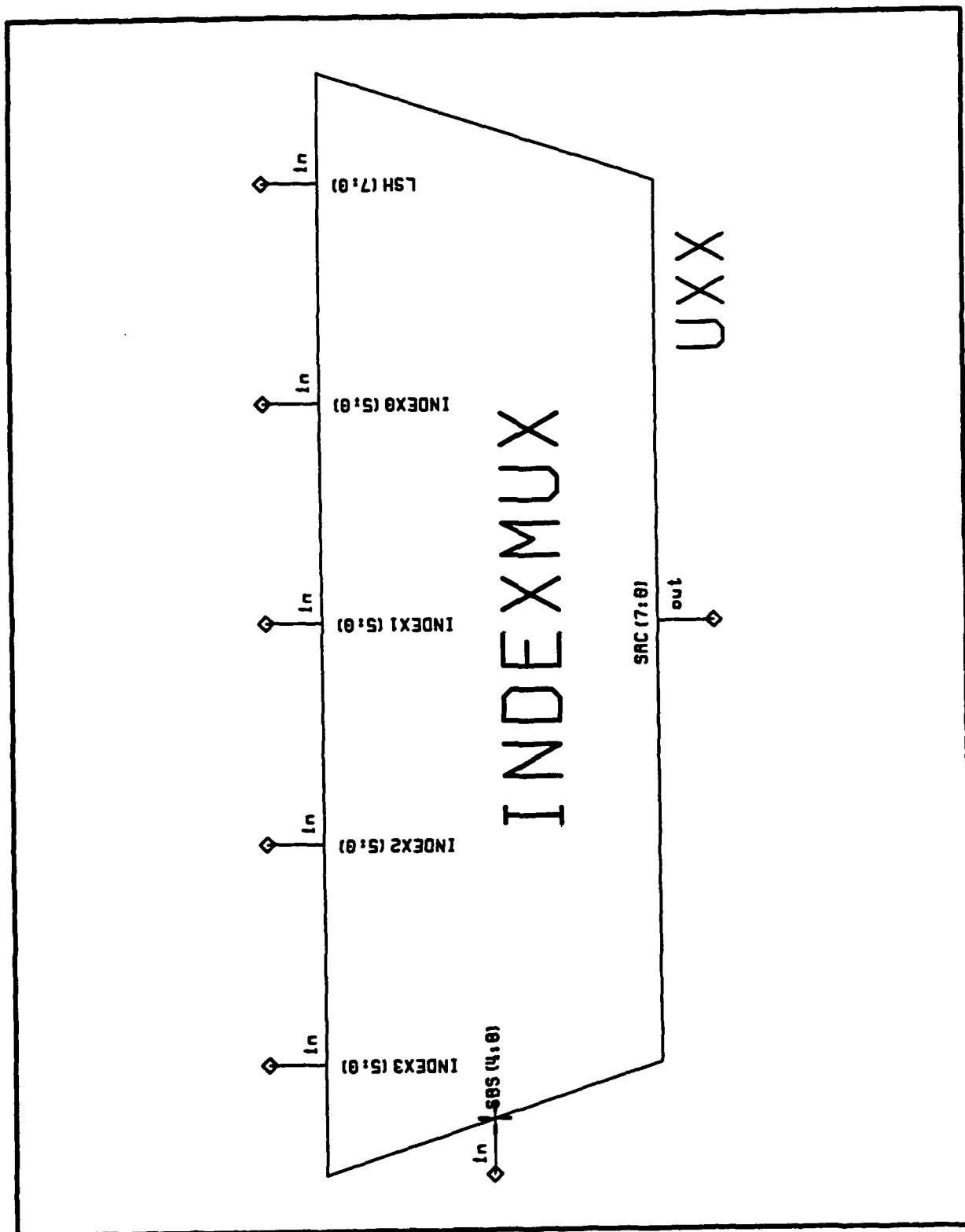




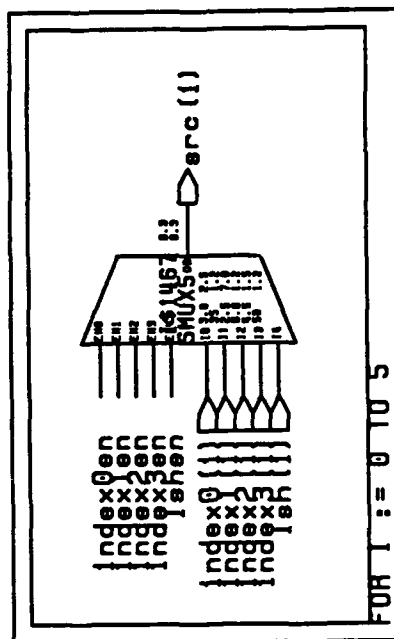
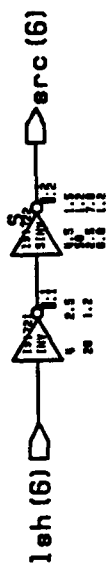
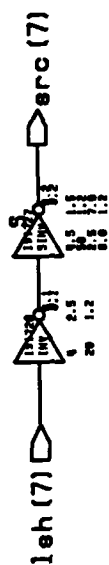
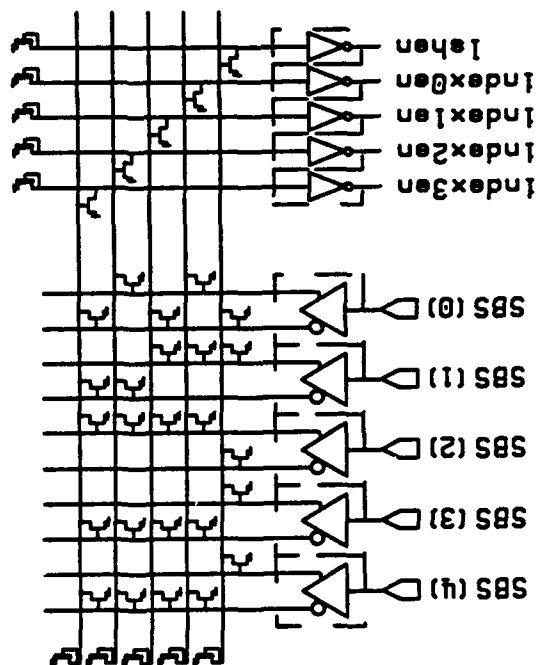


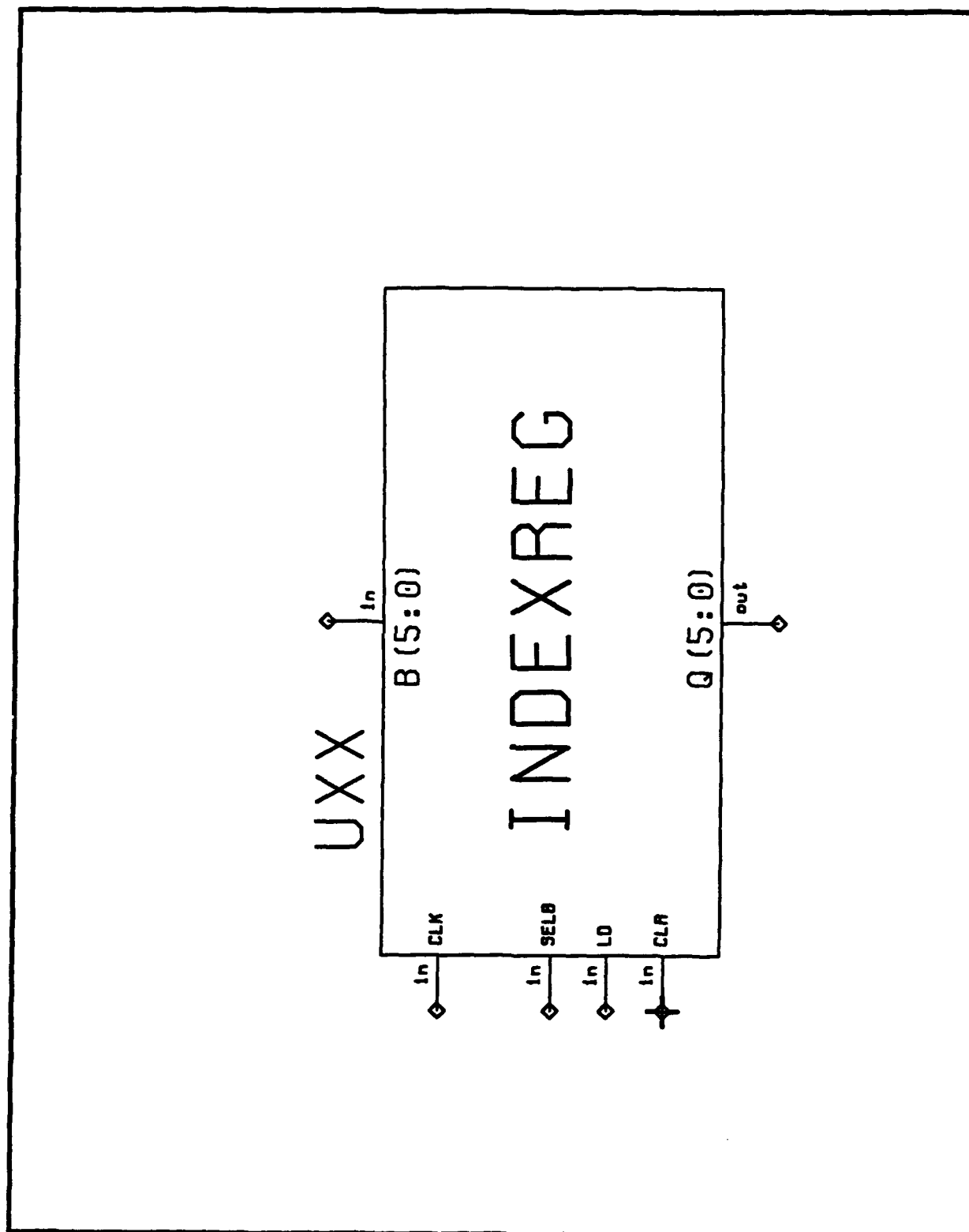


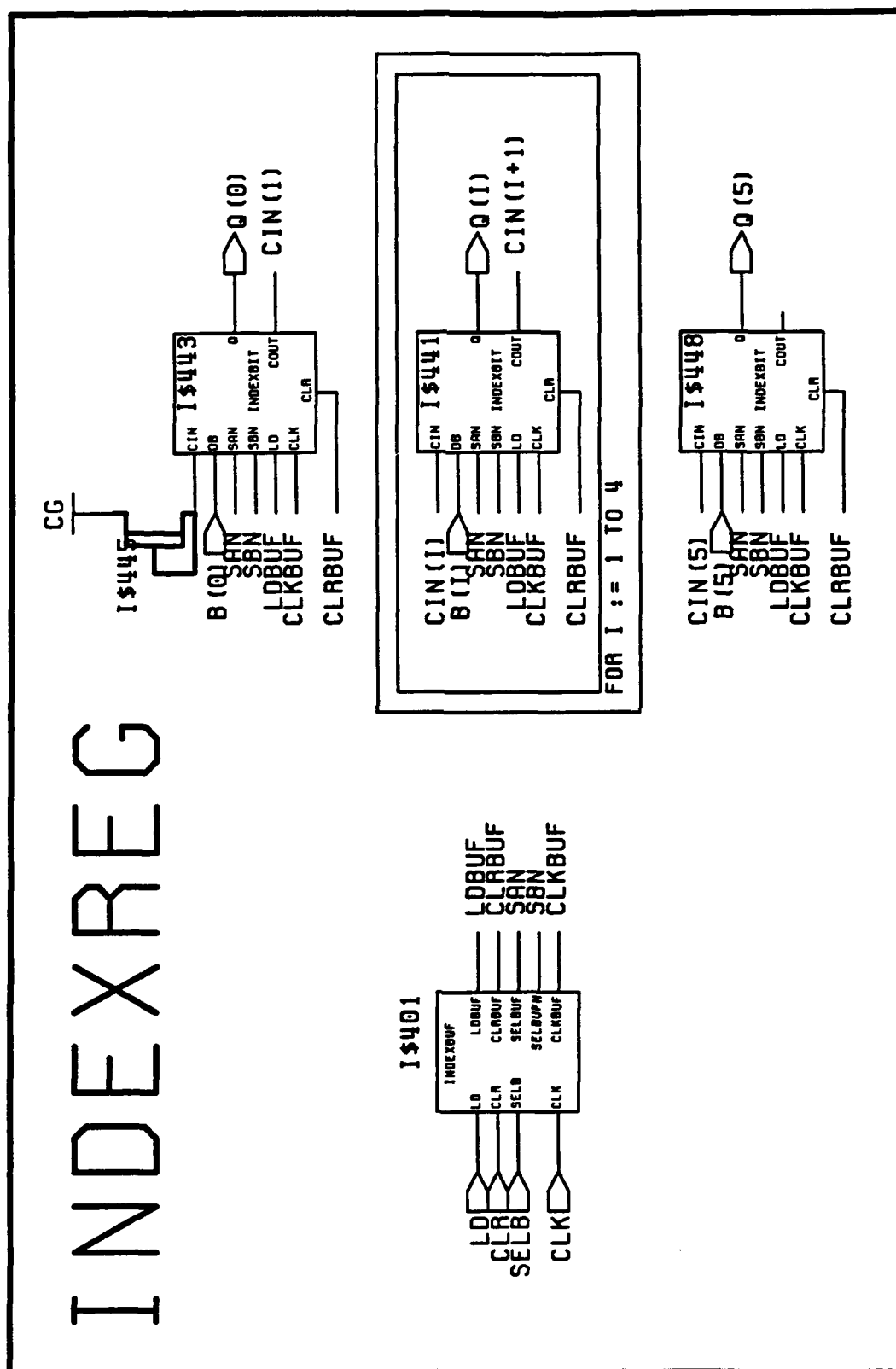
INDEXBUF: buffer for INDEXBIT



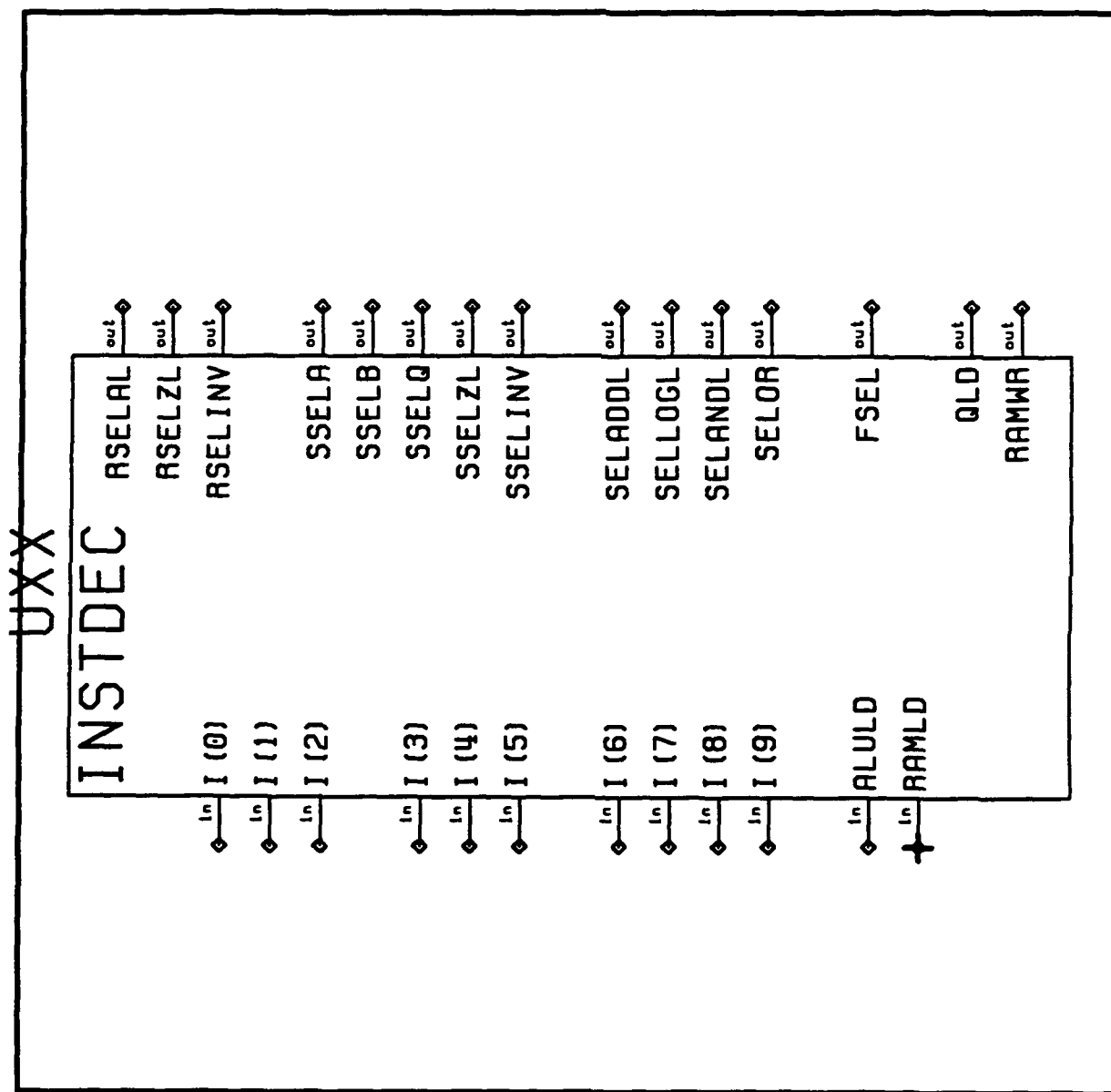
INDEXMUX: 5:1 by 8

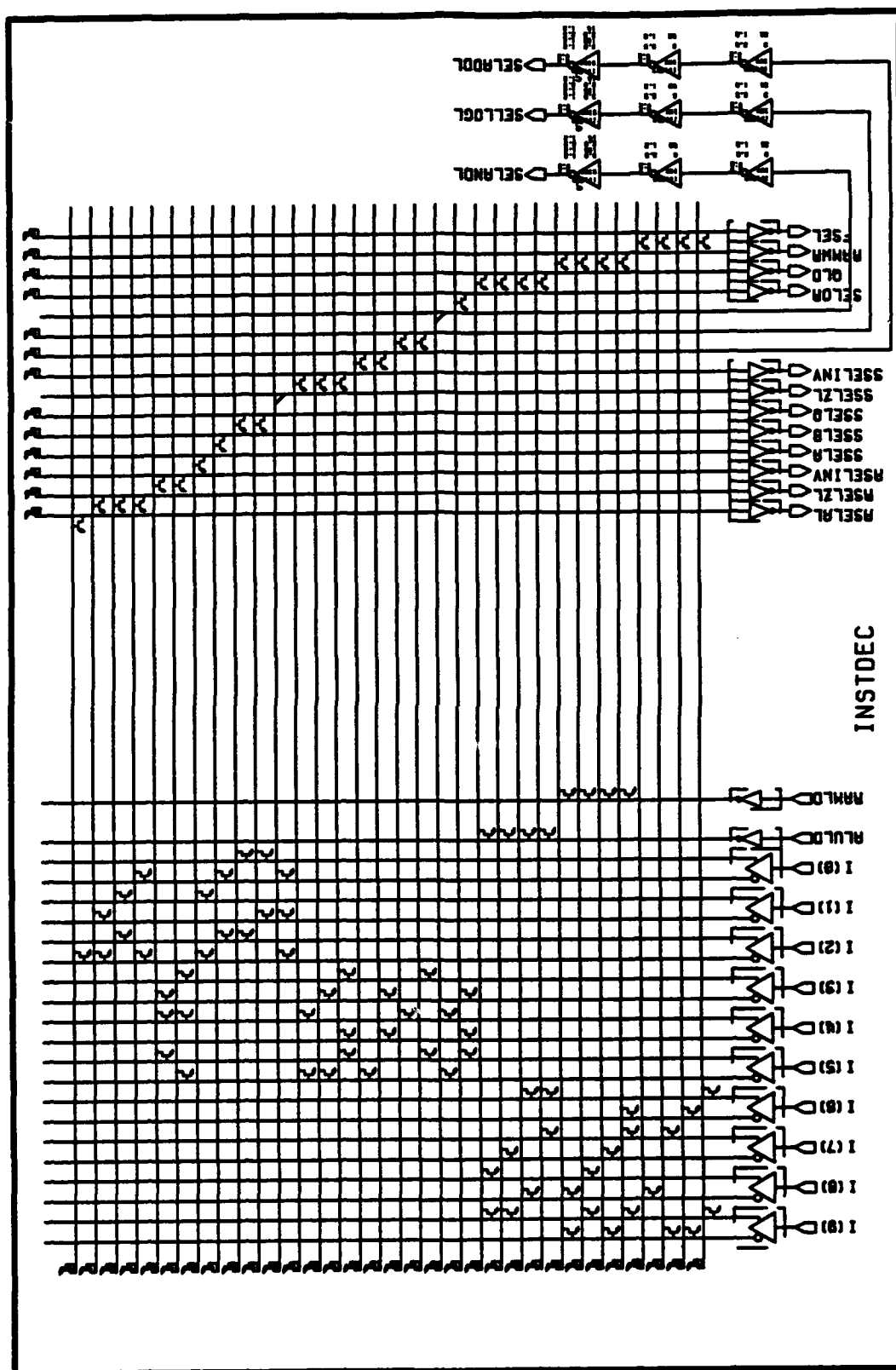


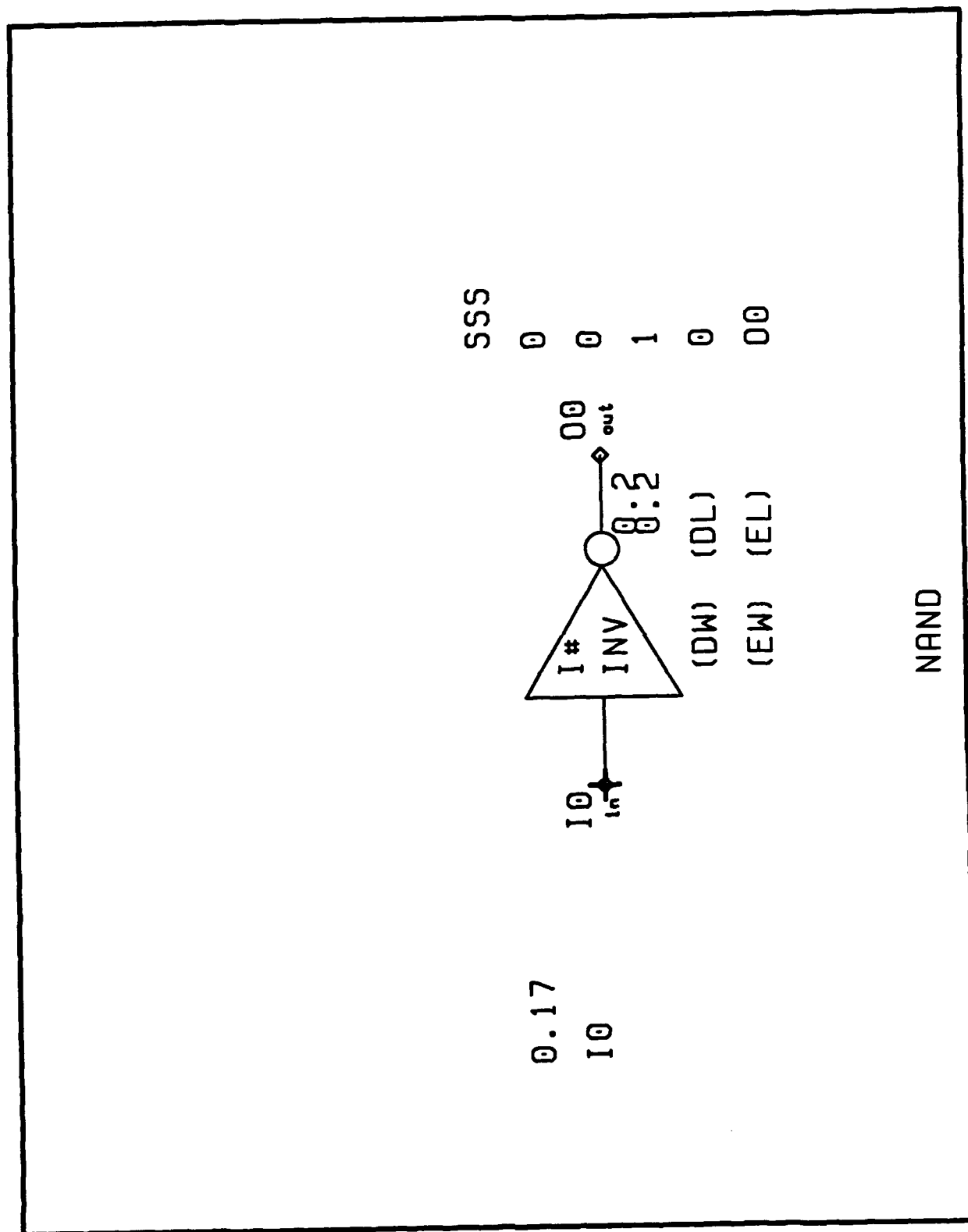


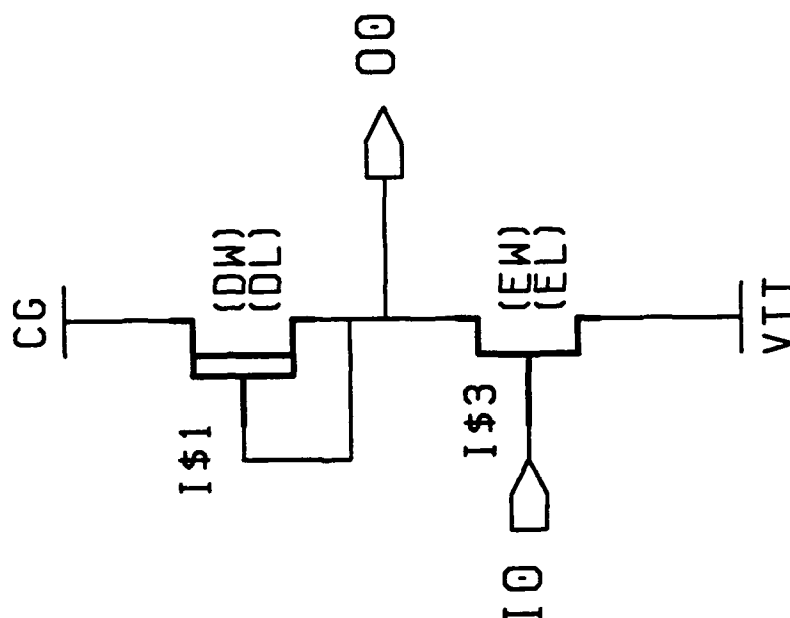


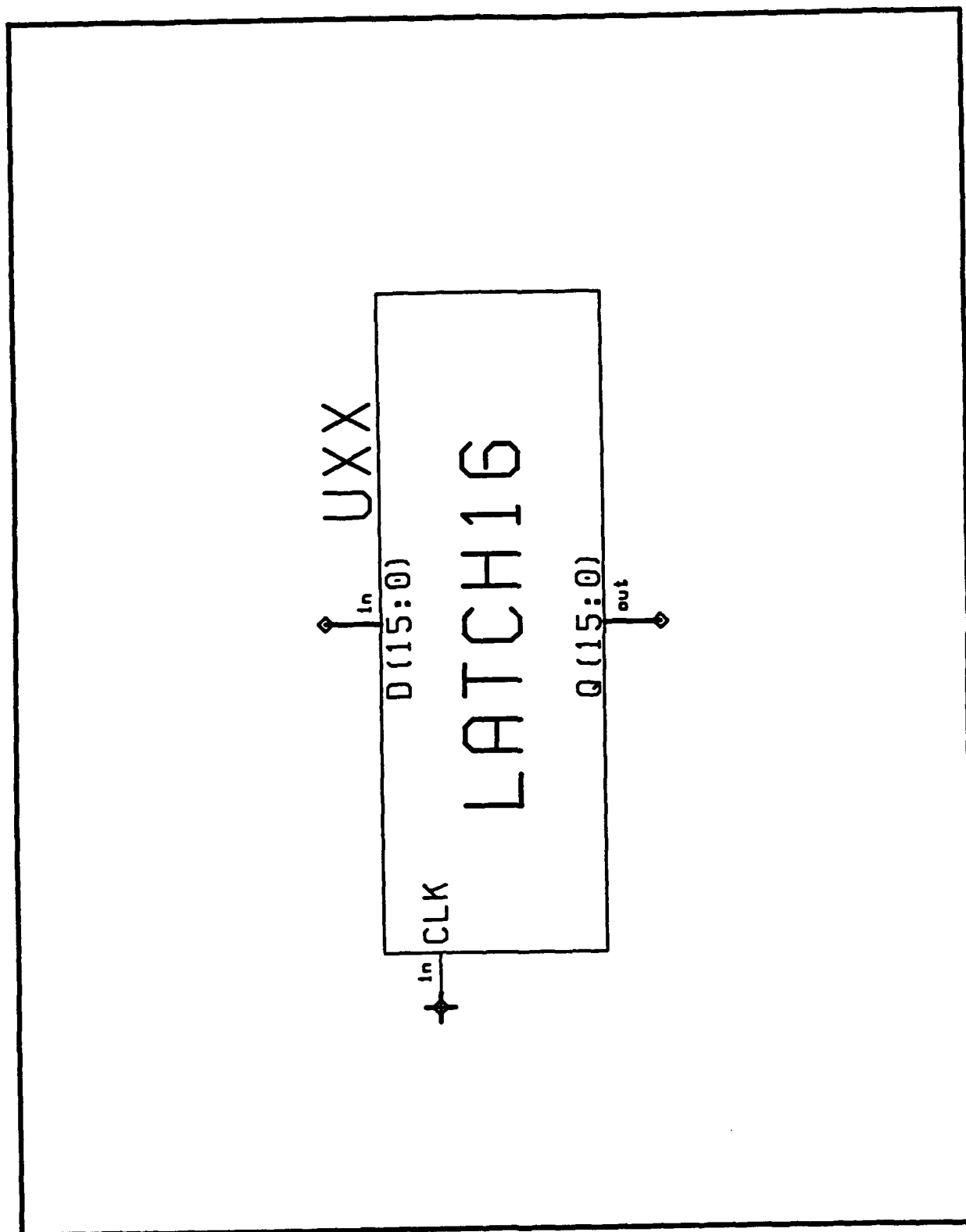




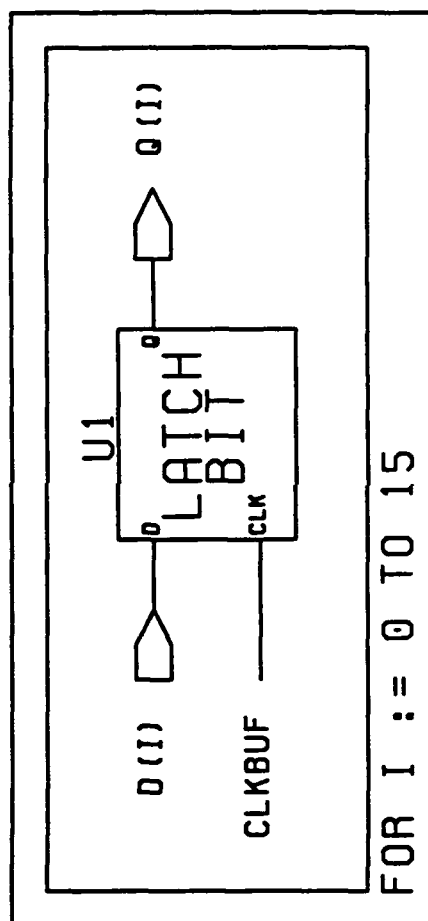
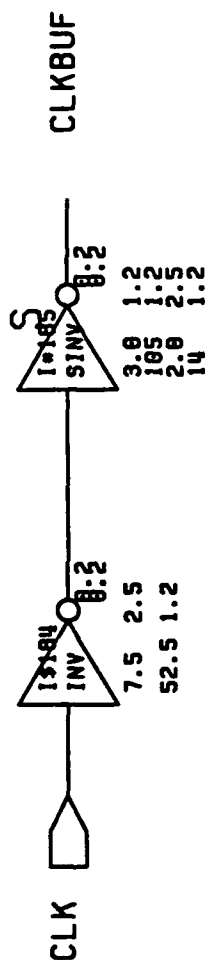


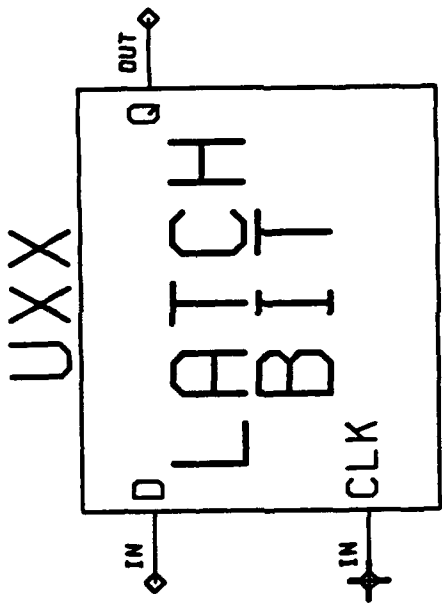


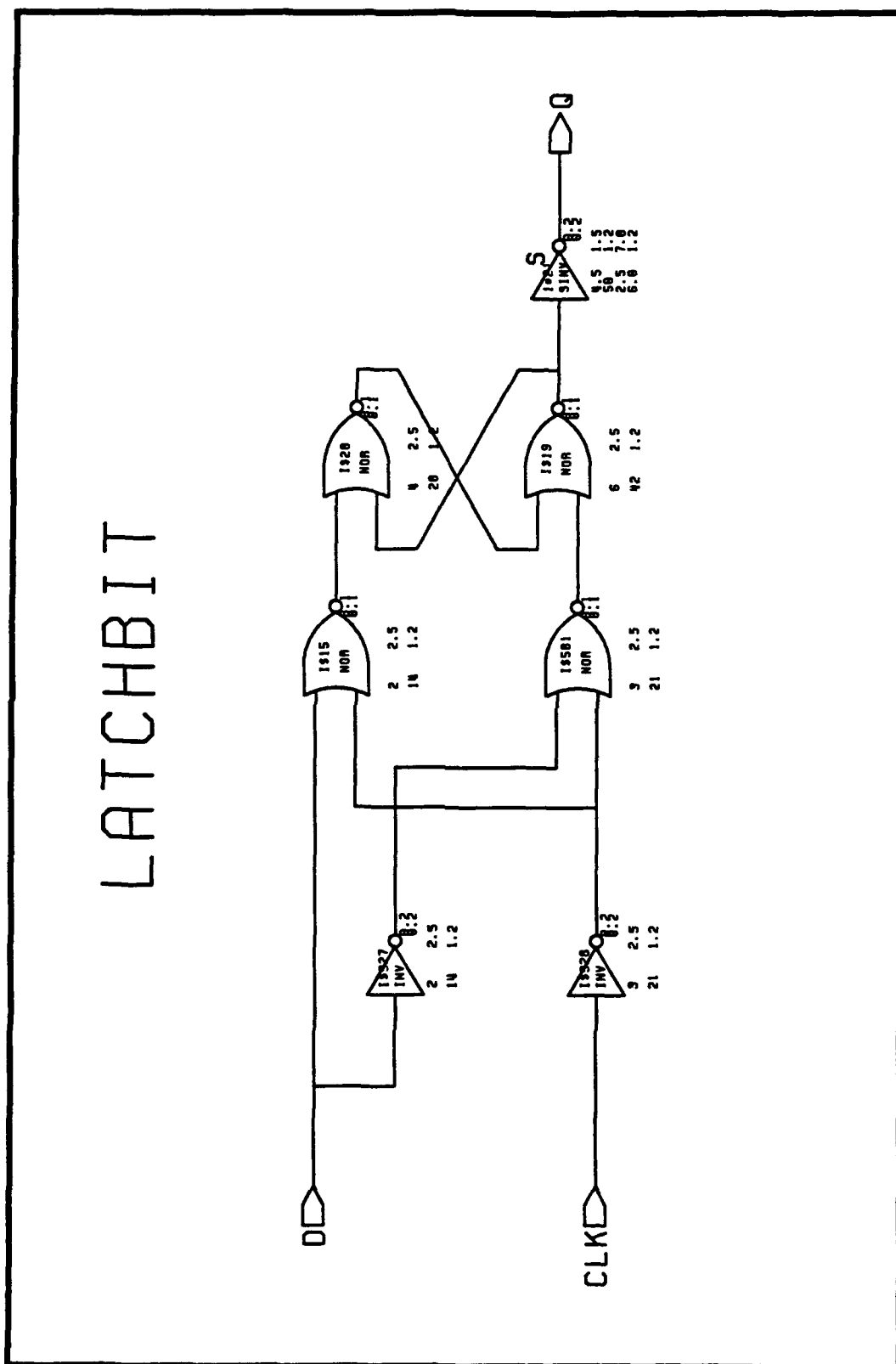




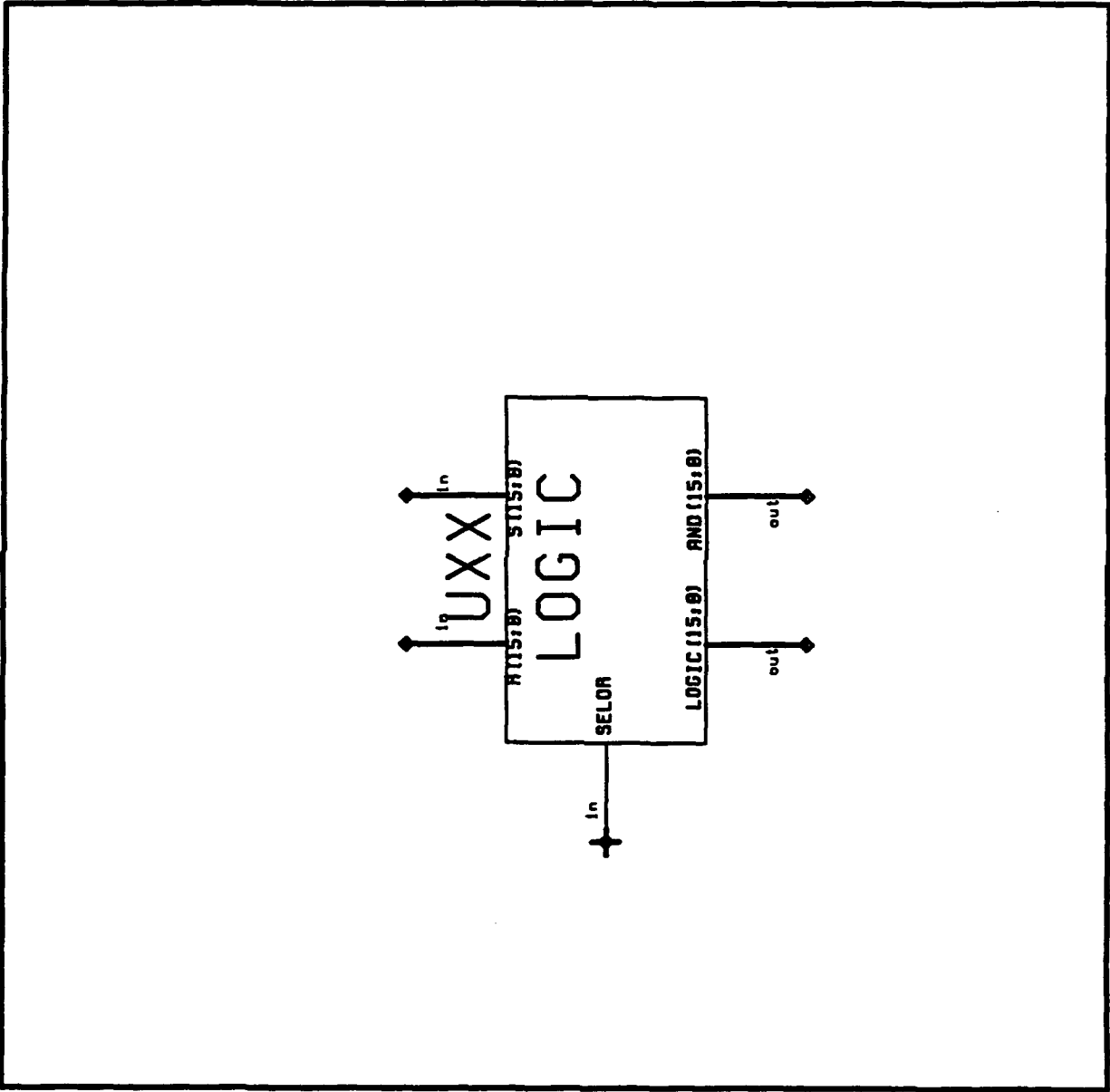
# LATCH16



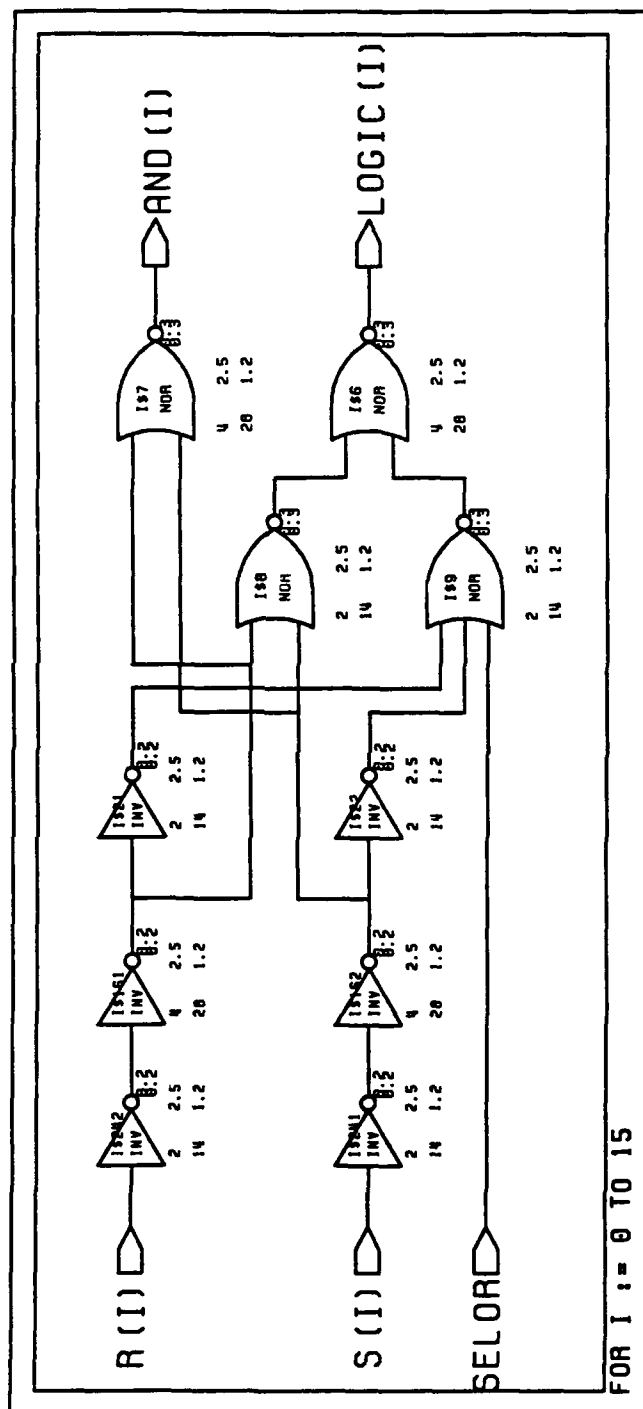


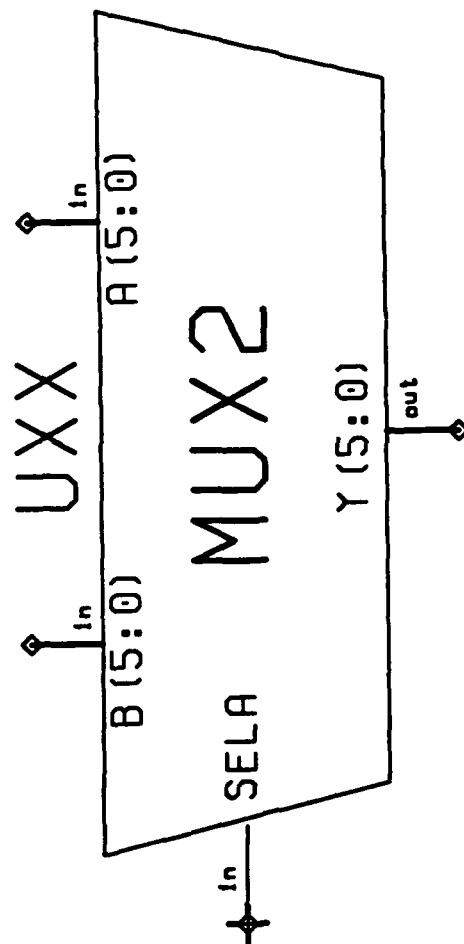


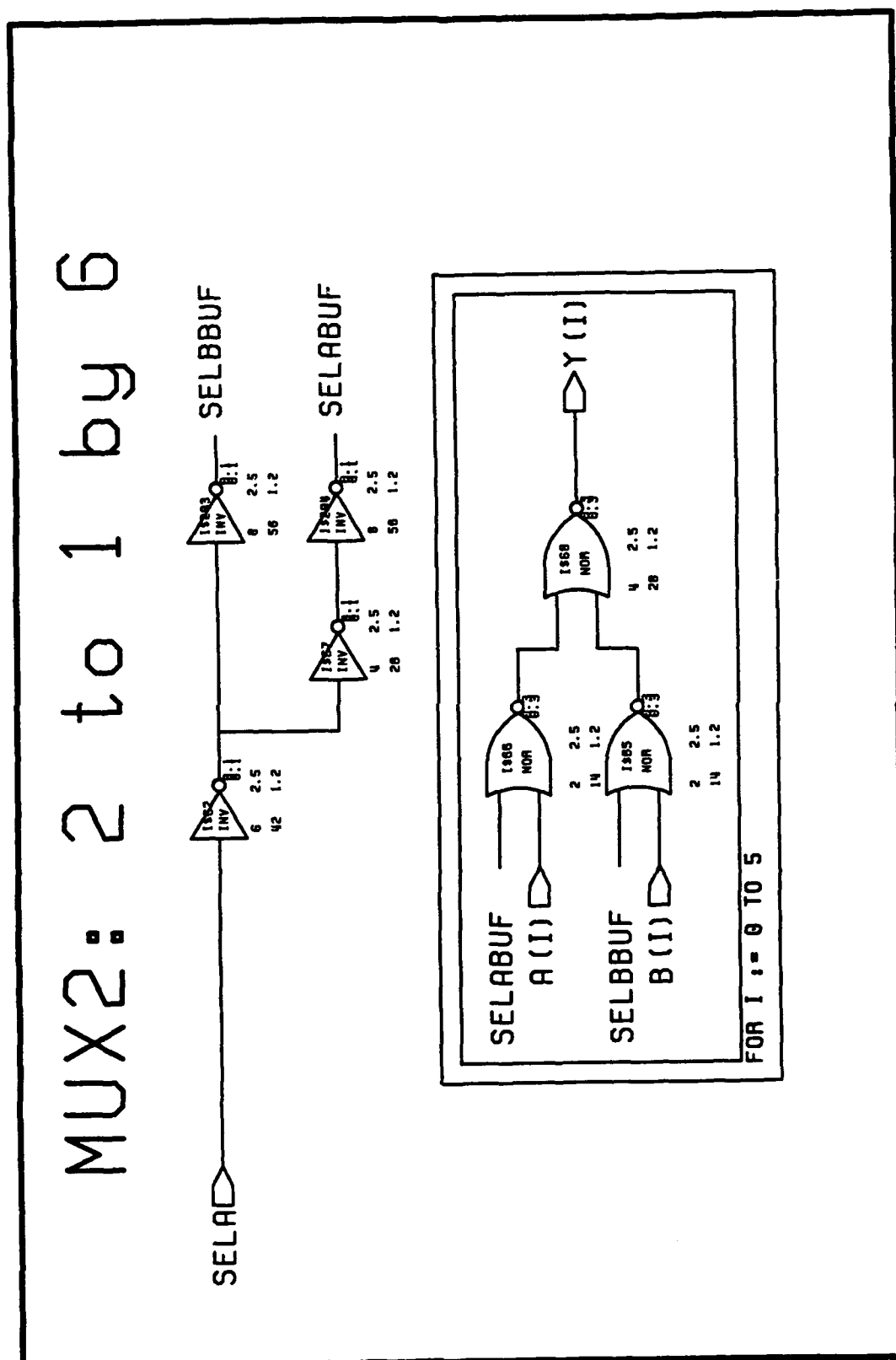


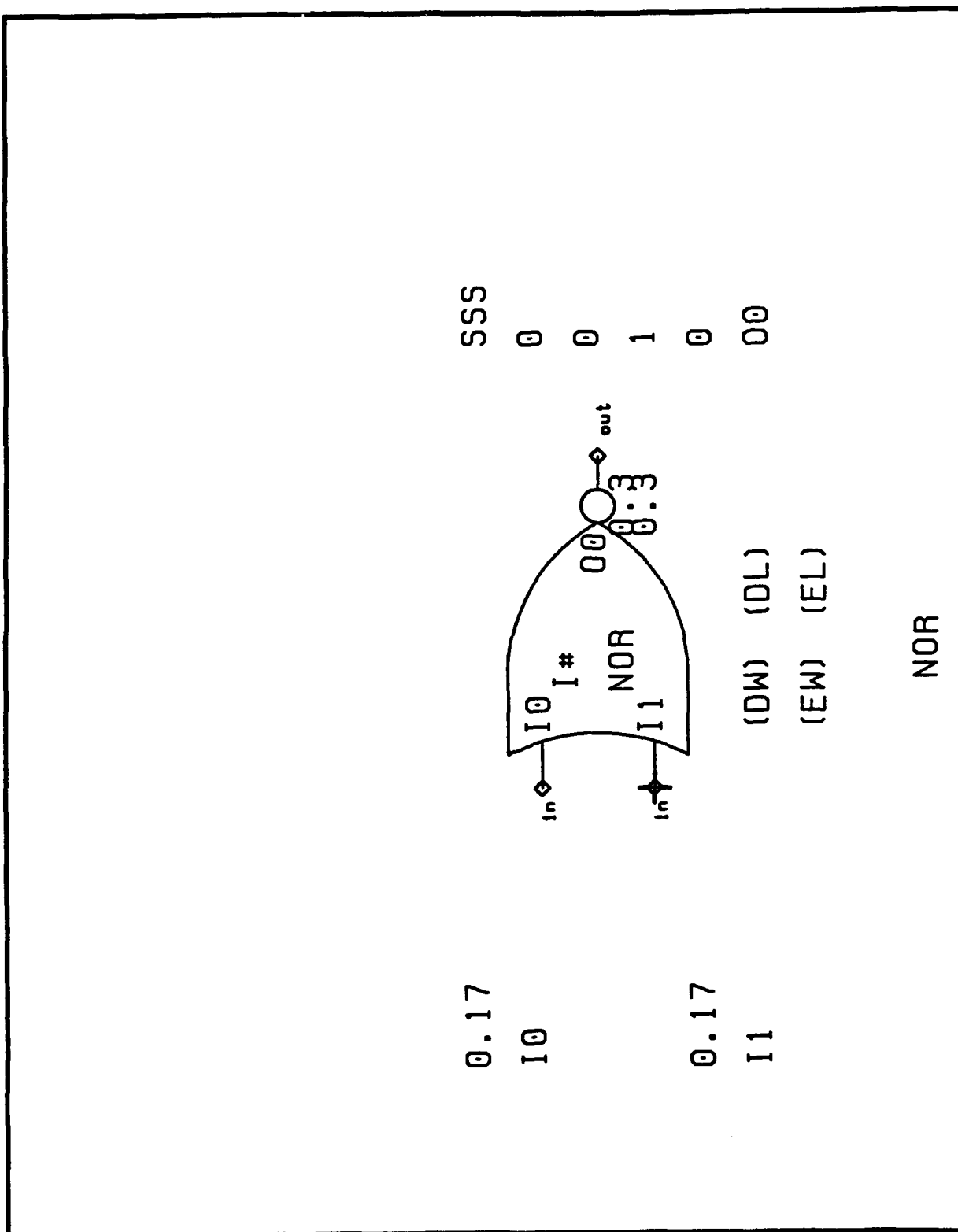


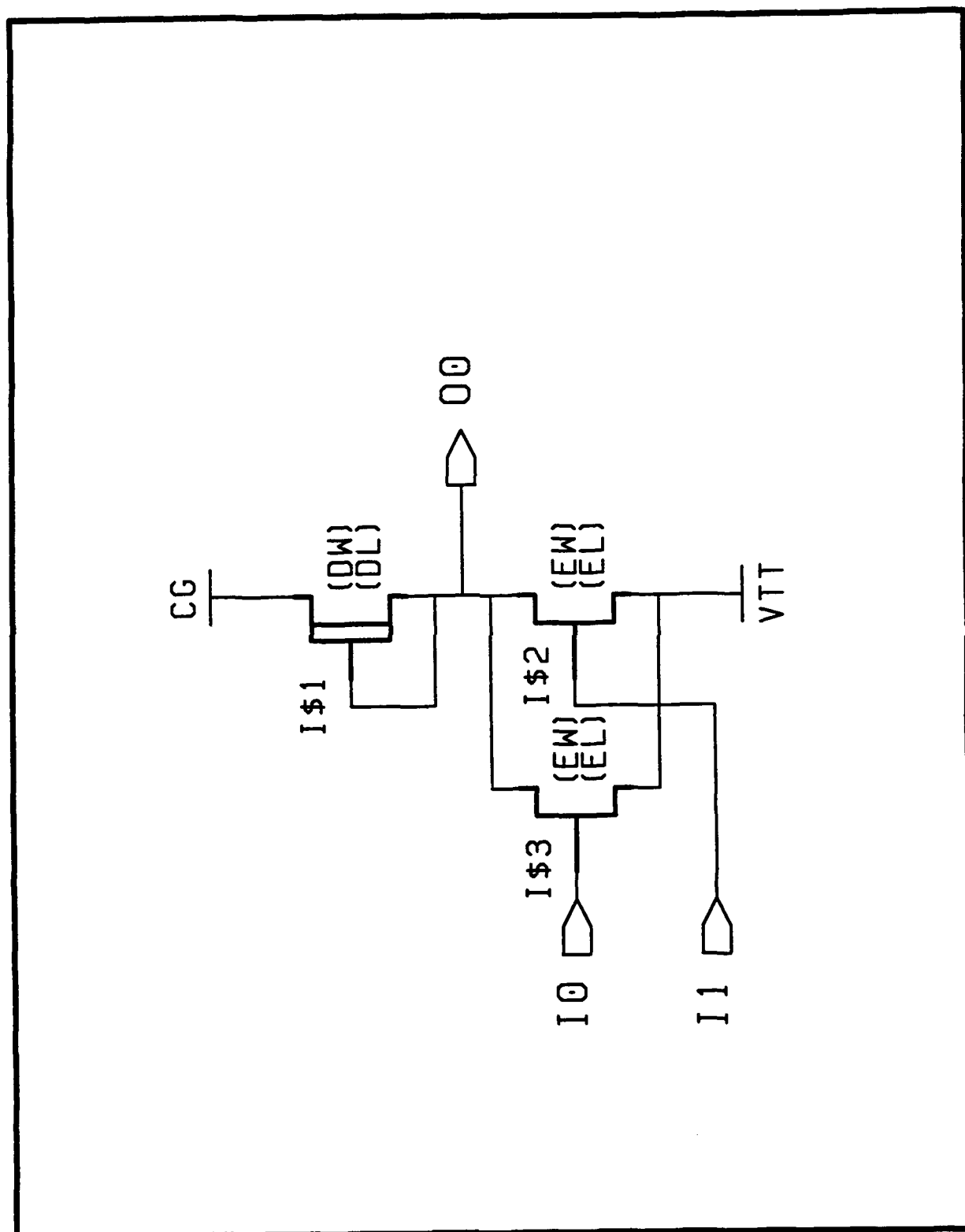
# LOGIC: ALU LOGIC FUNCTIONS

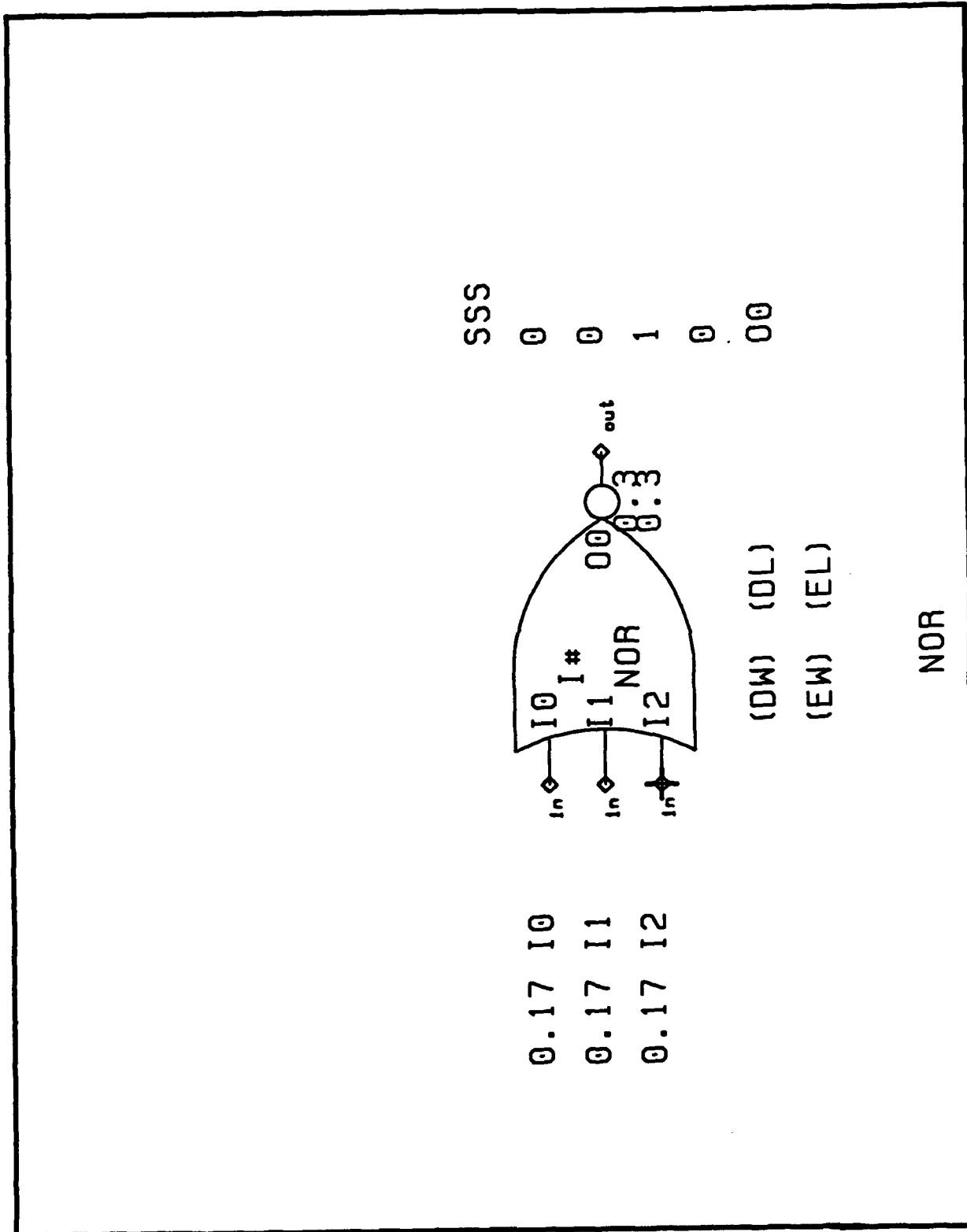


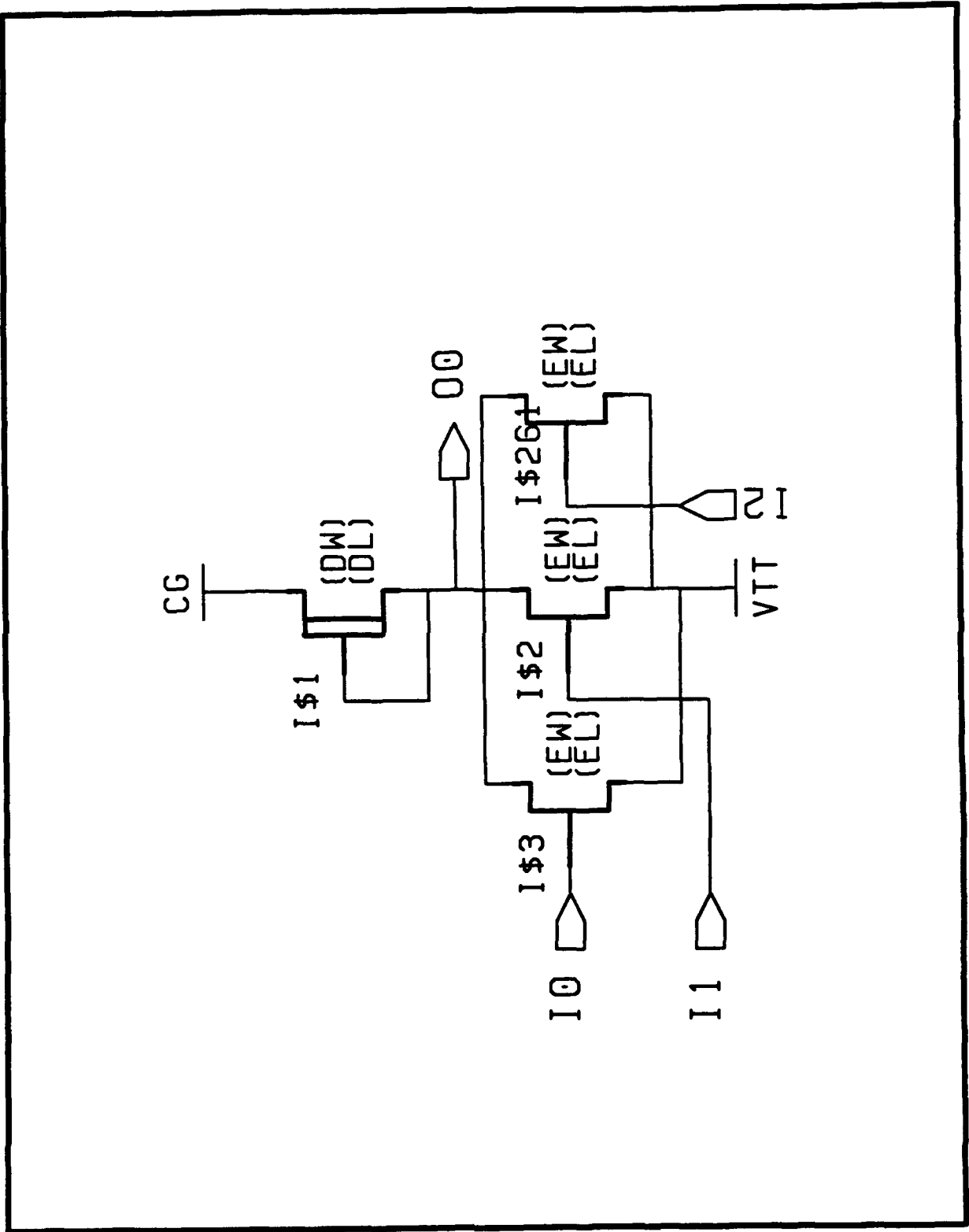




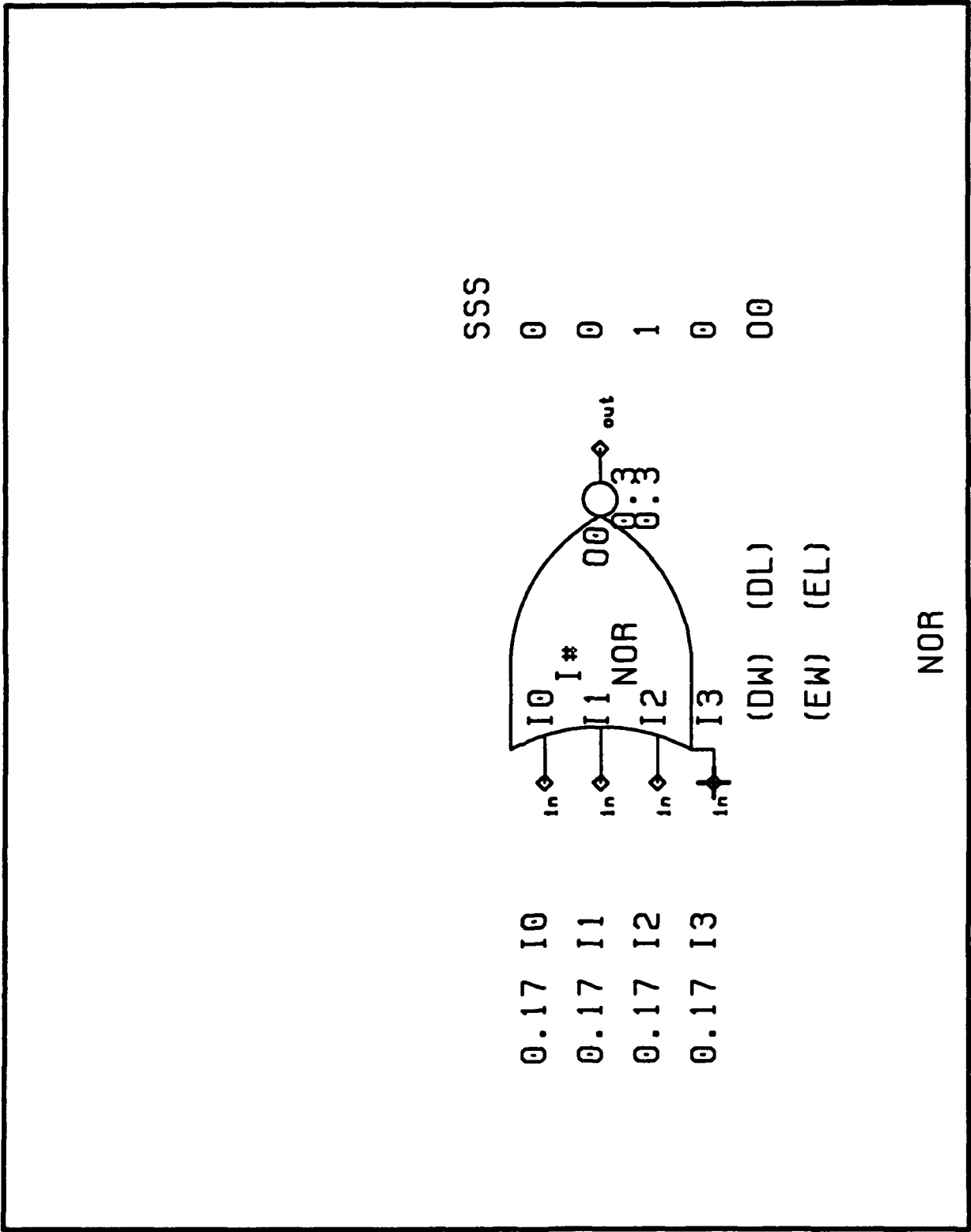


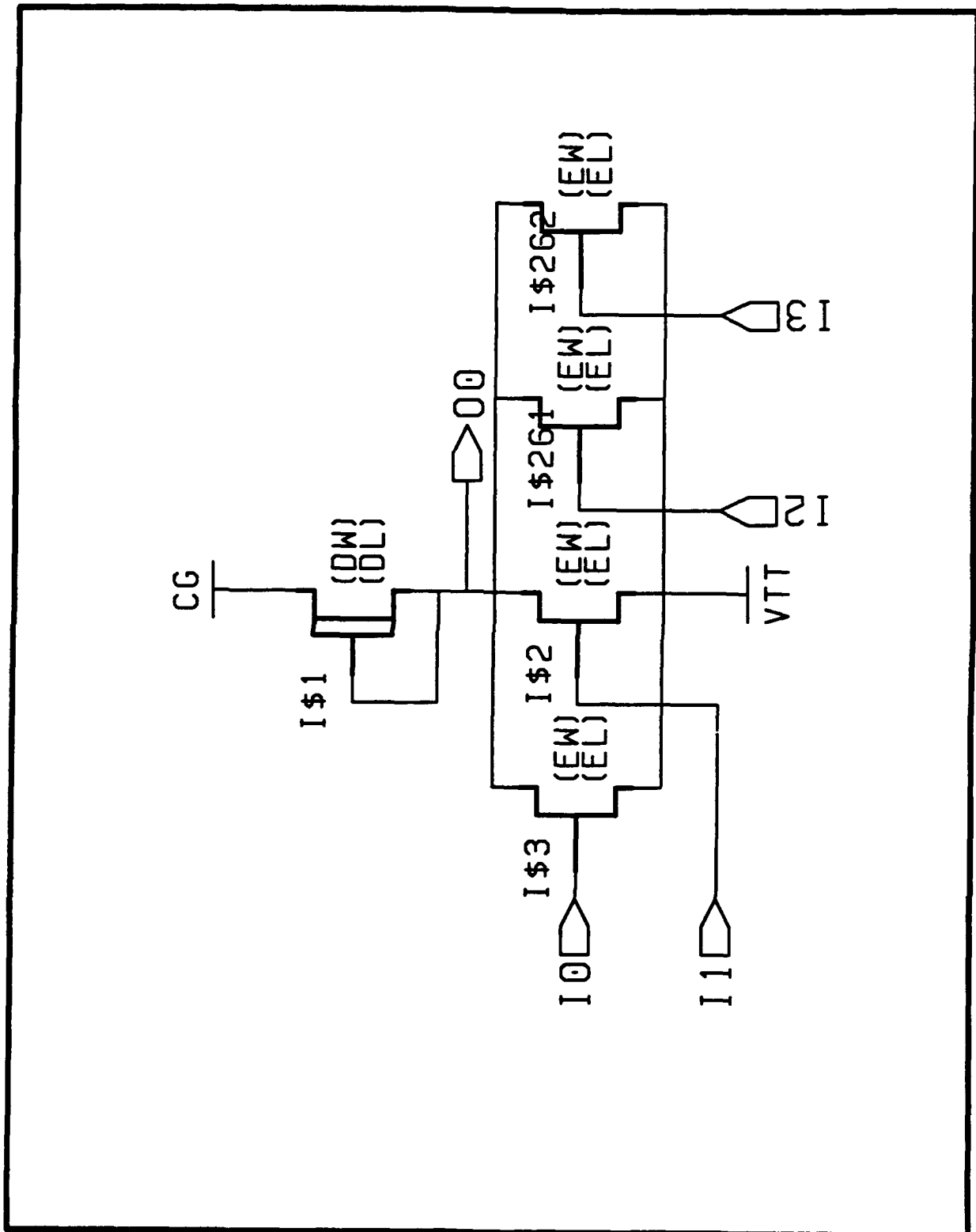


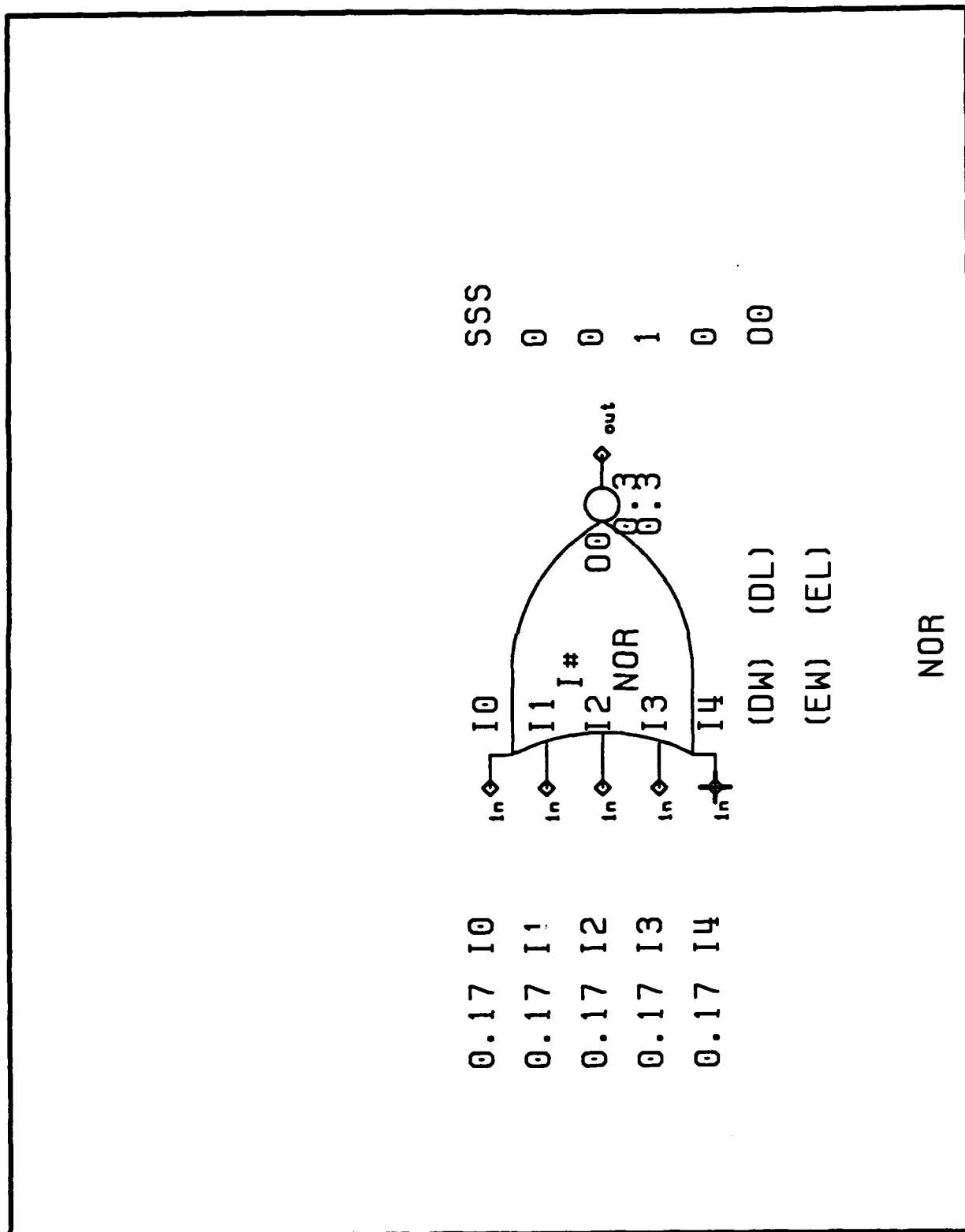


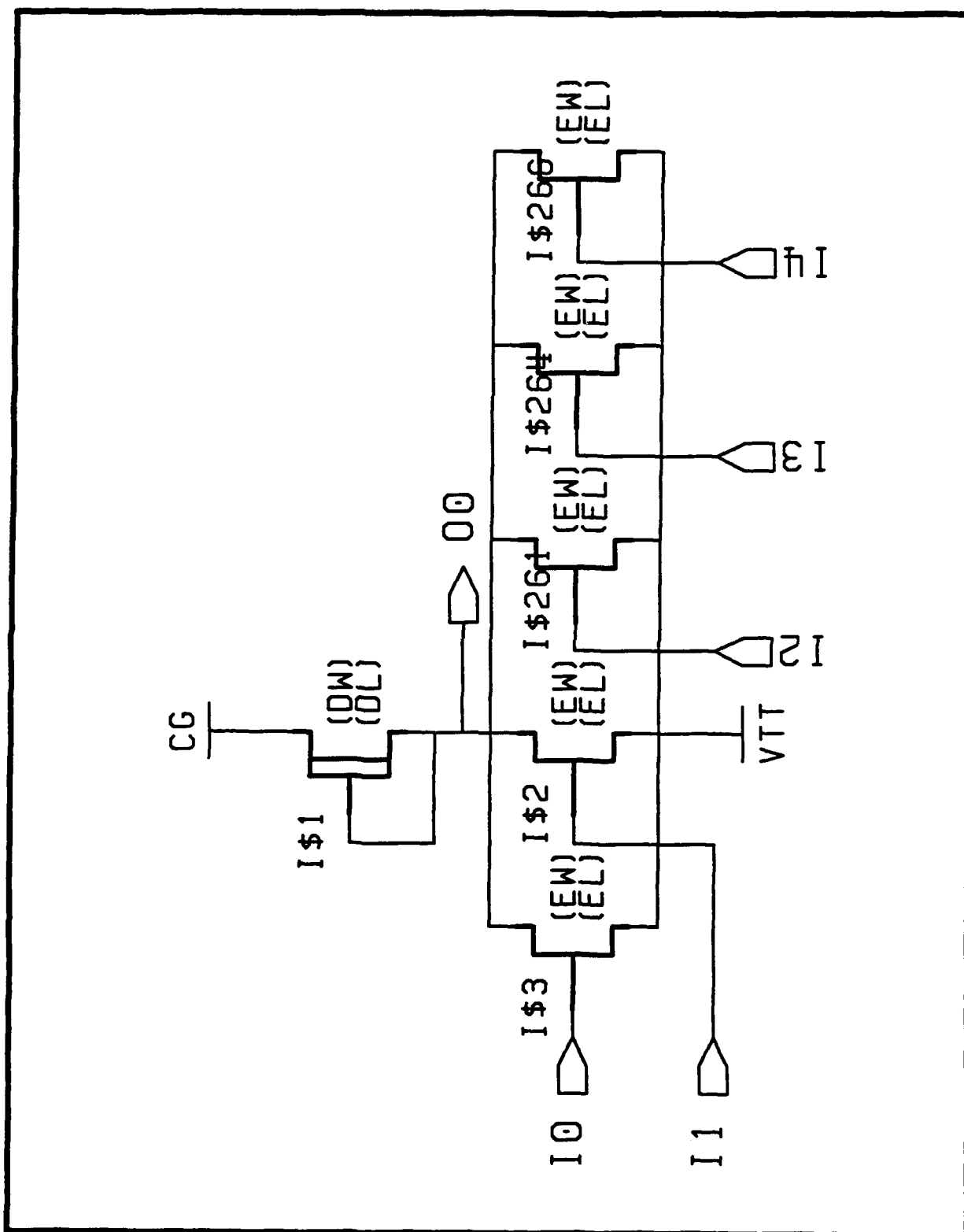


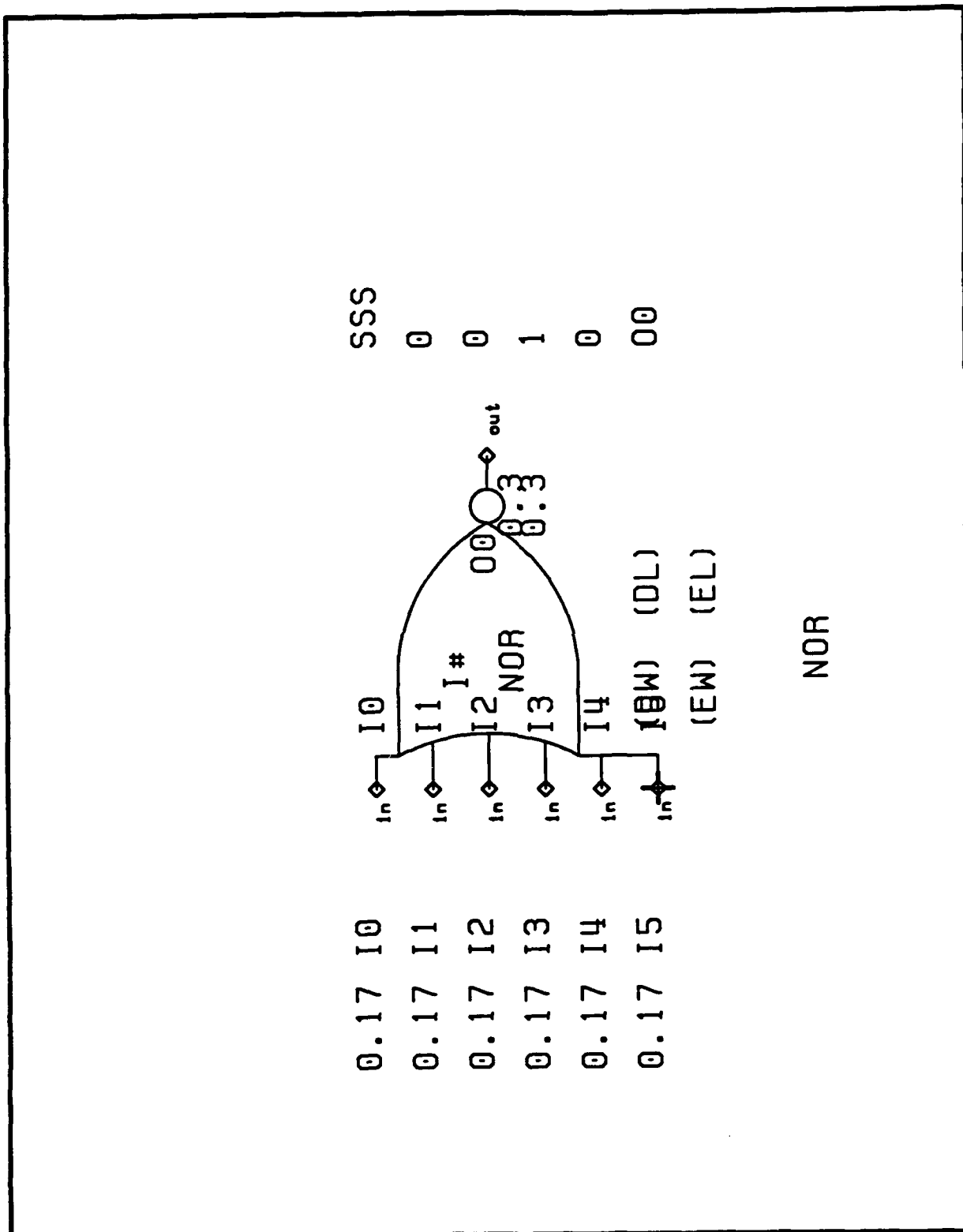


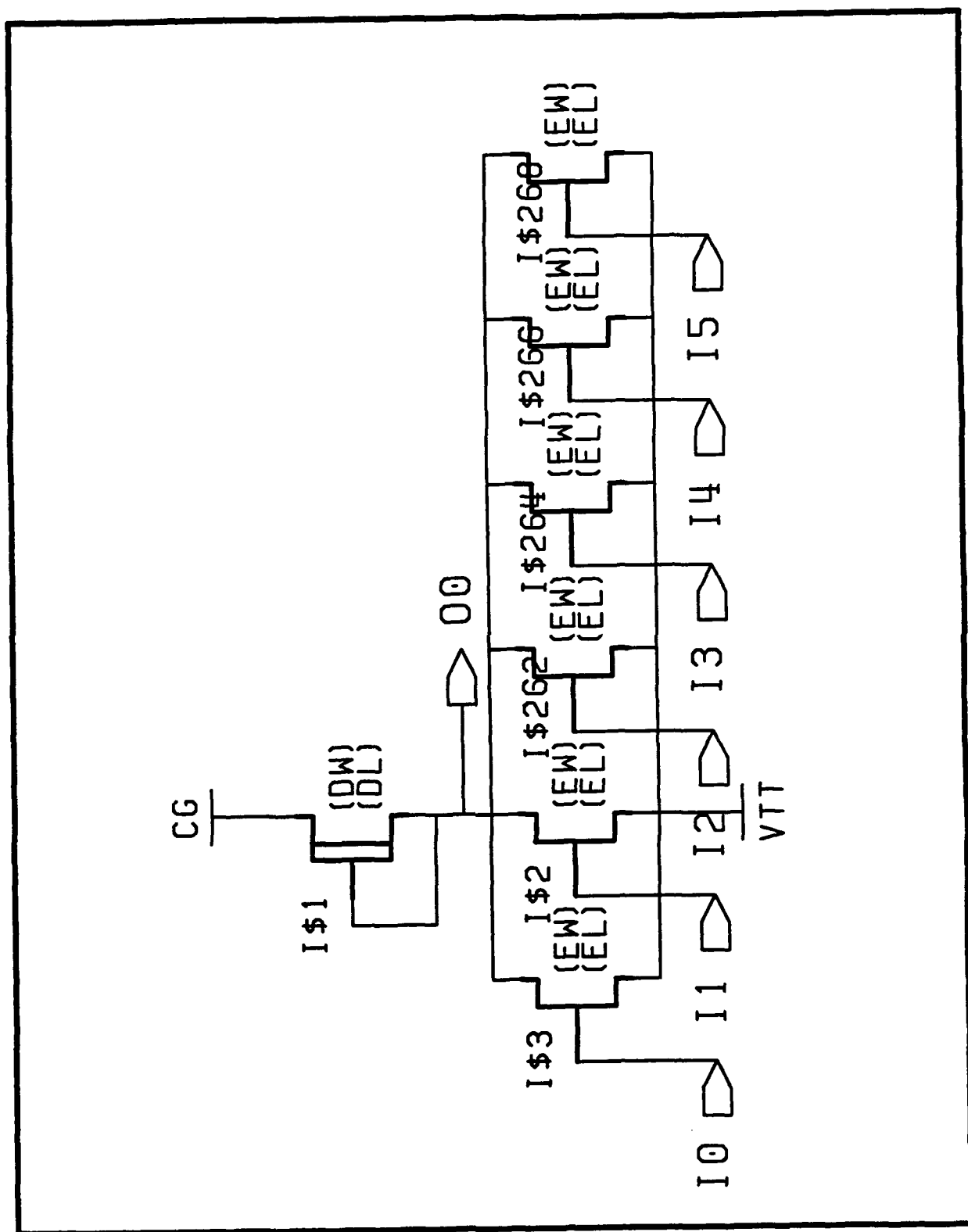


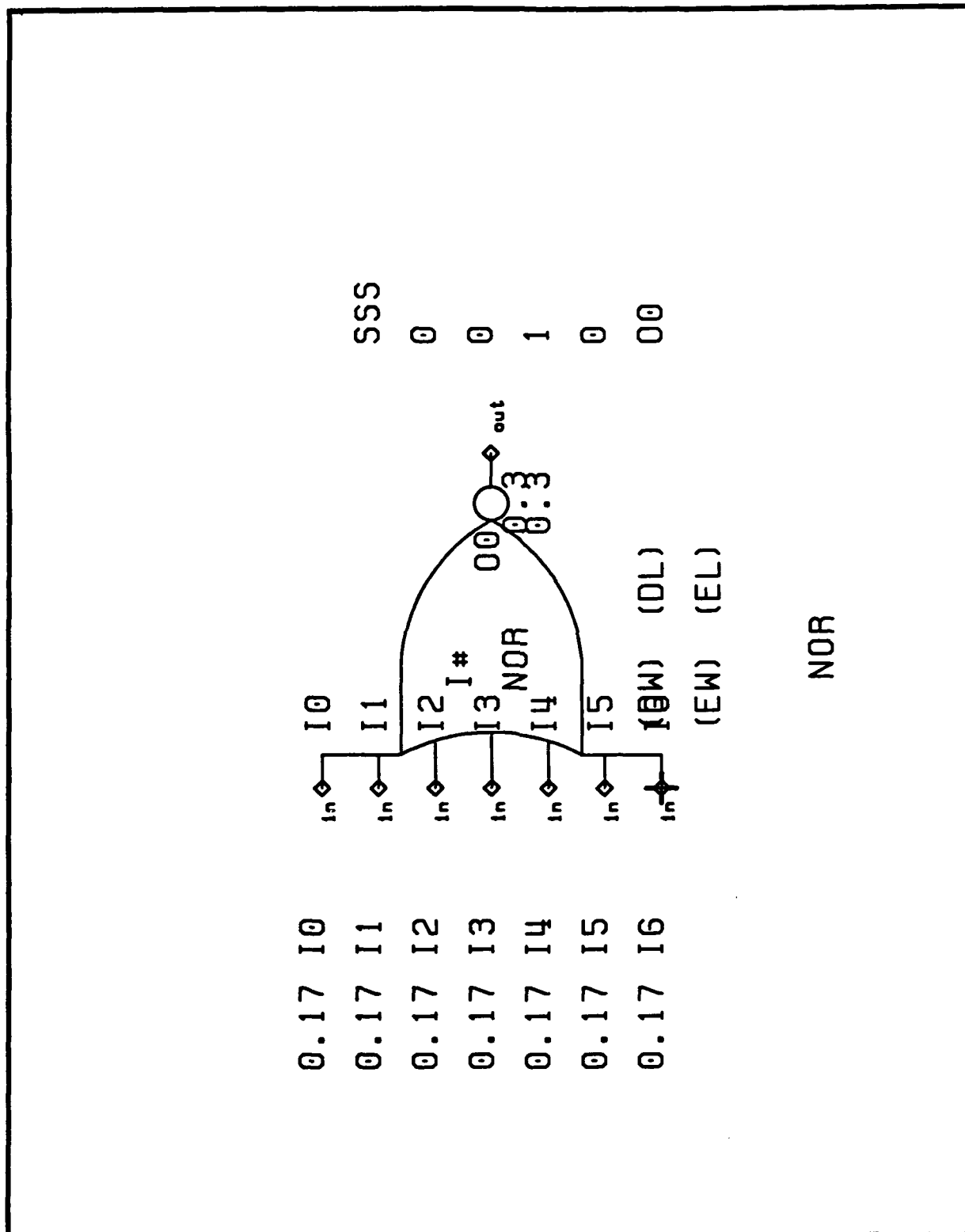


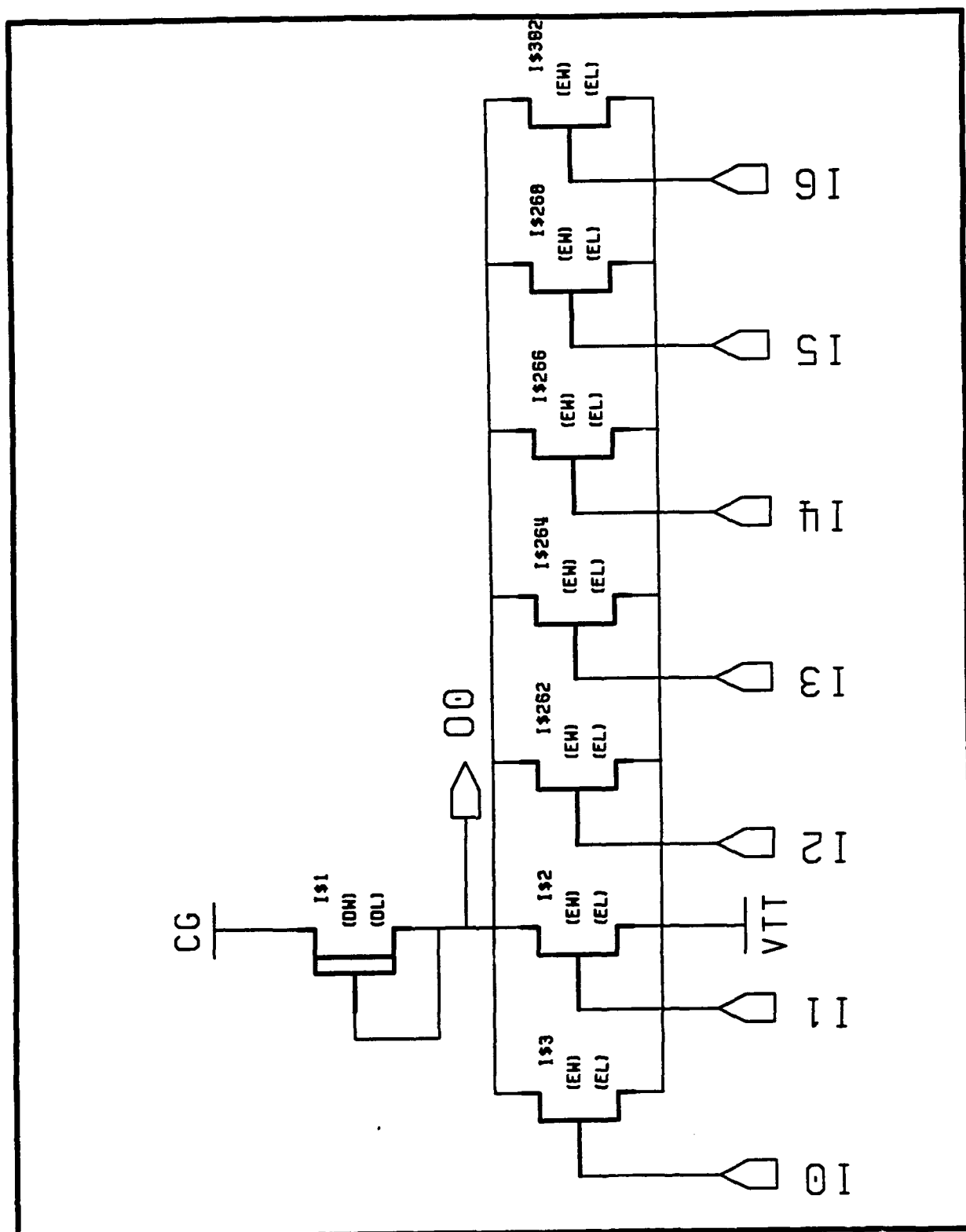




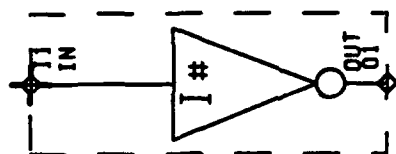


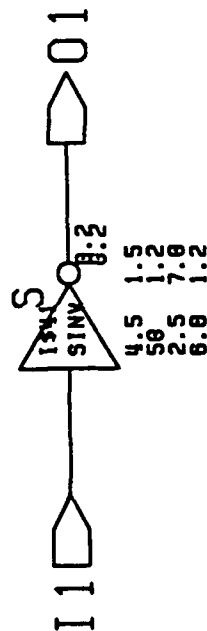


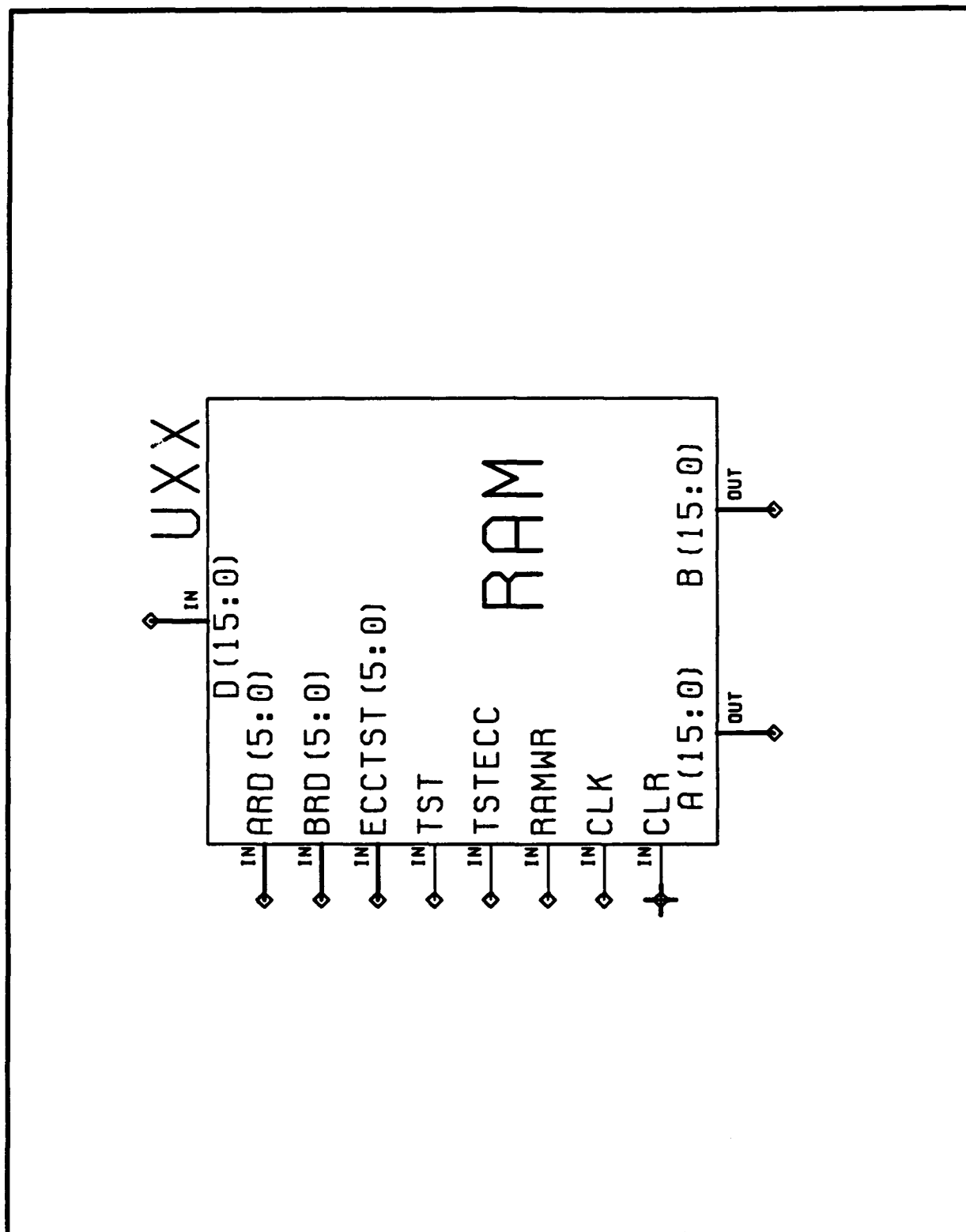


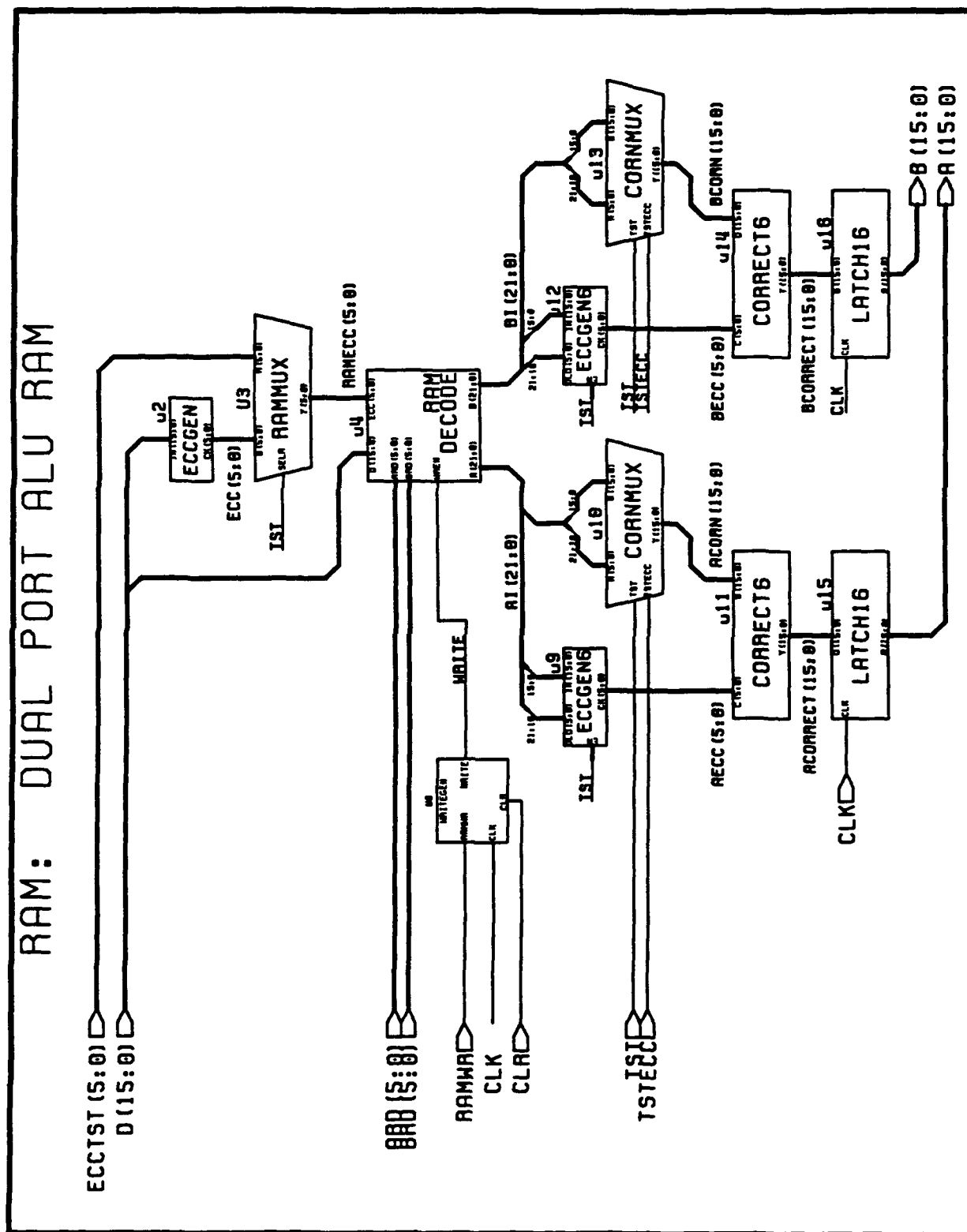


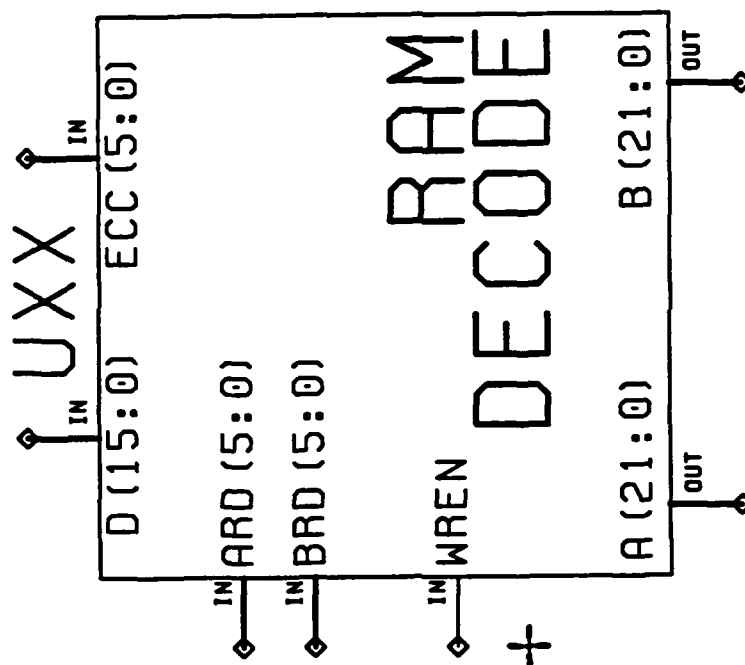


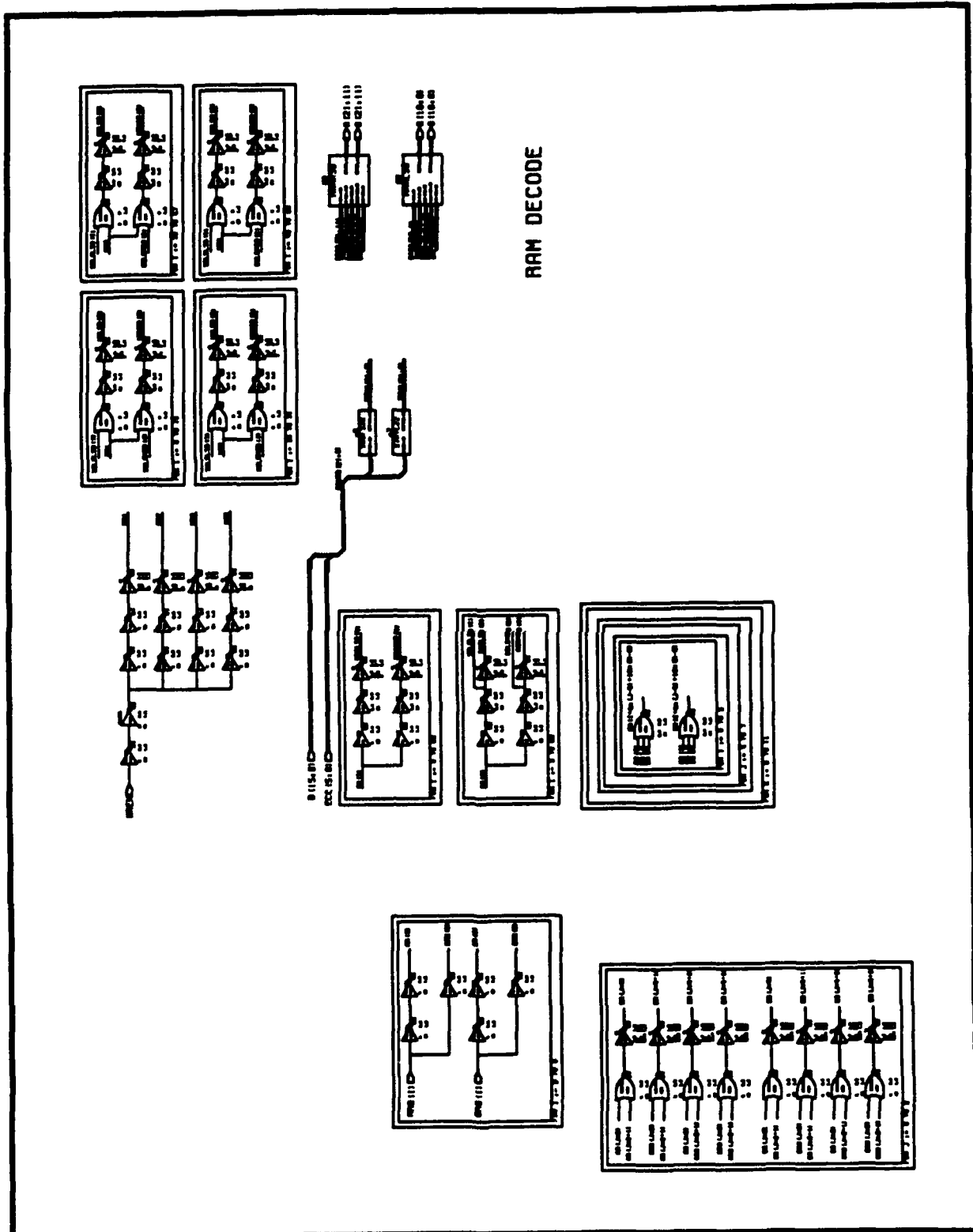


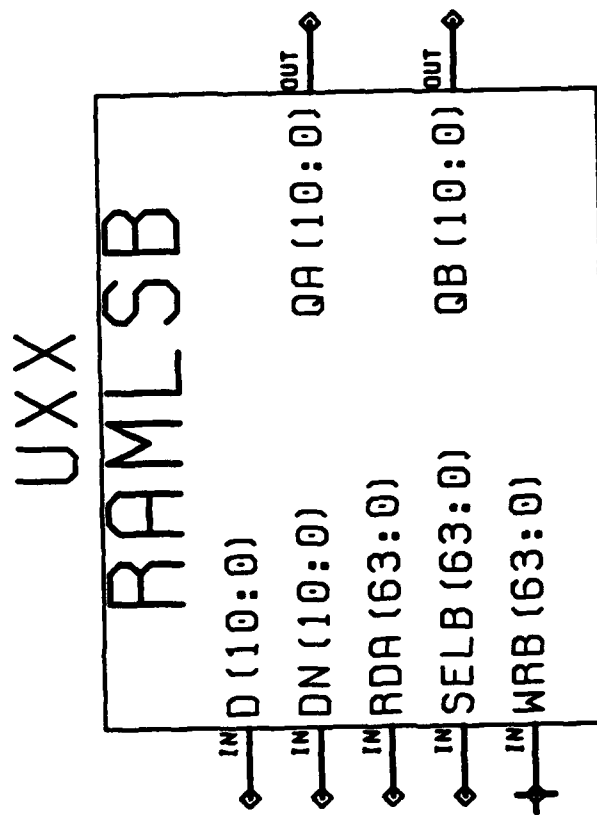


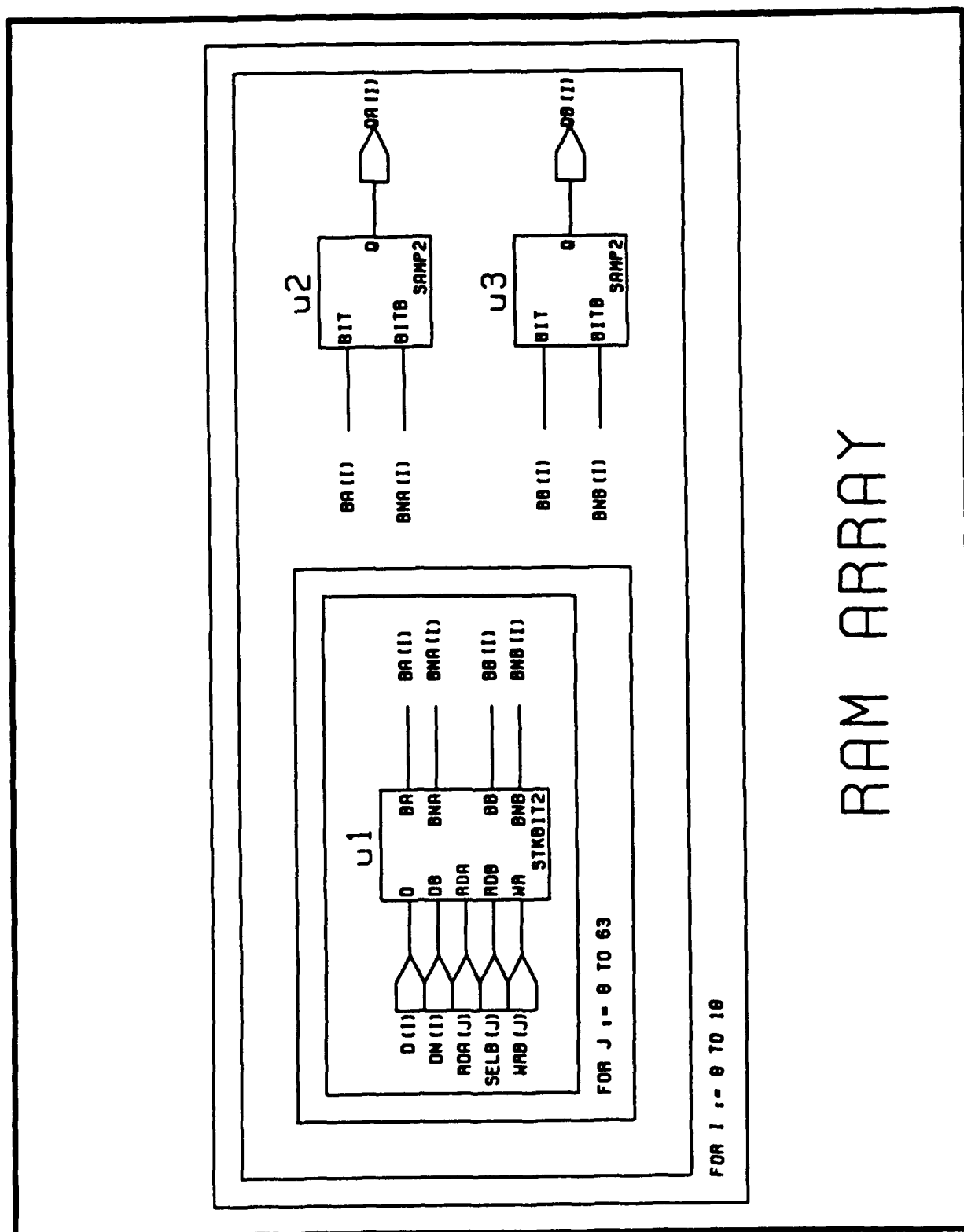




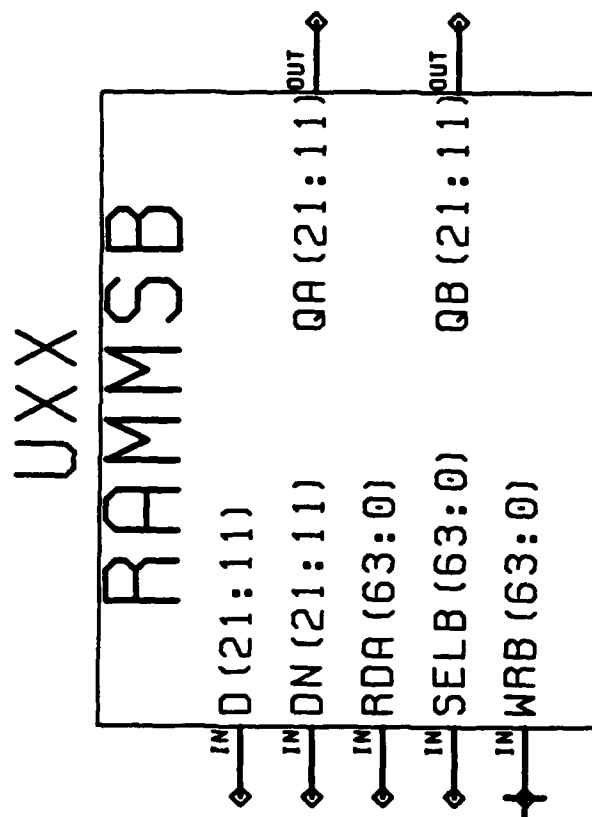


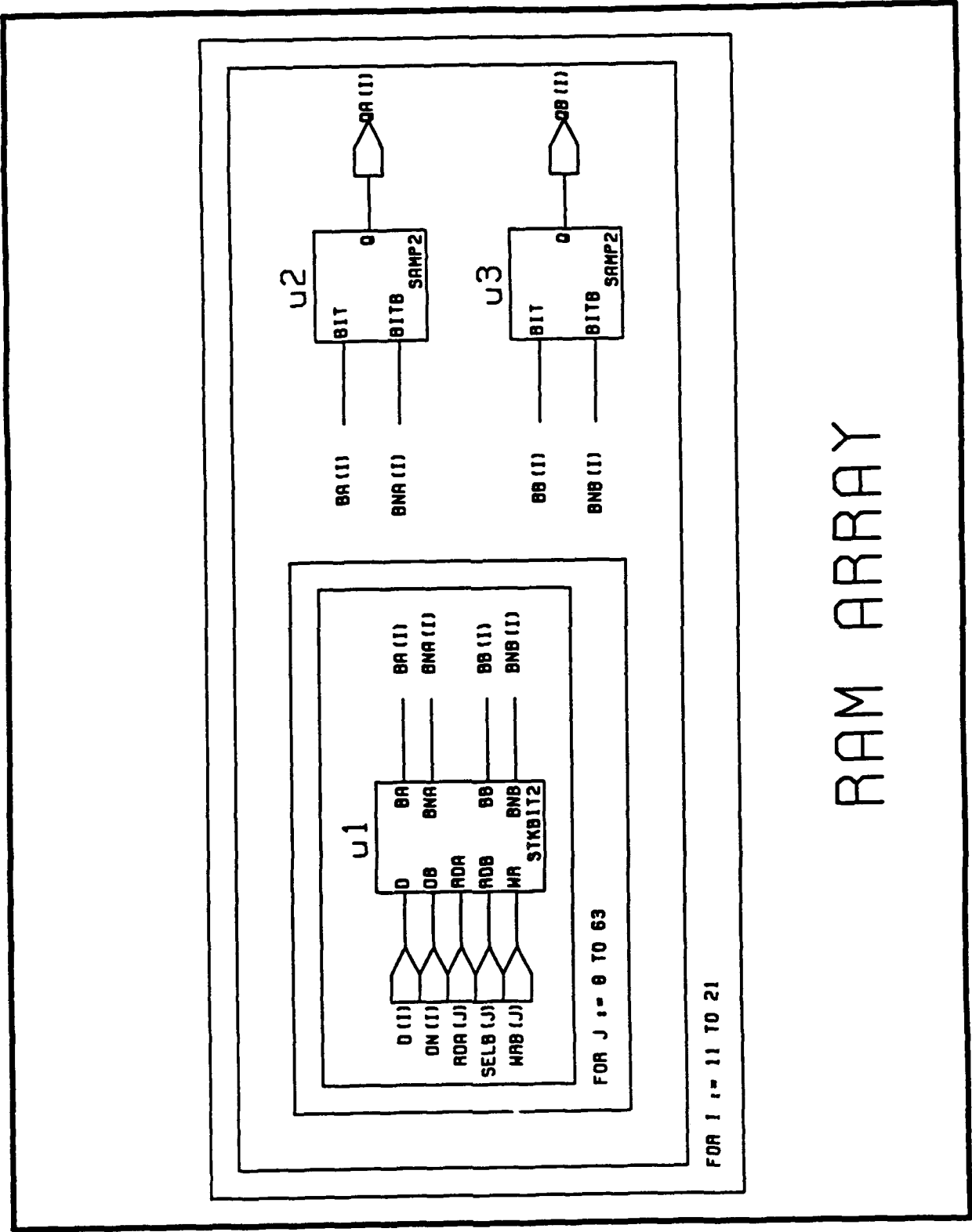


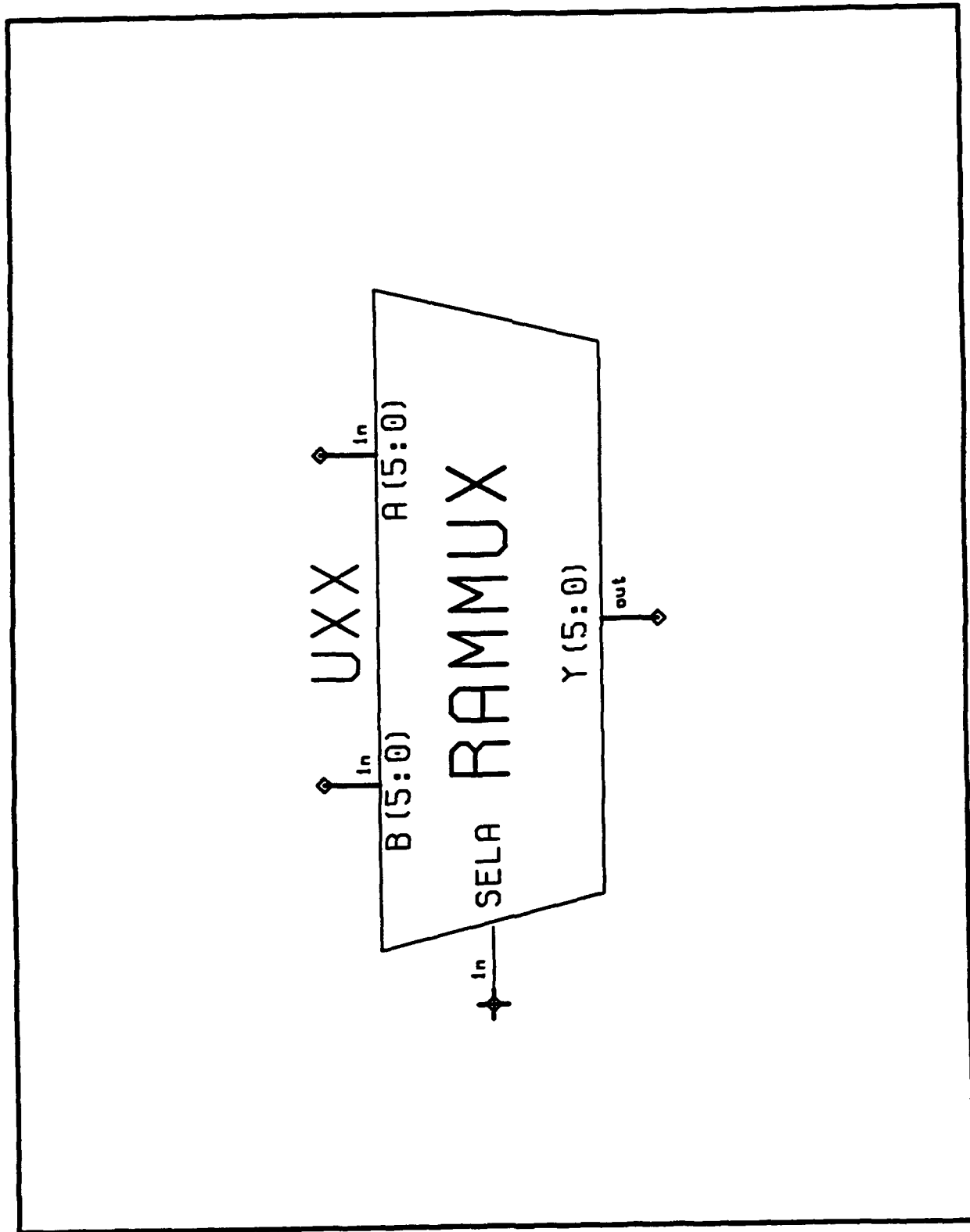


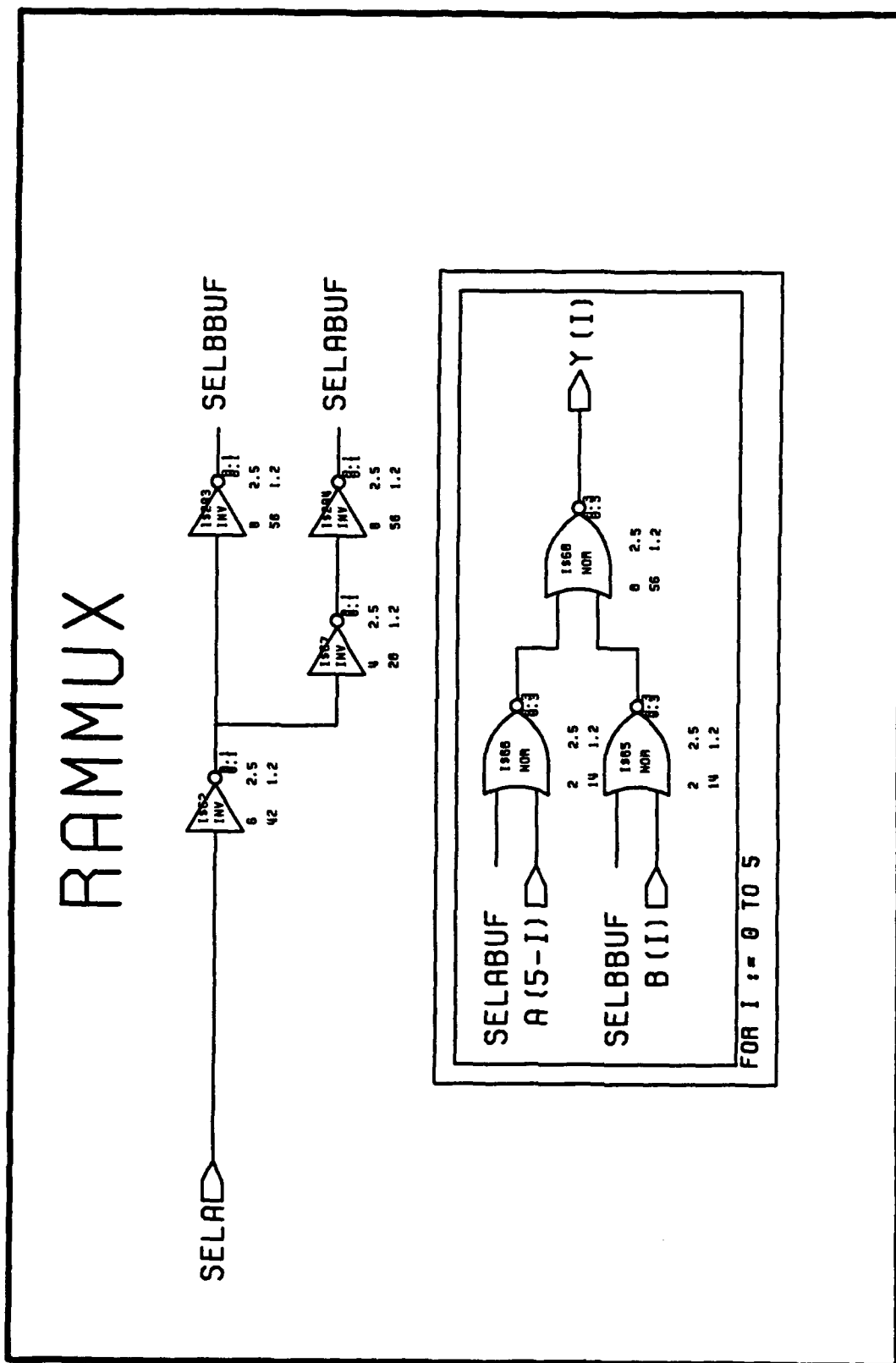








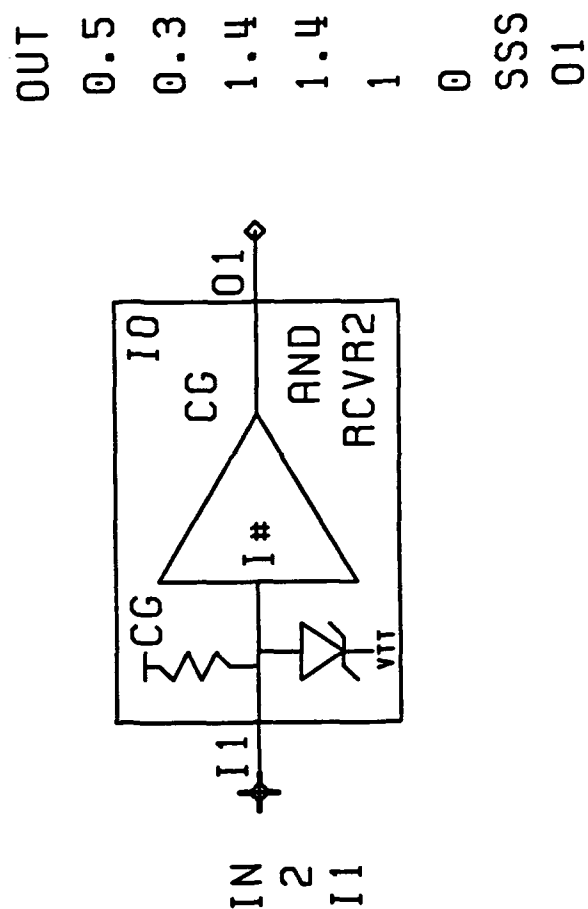


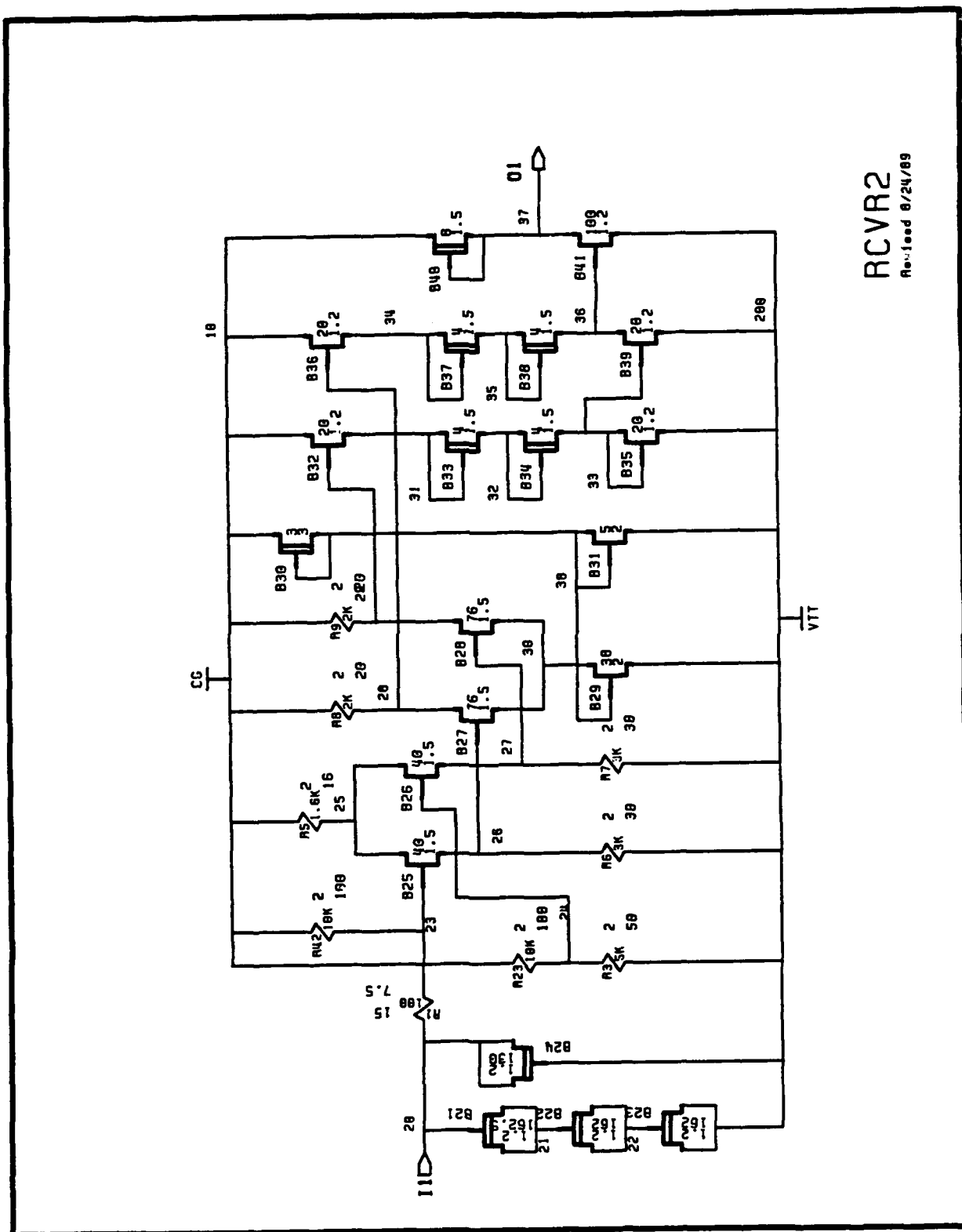


VITESSE GAAS CELL LIBRARY  
Version 0.8

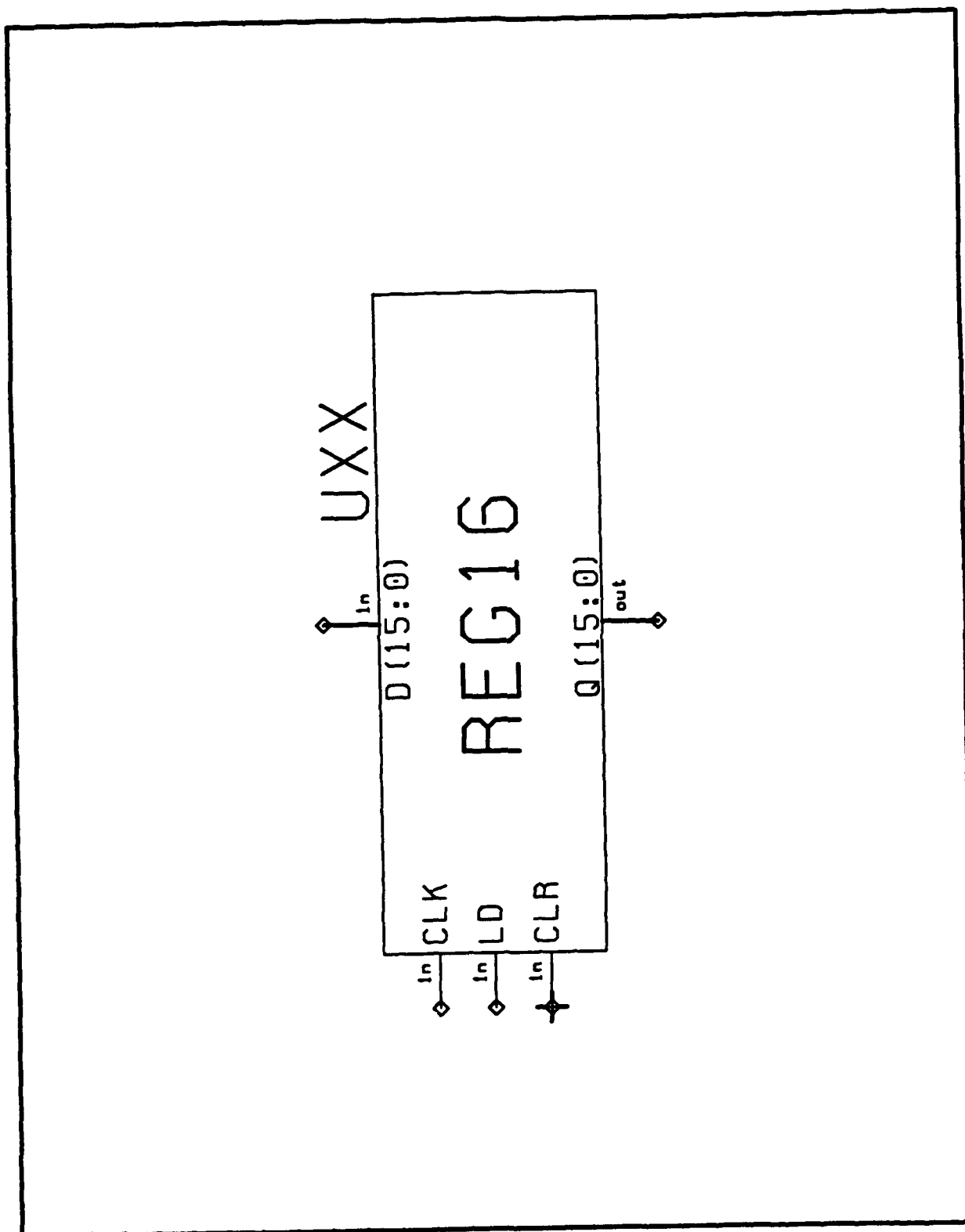
NAME: RCVR2

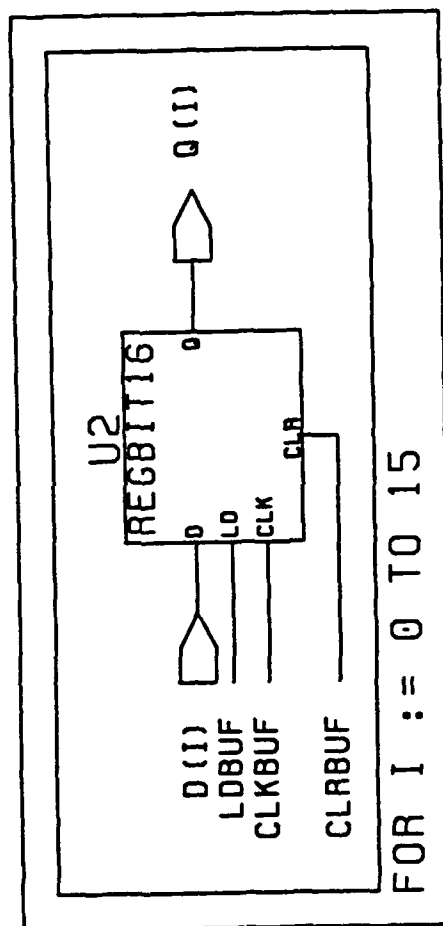
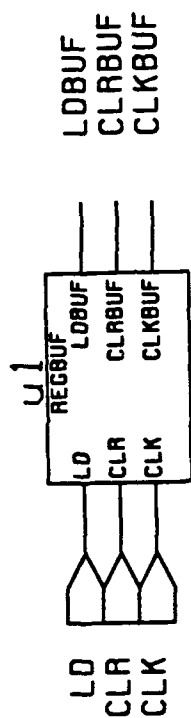
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD





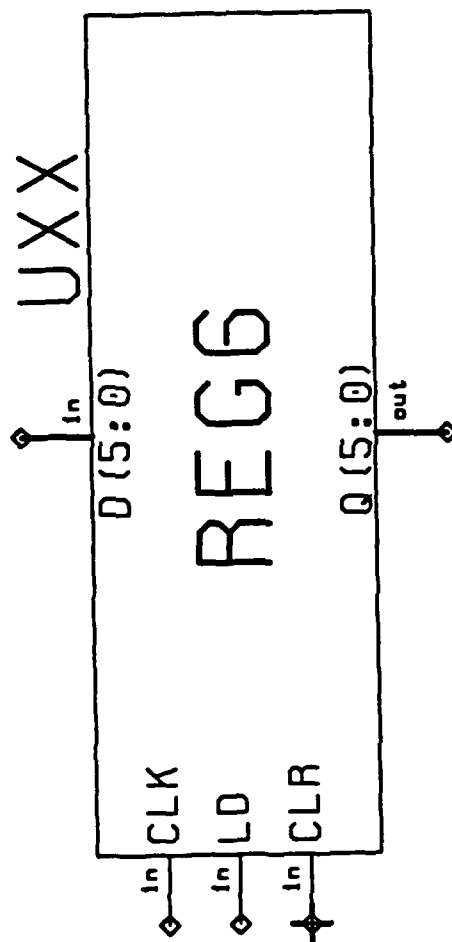
RCVR2  
Rev. 10/8/89

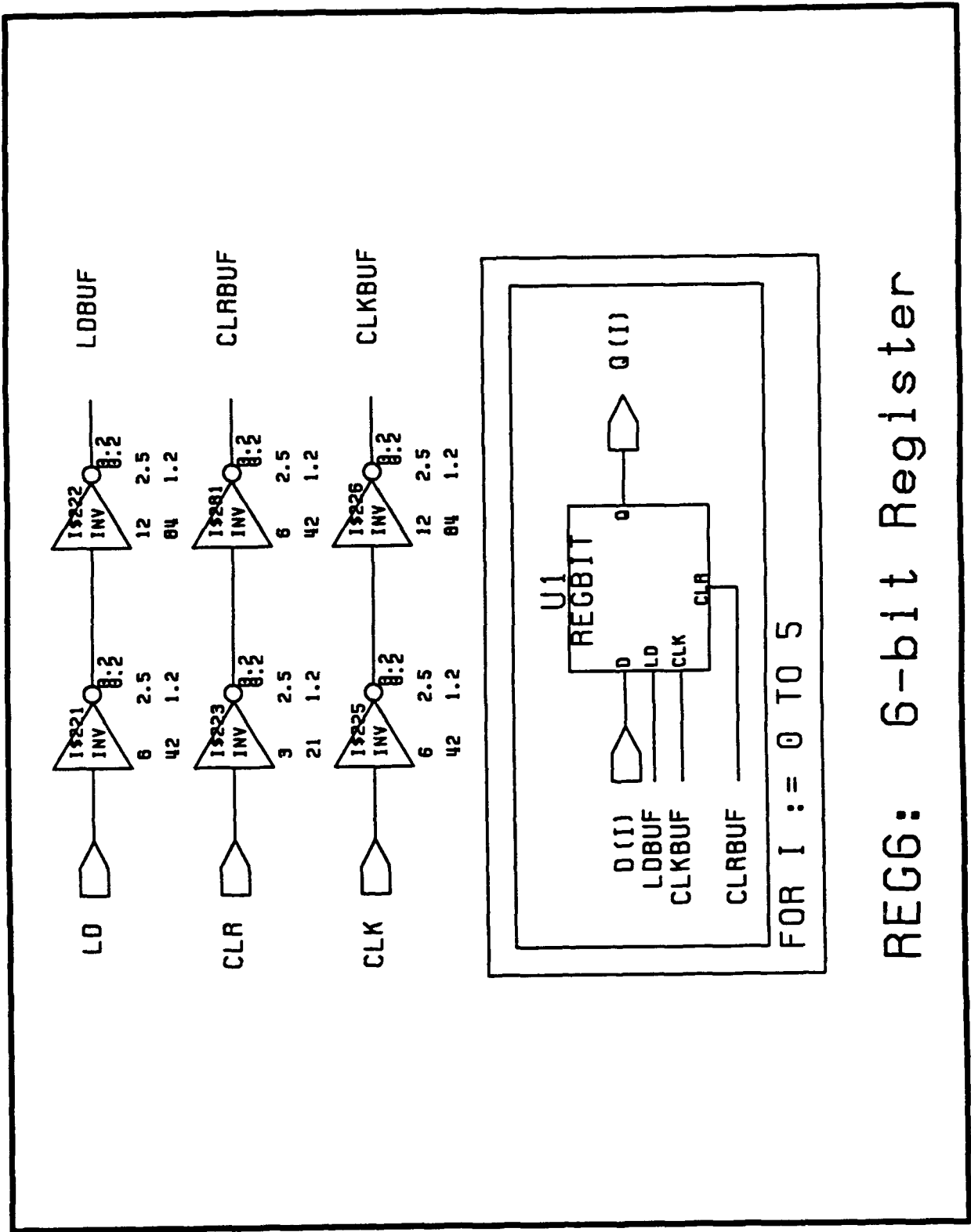




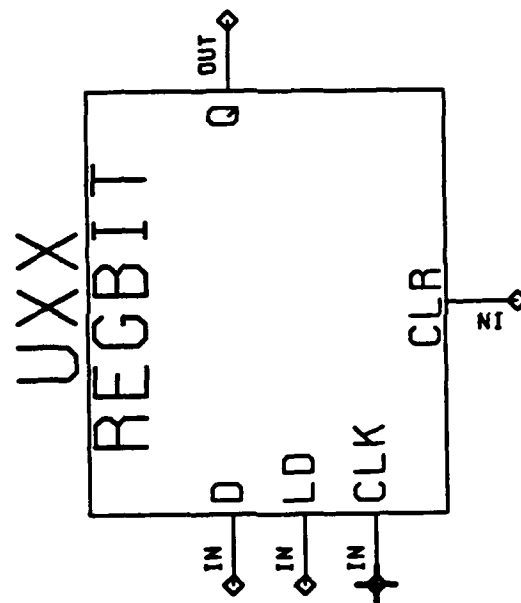
REG16: 16-bit Register

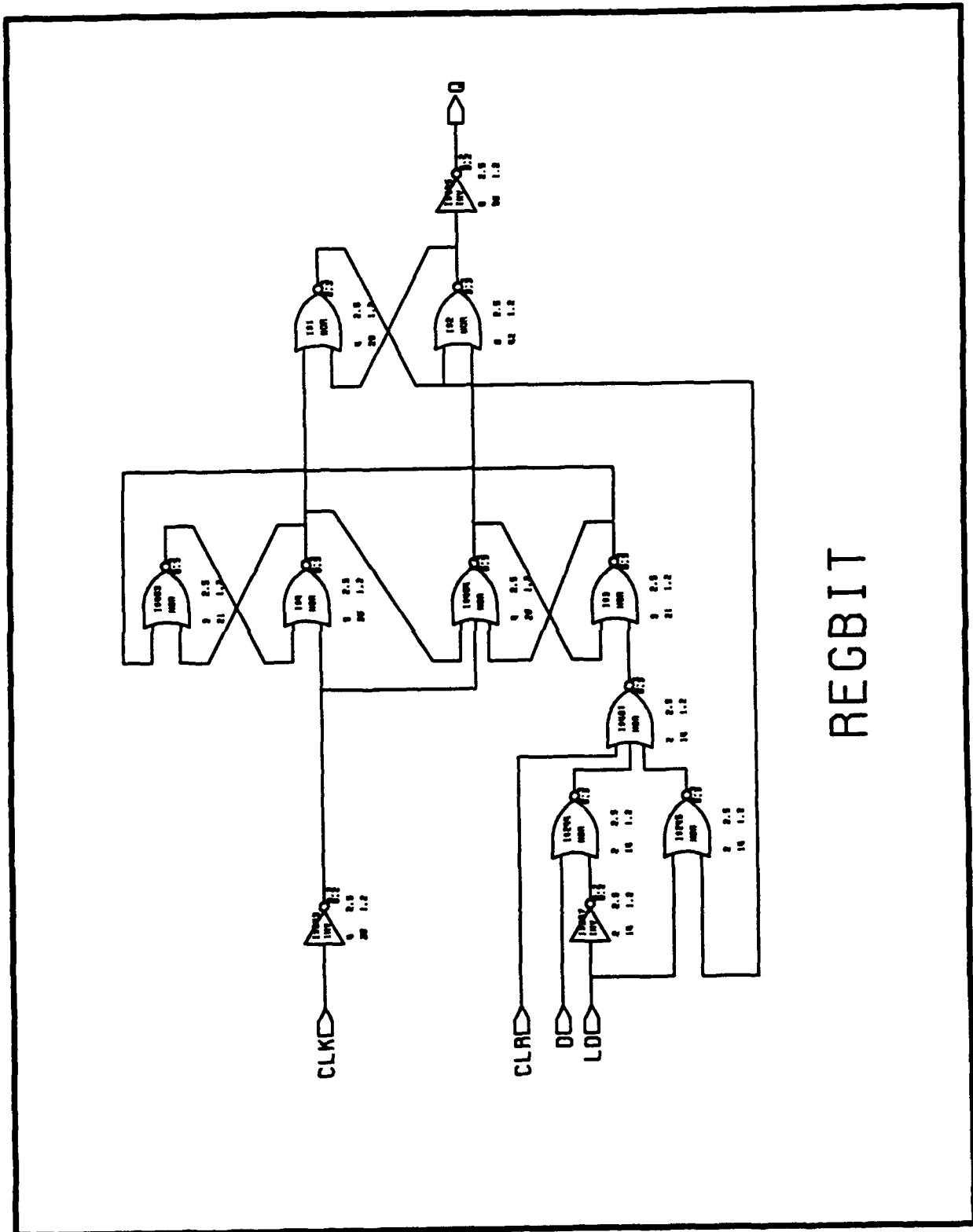


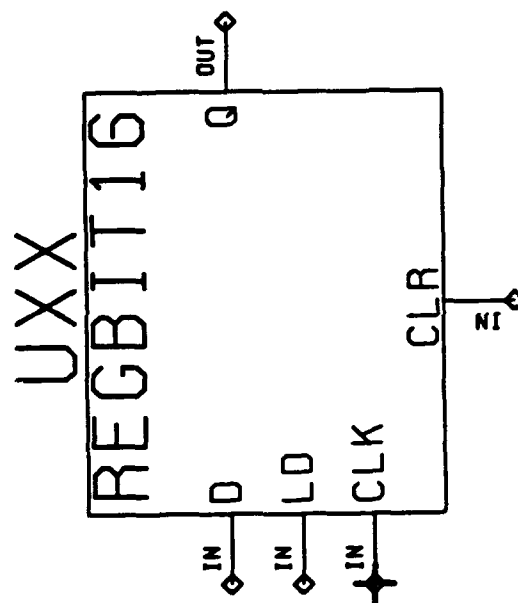


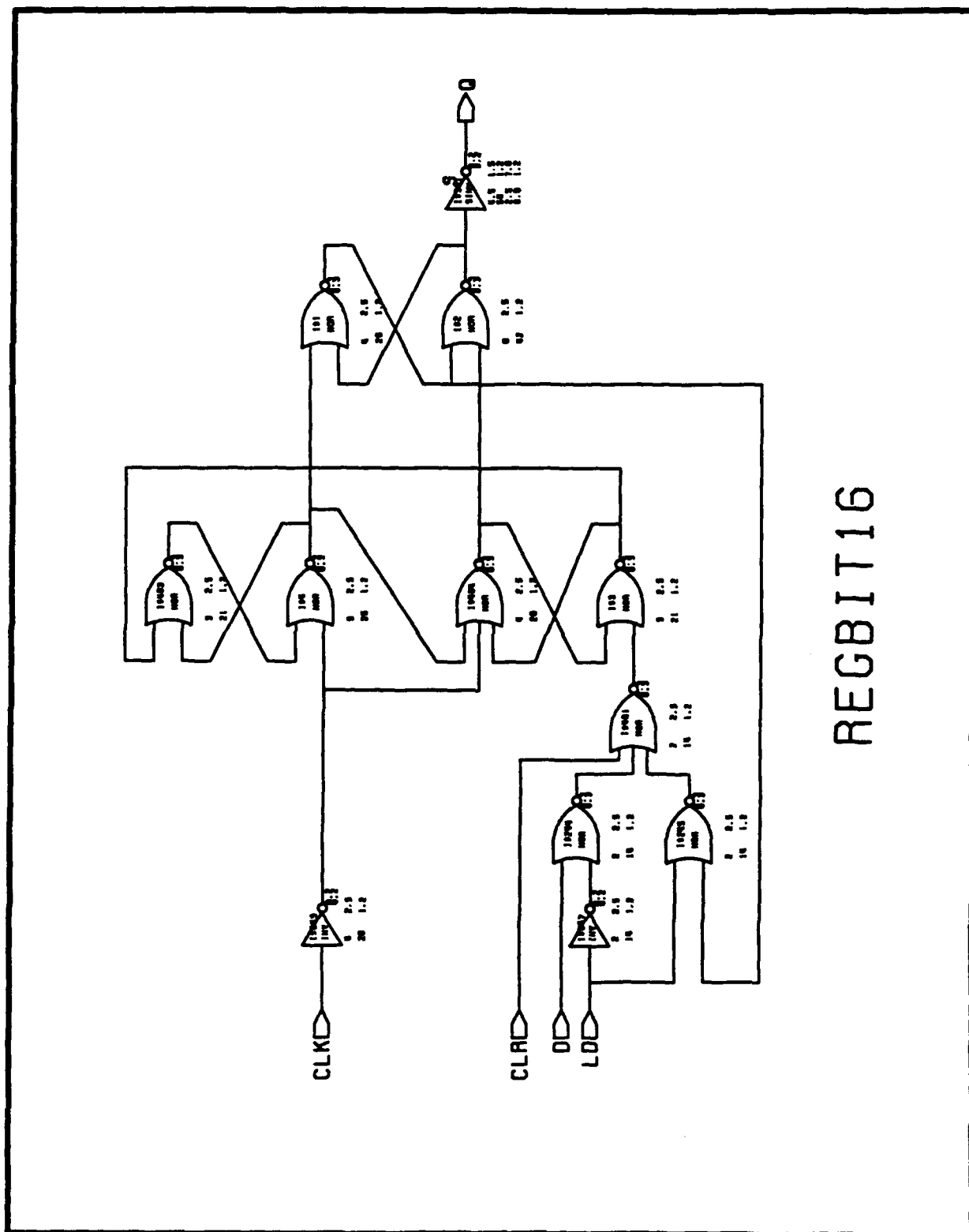


REG6: 6-bit Register

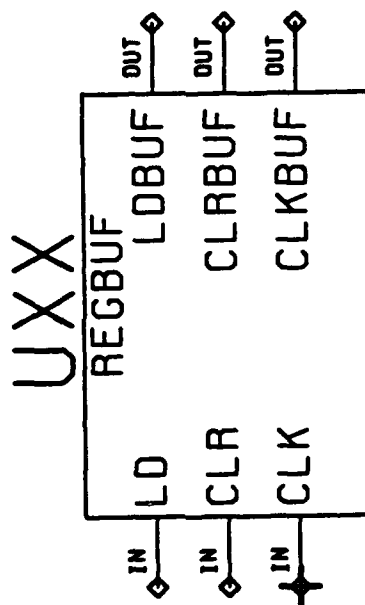


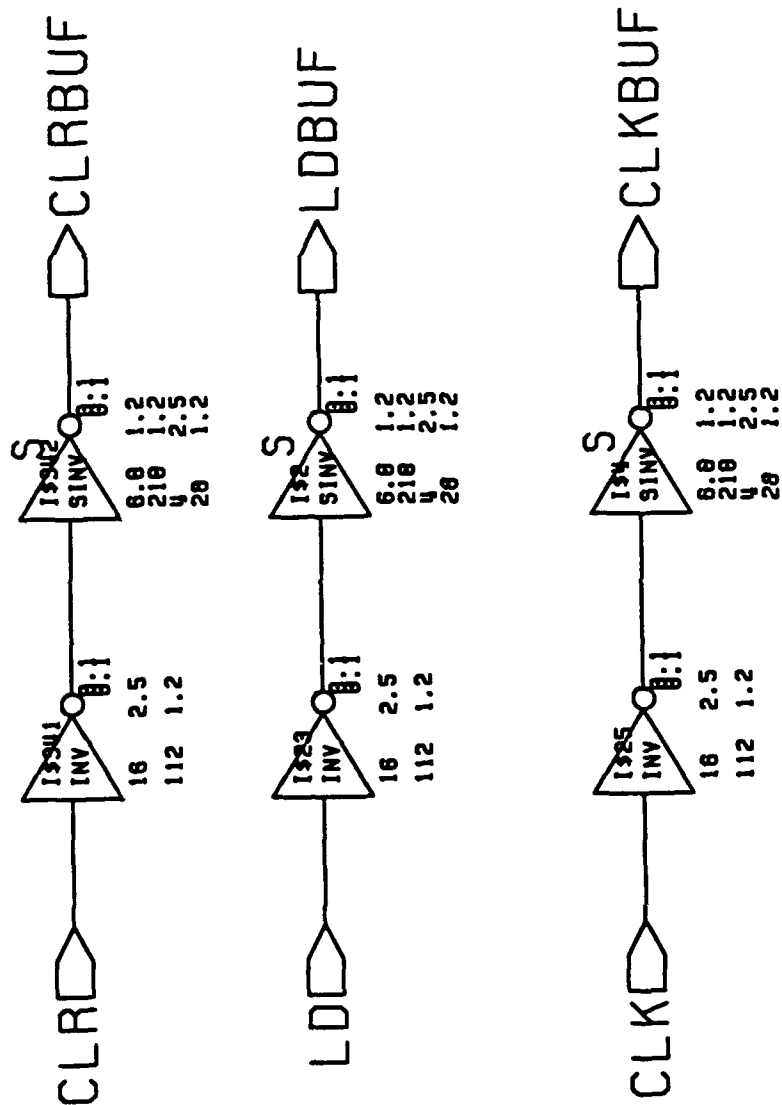






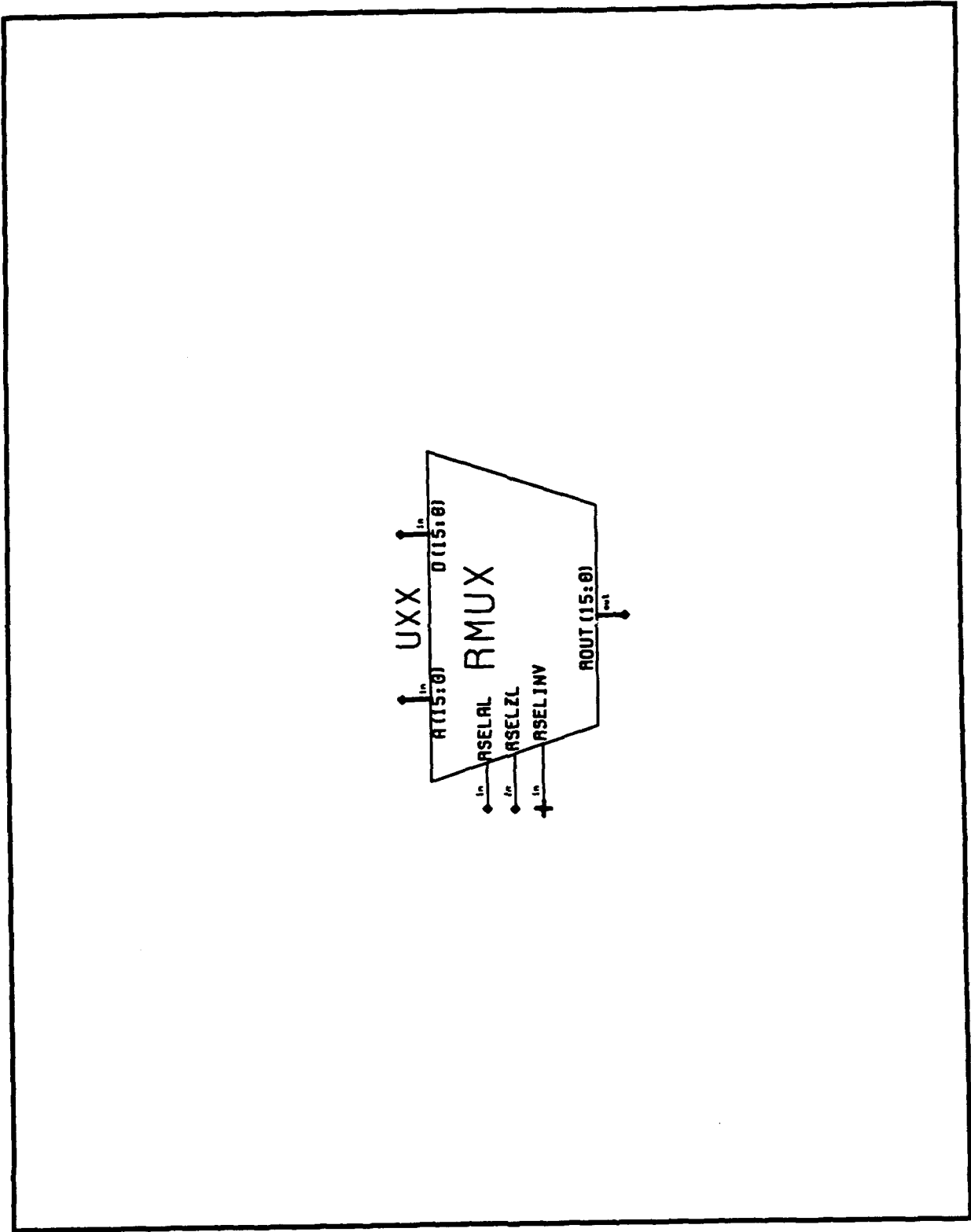
REGBIT16



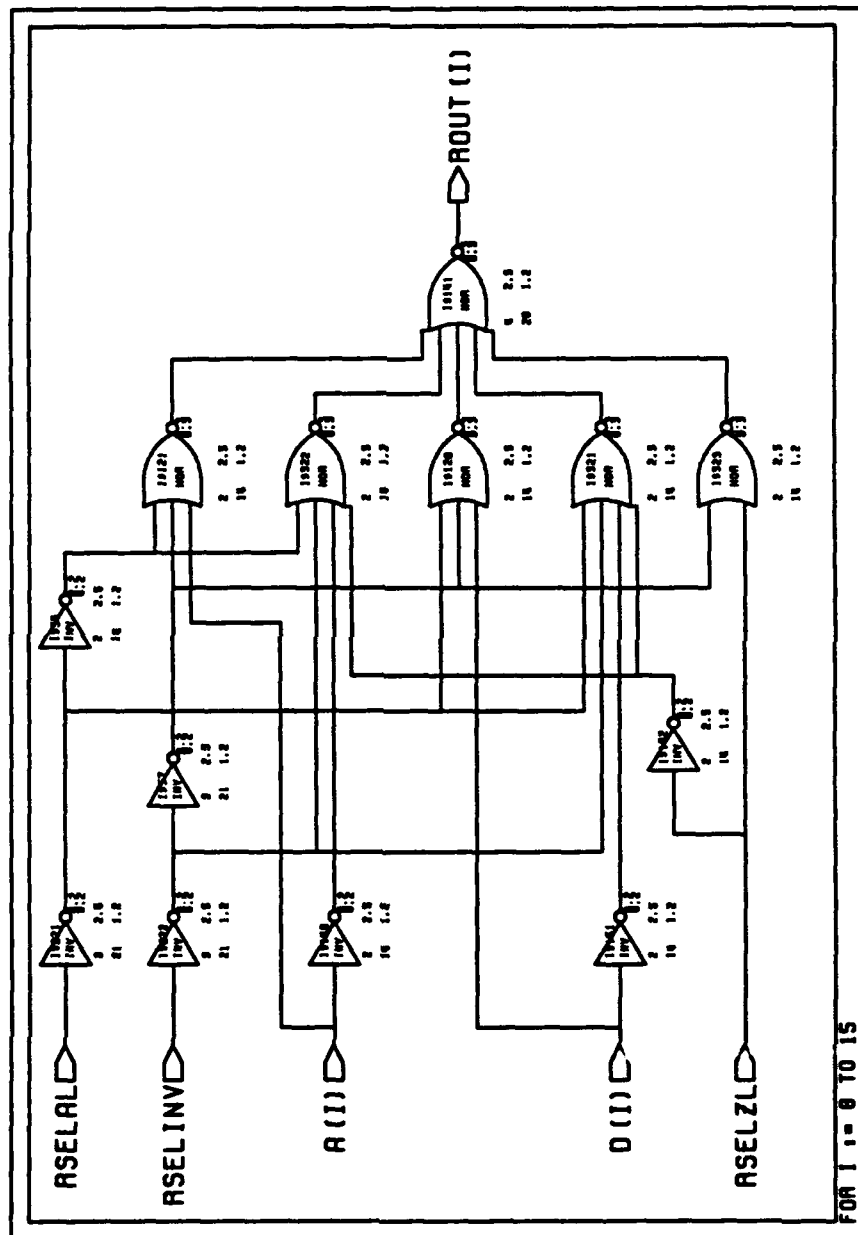


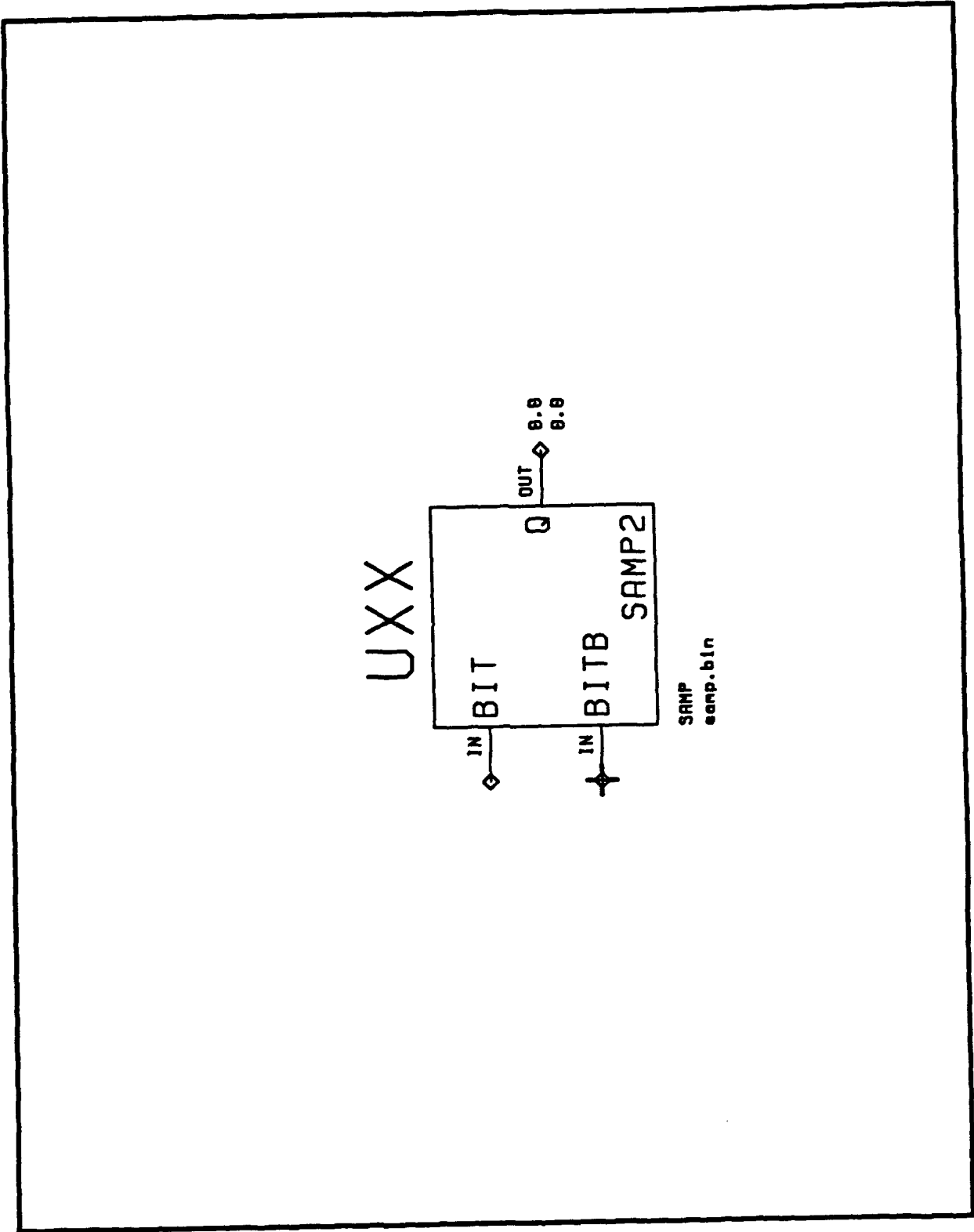
REGBUF: buffer for REGBIT

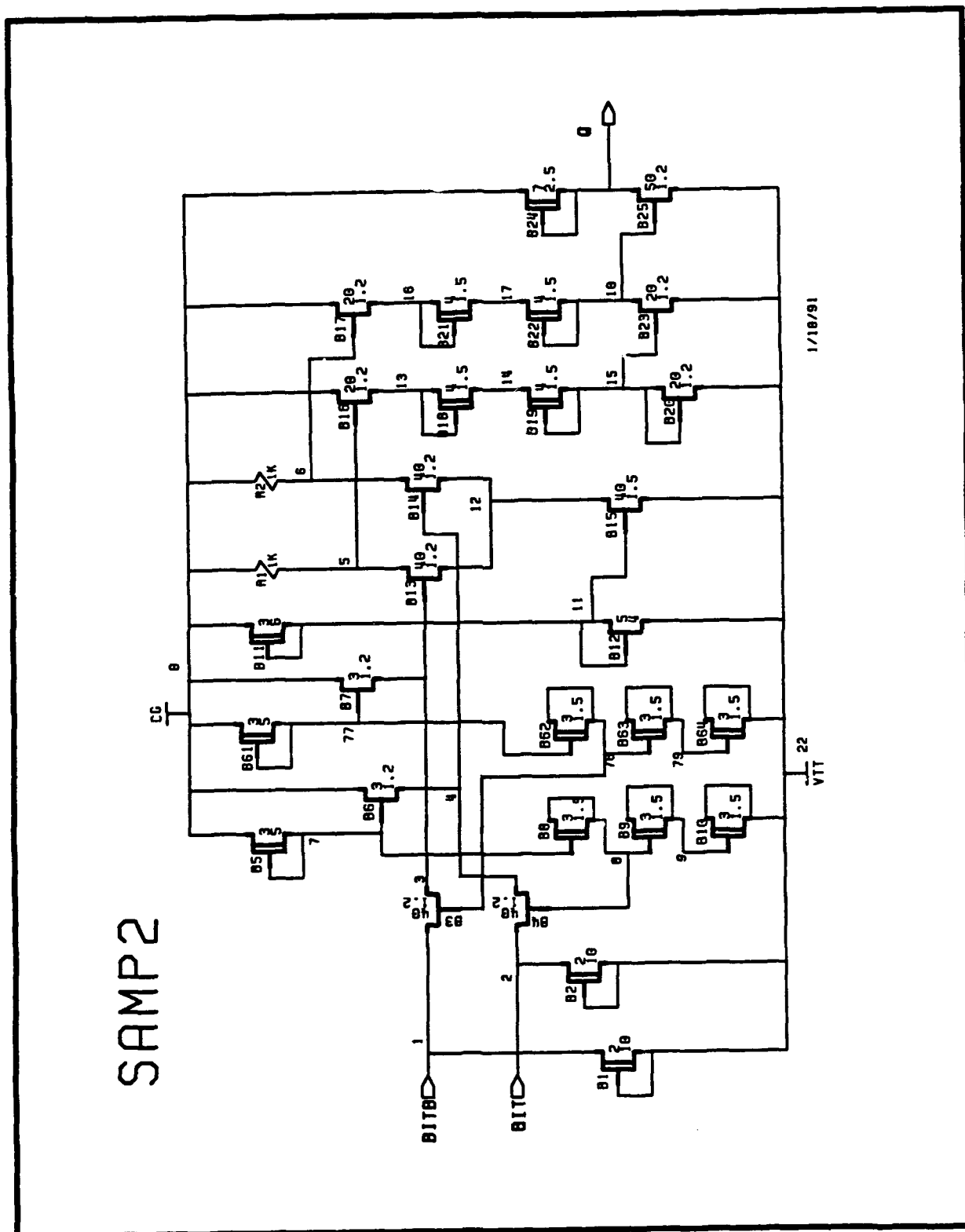


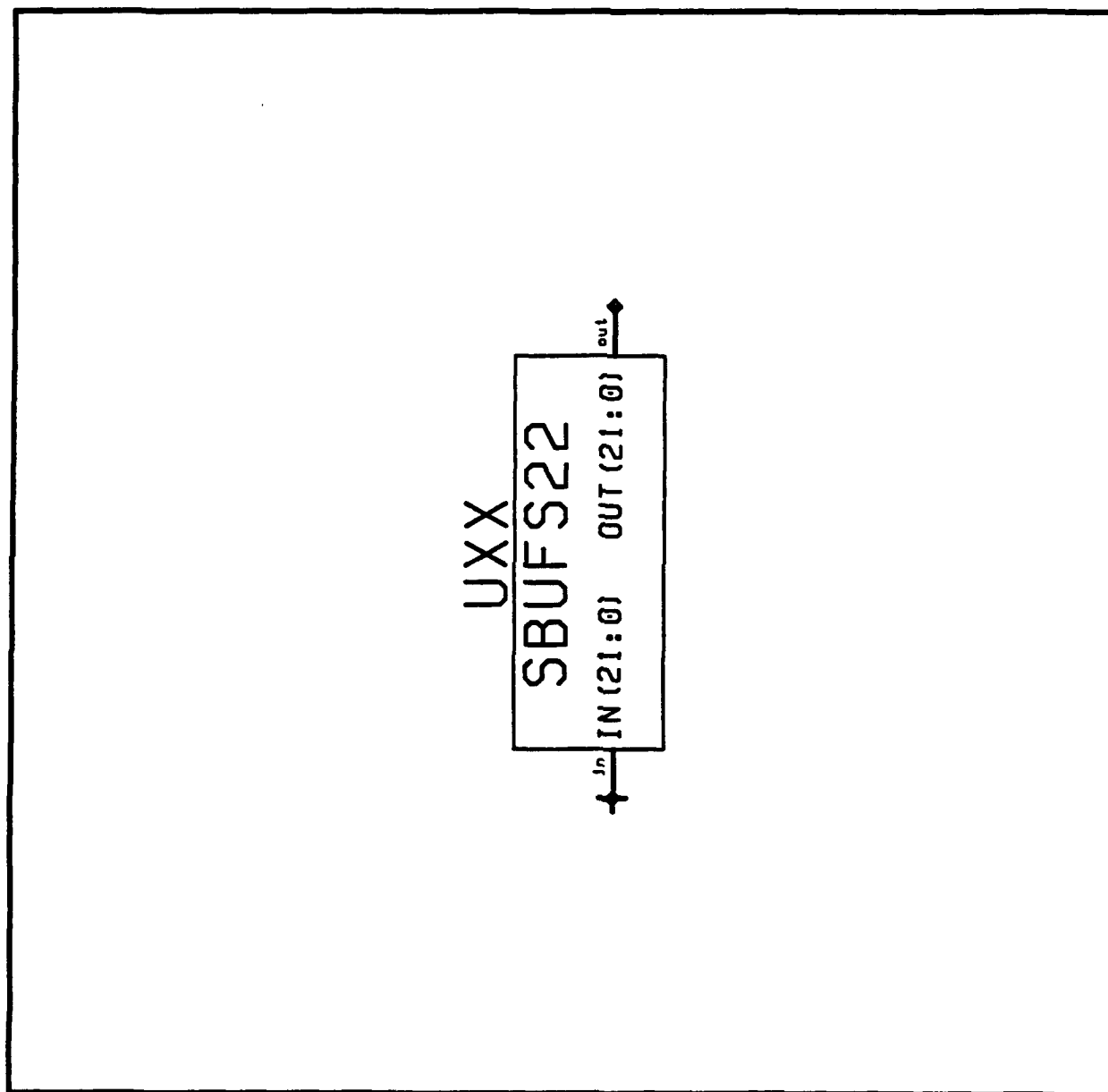


# RMUX

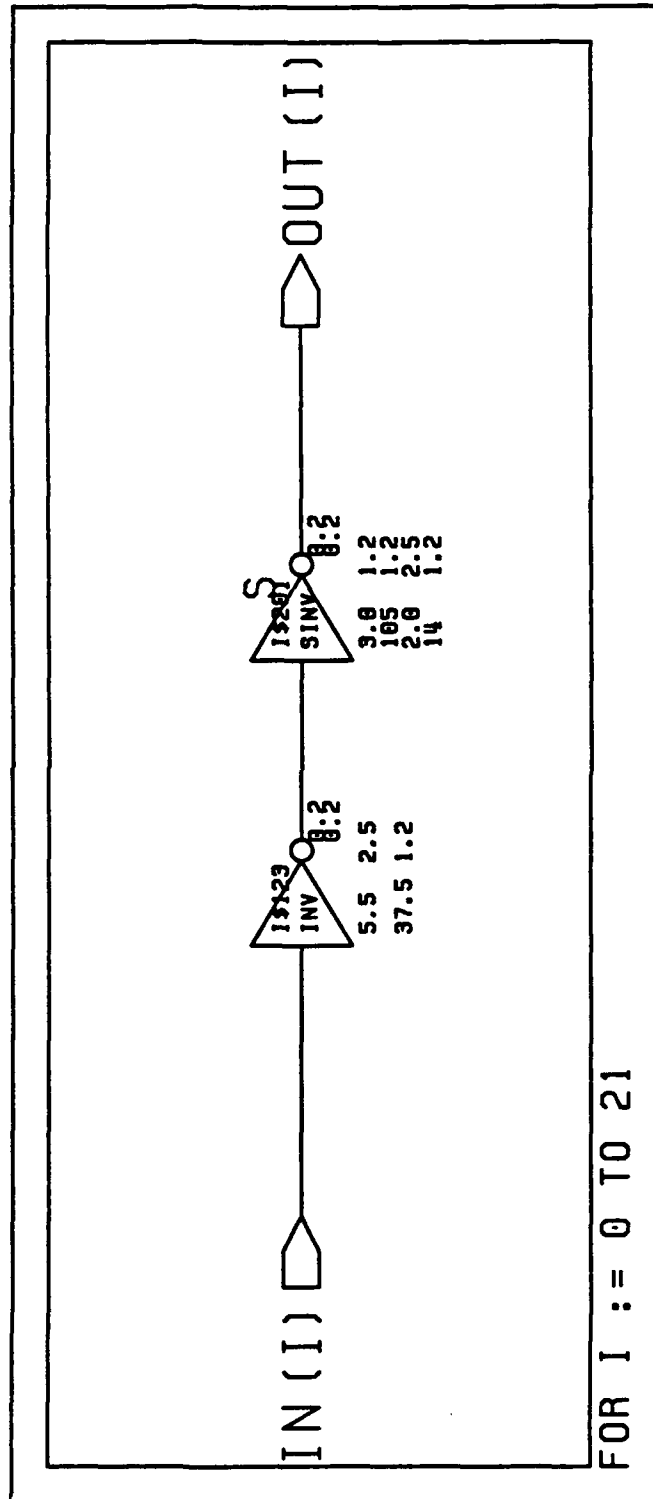


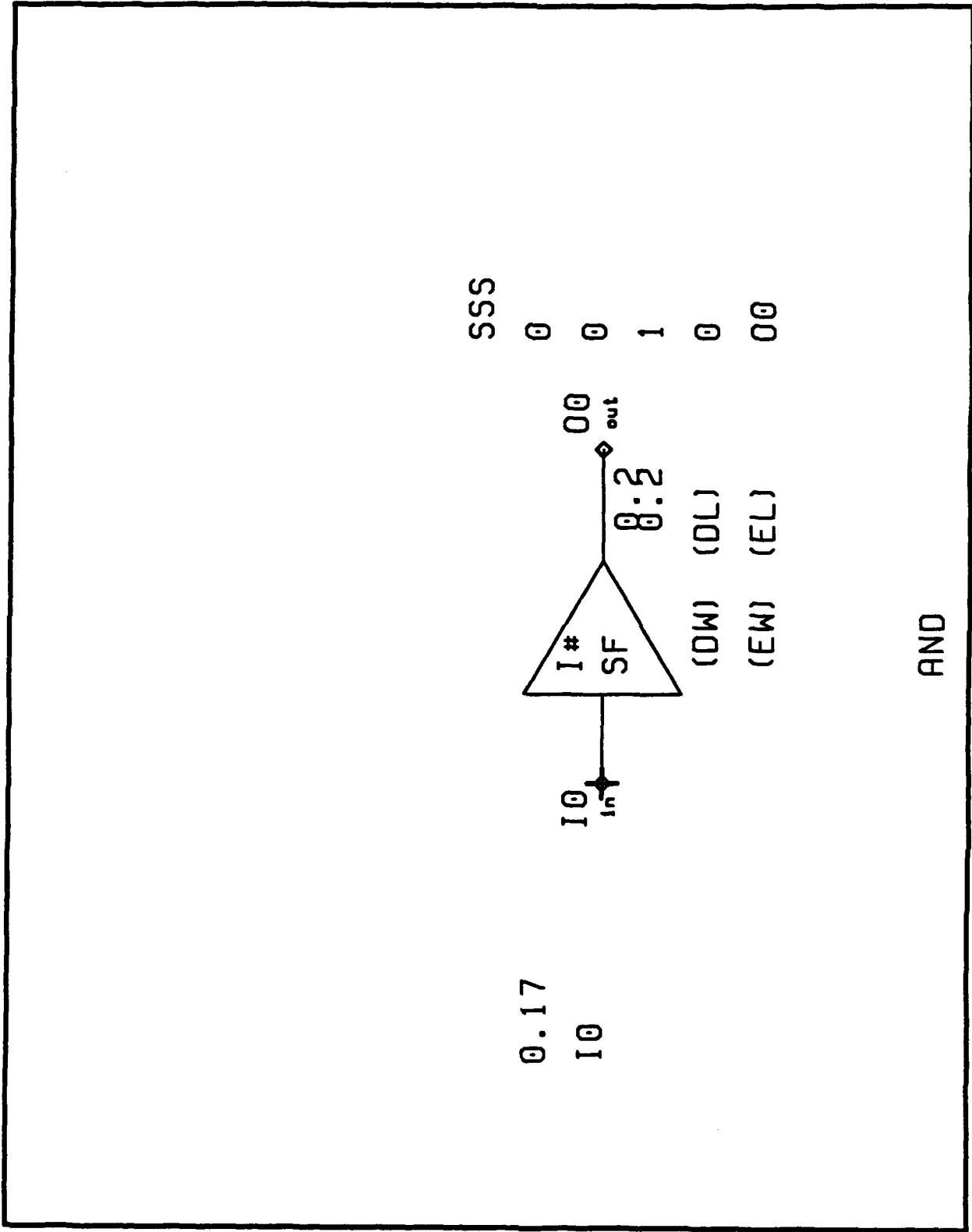


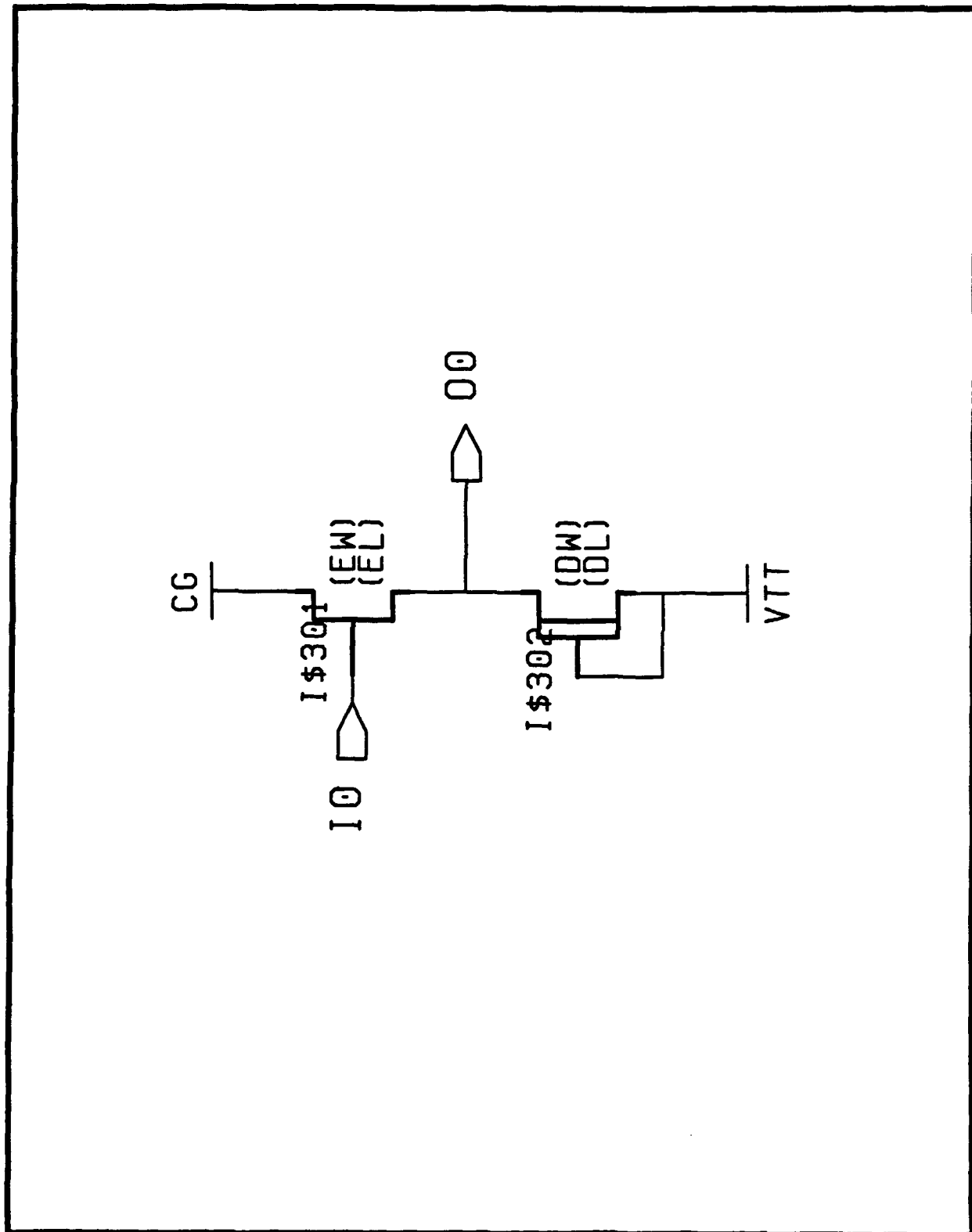




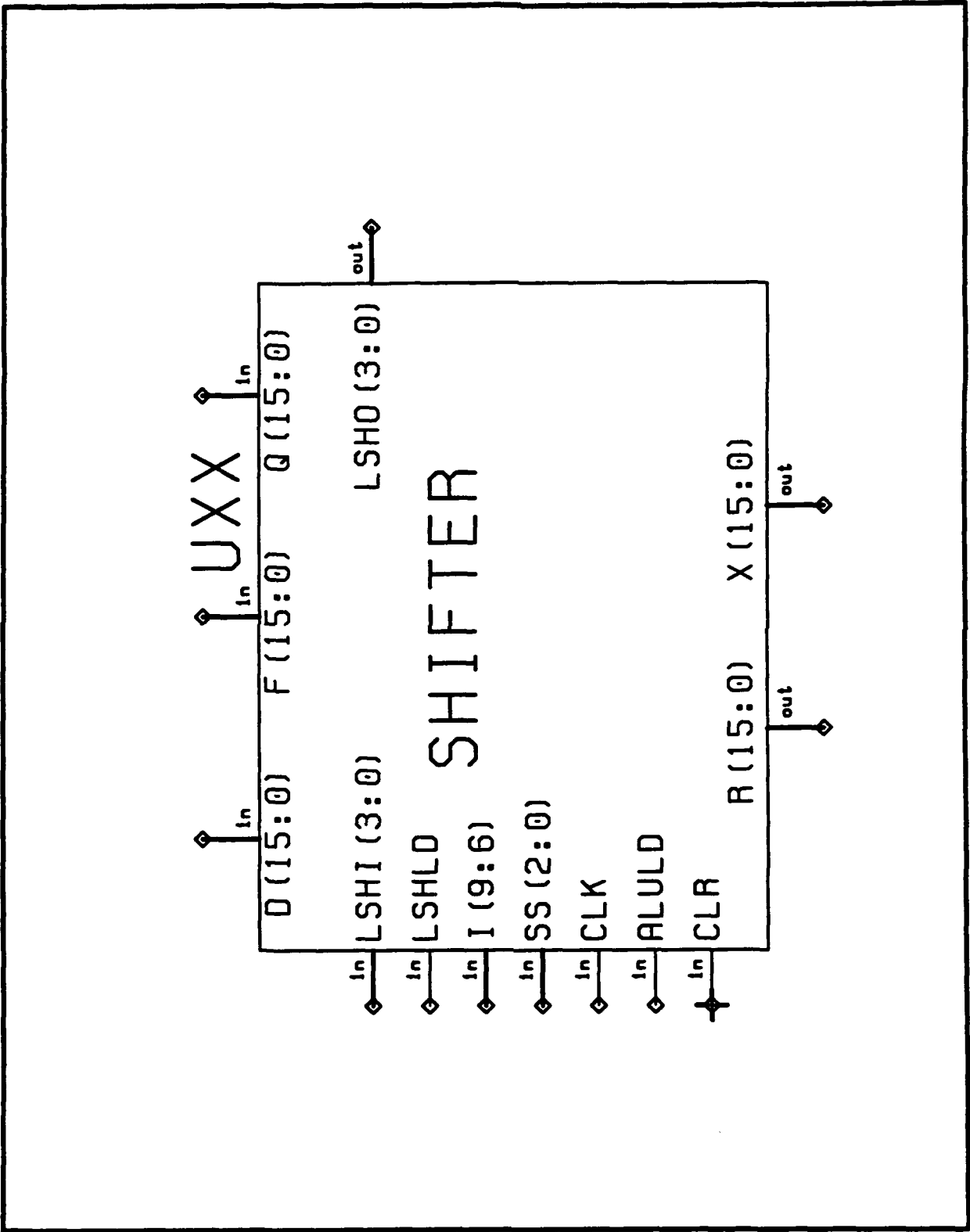
# SBUF22: 22-BIT SMALL SUPERBUFFER

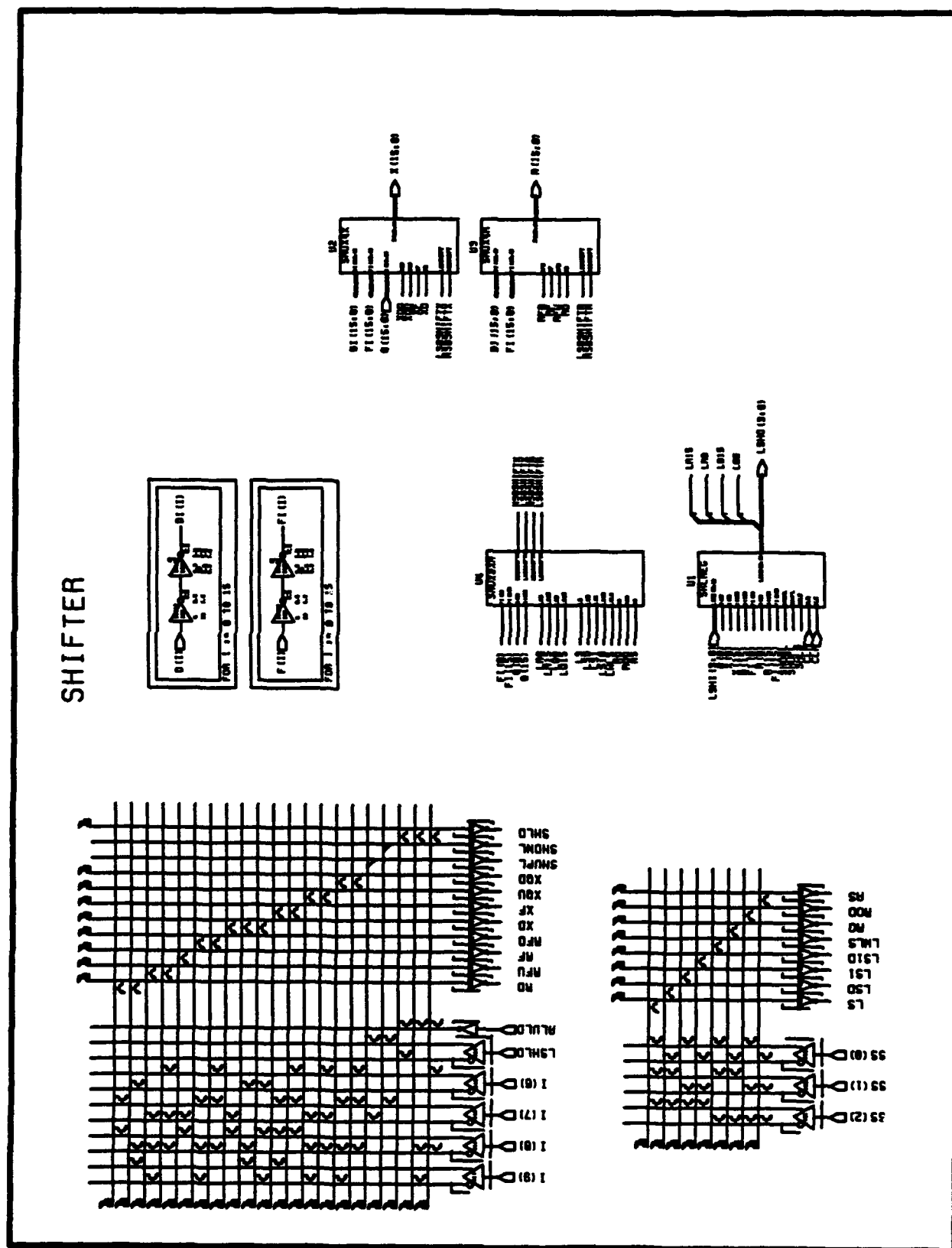


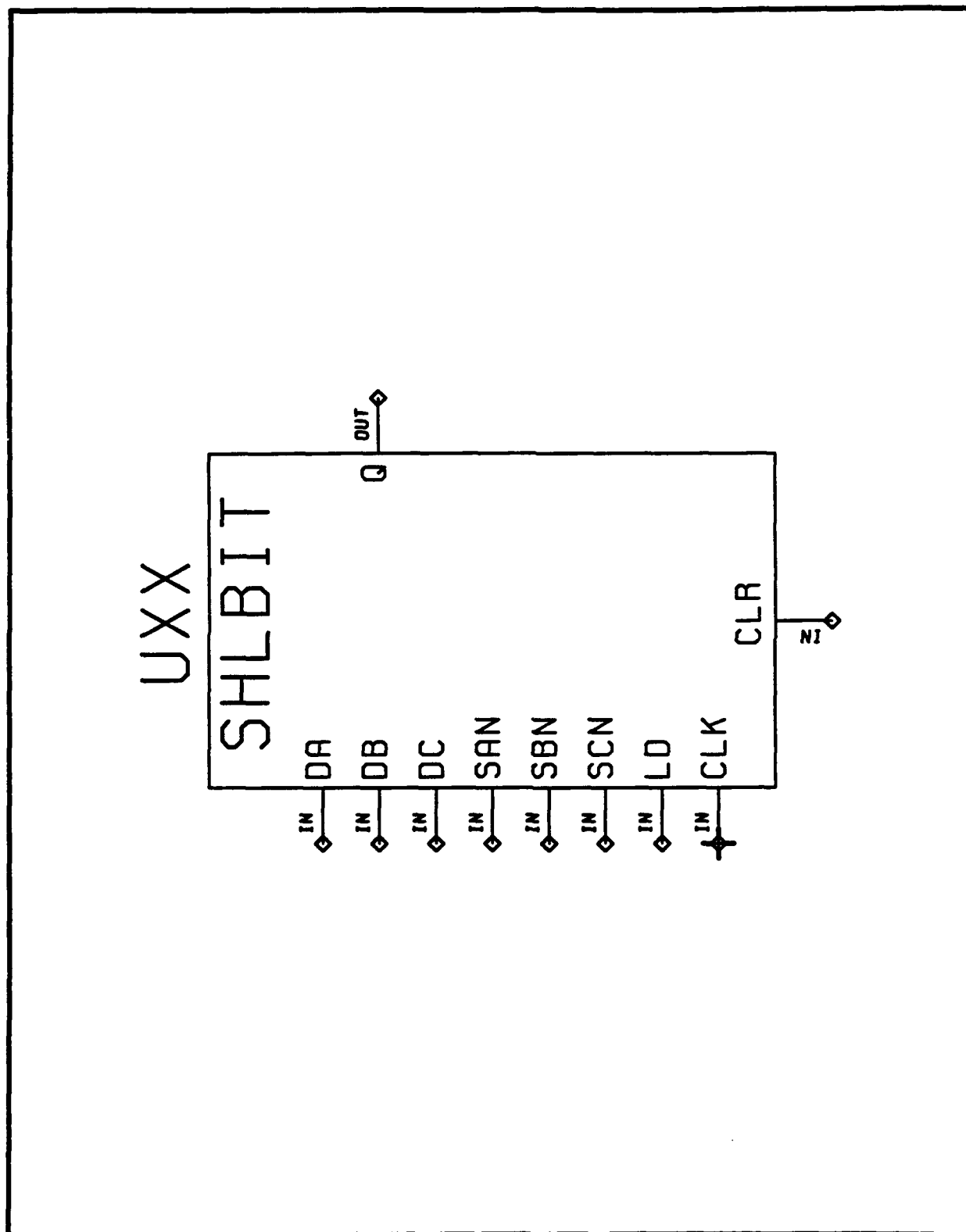


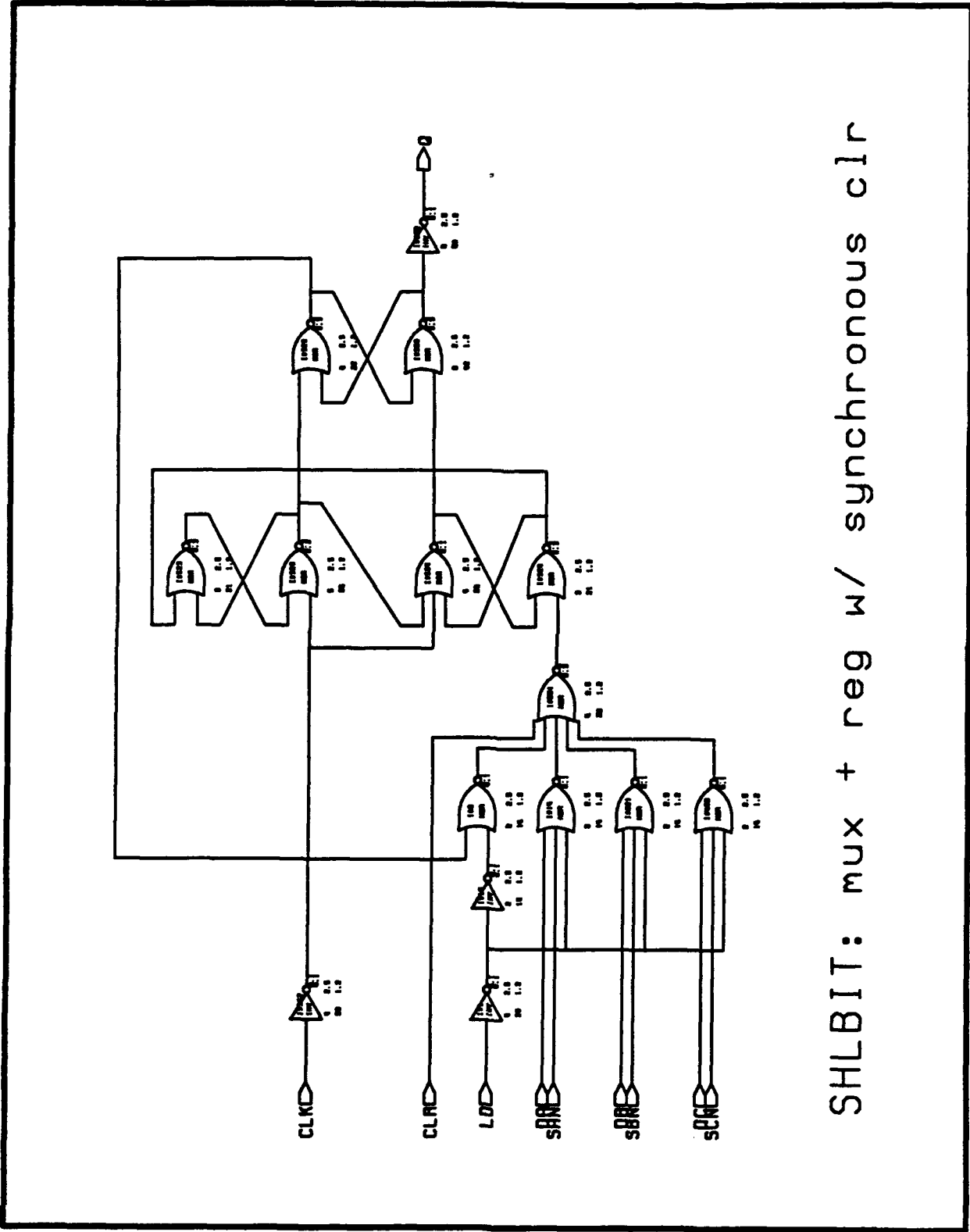


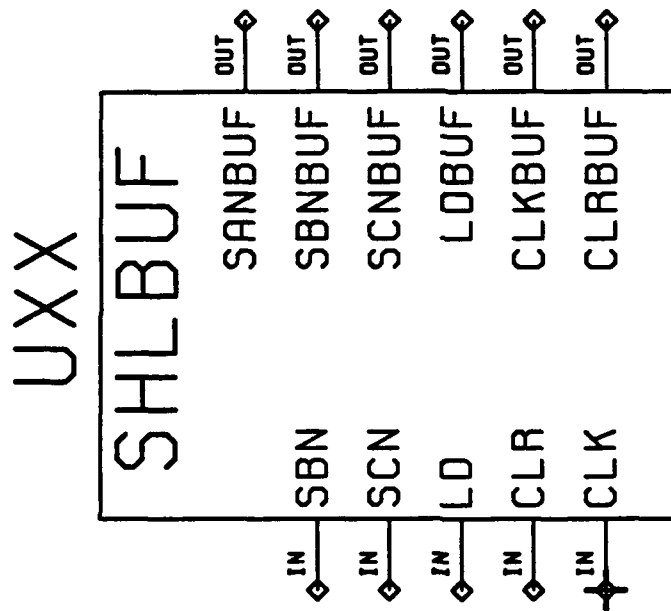


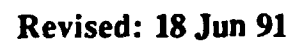


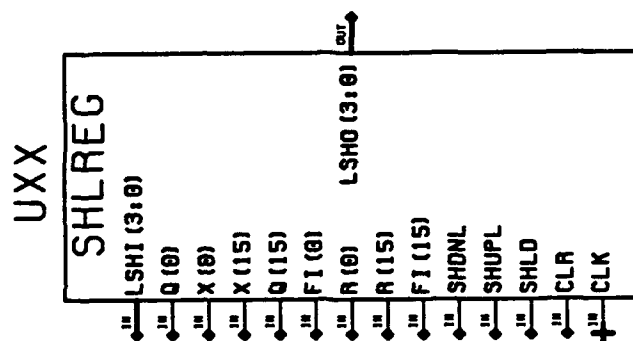


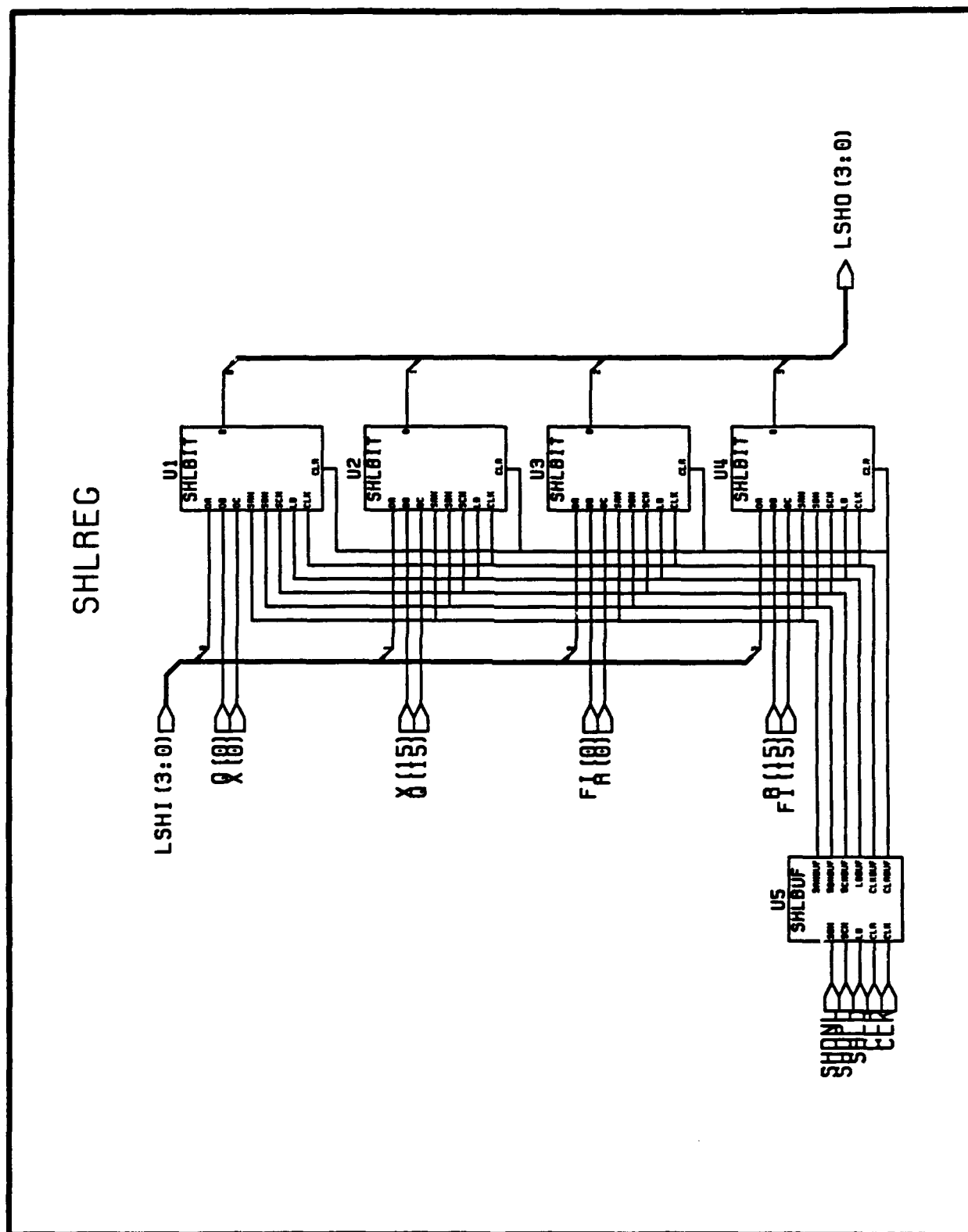




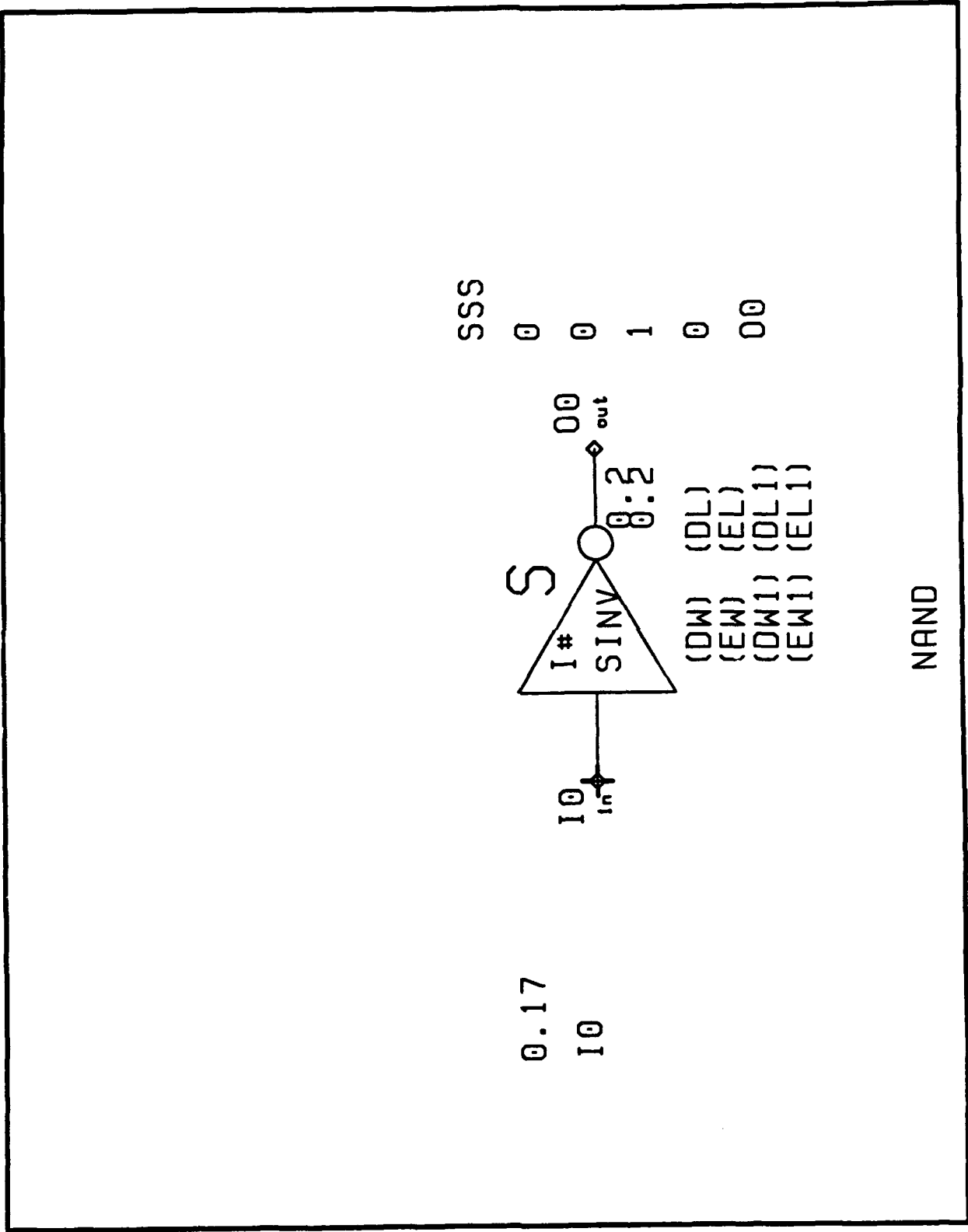


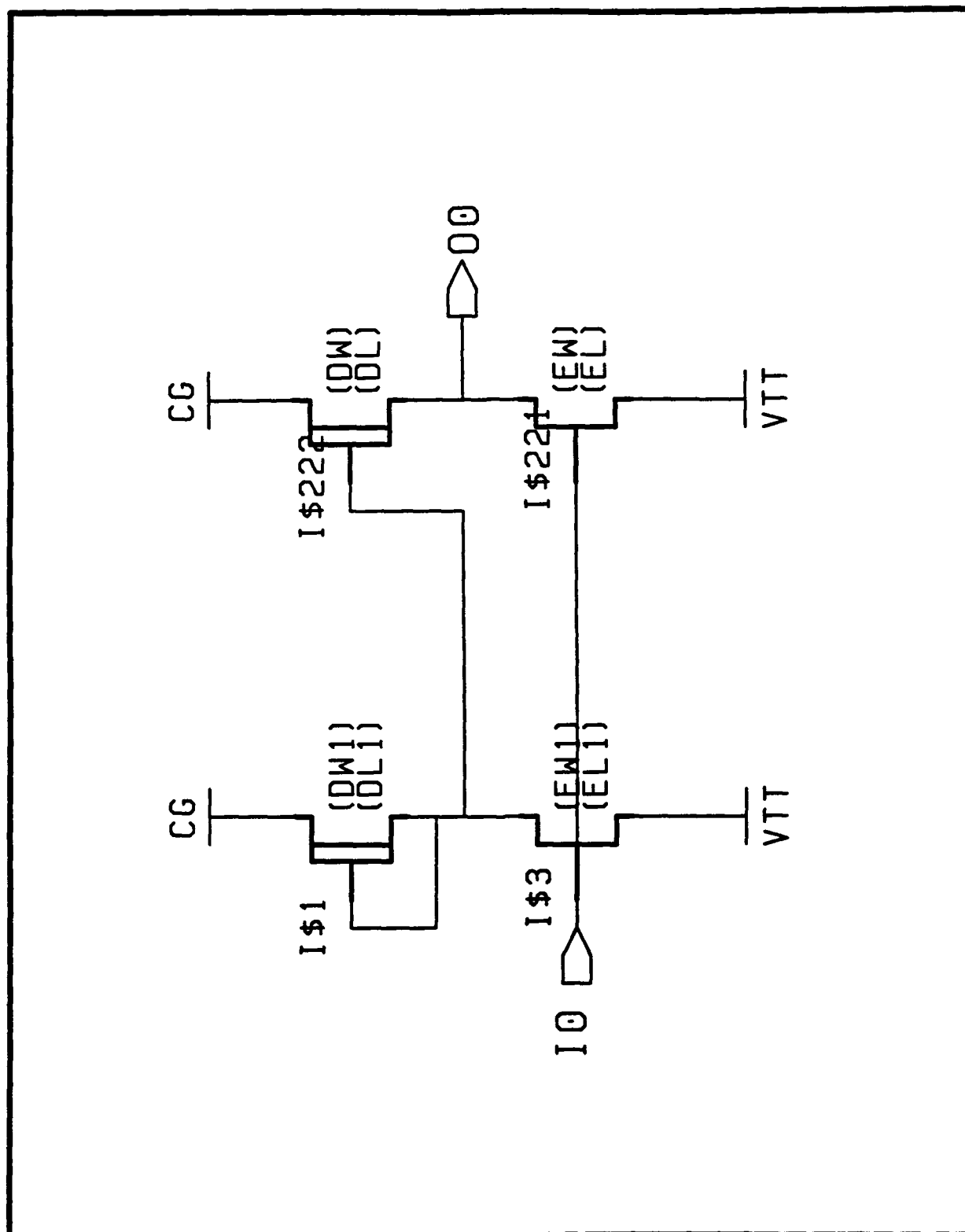


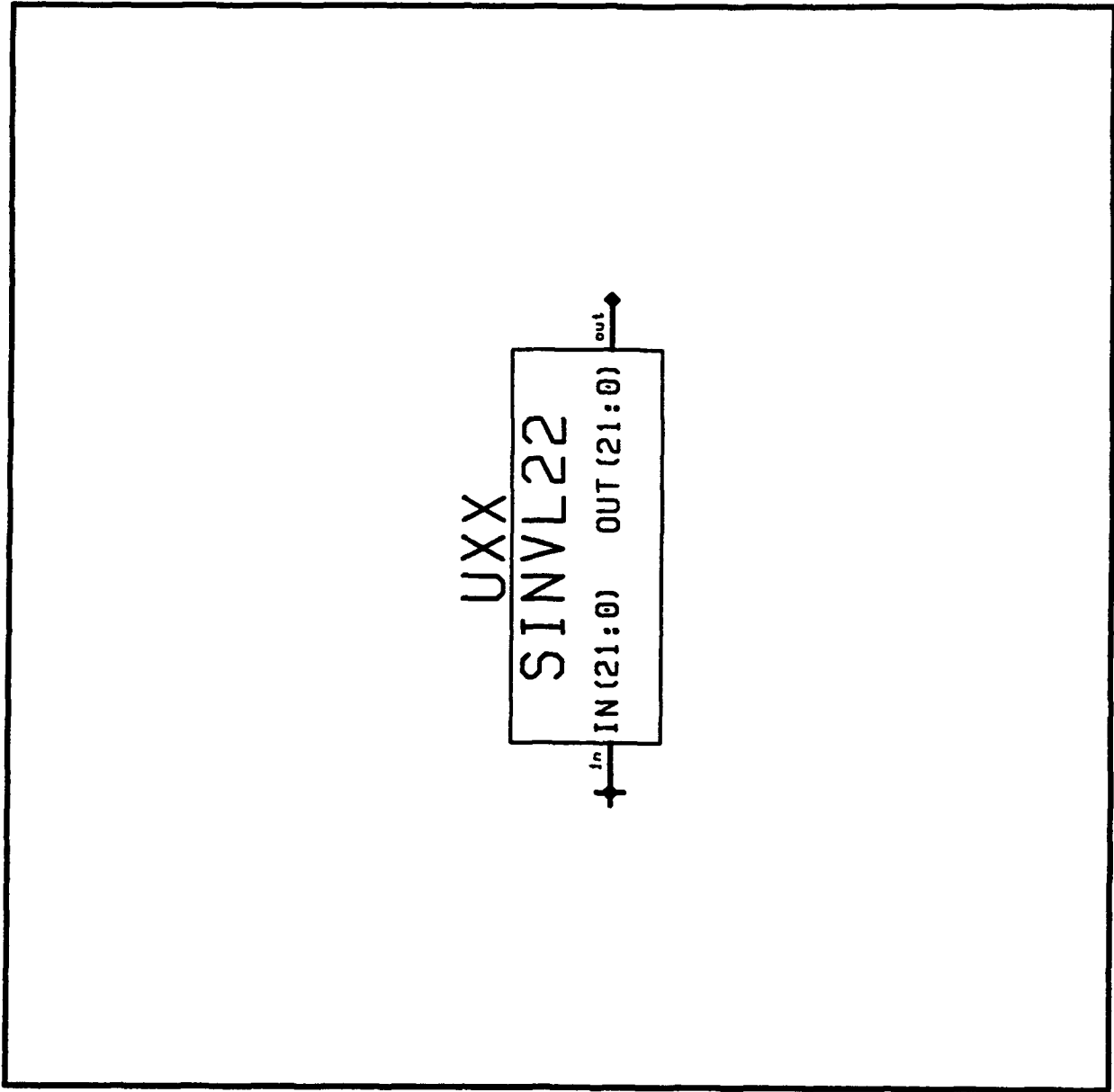


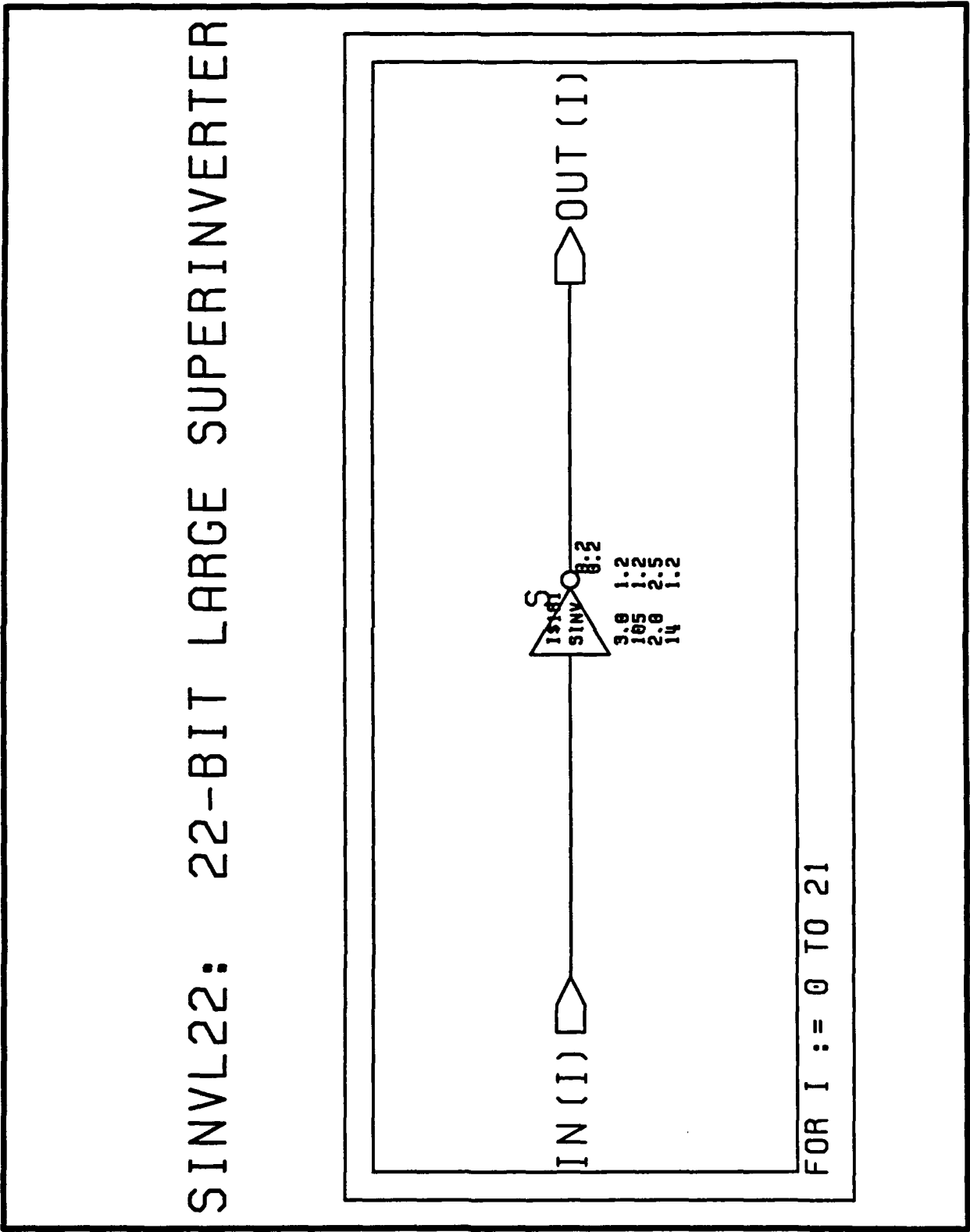


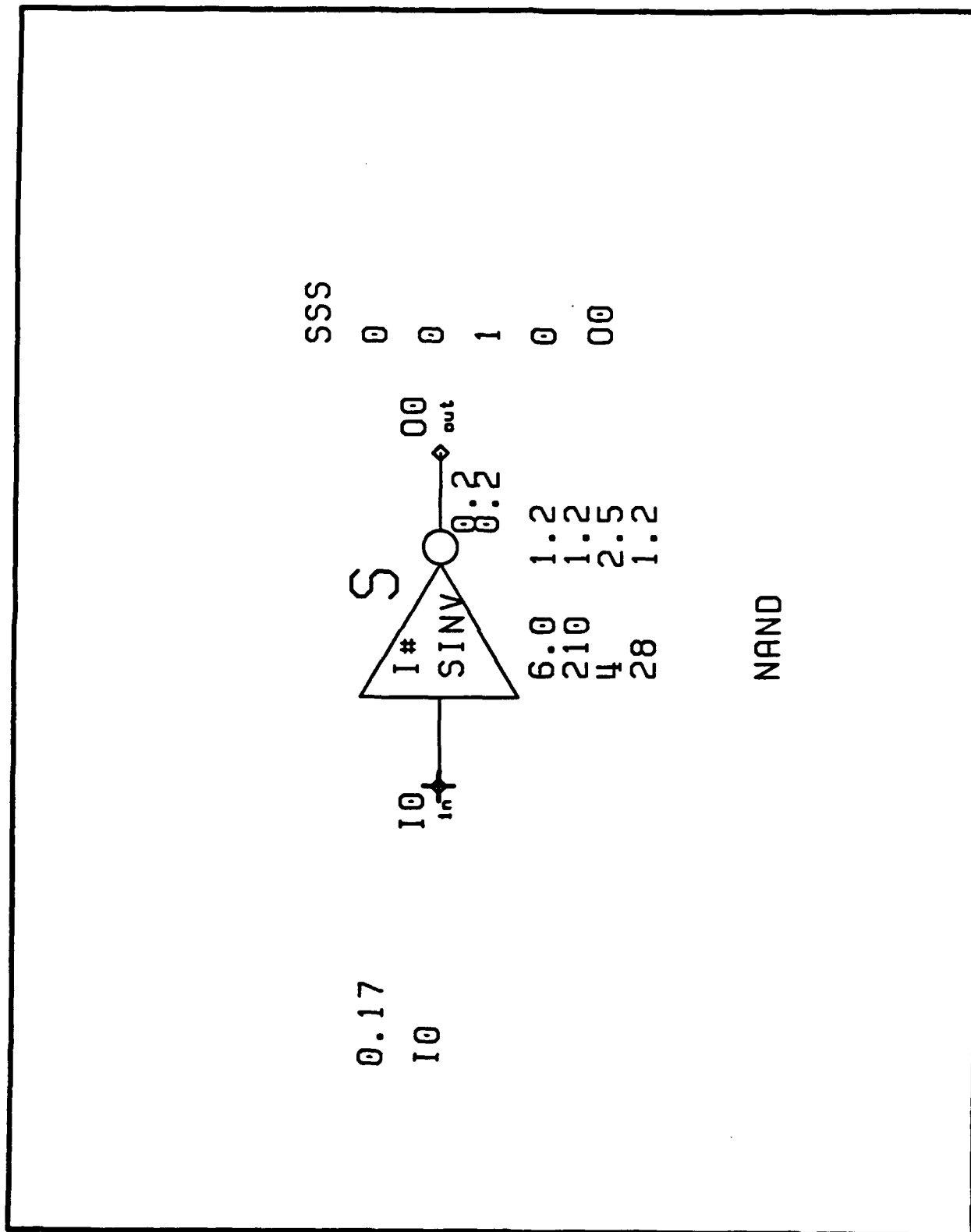


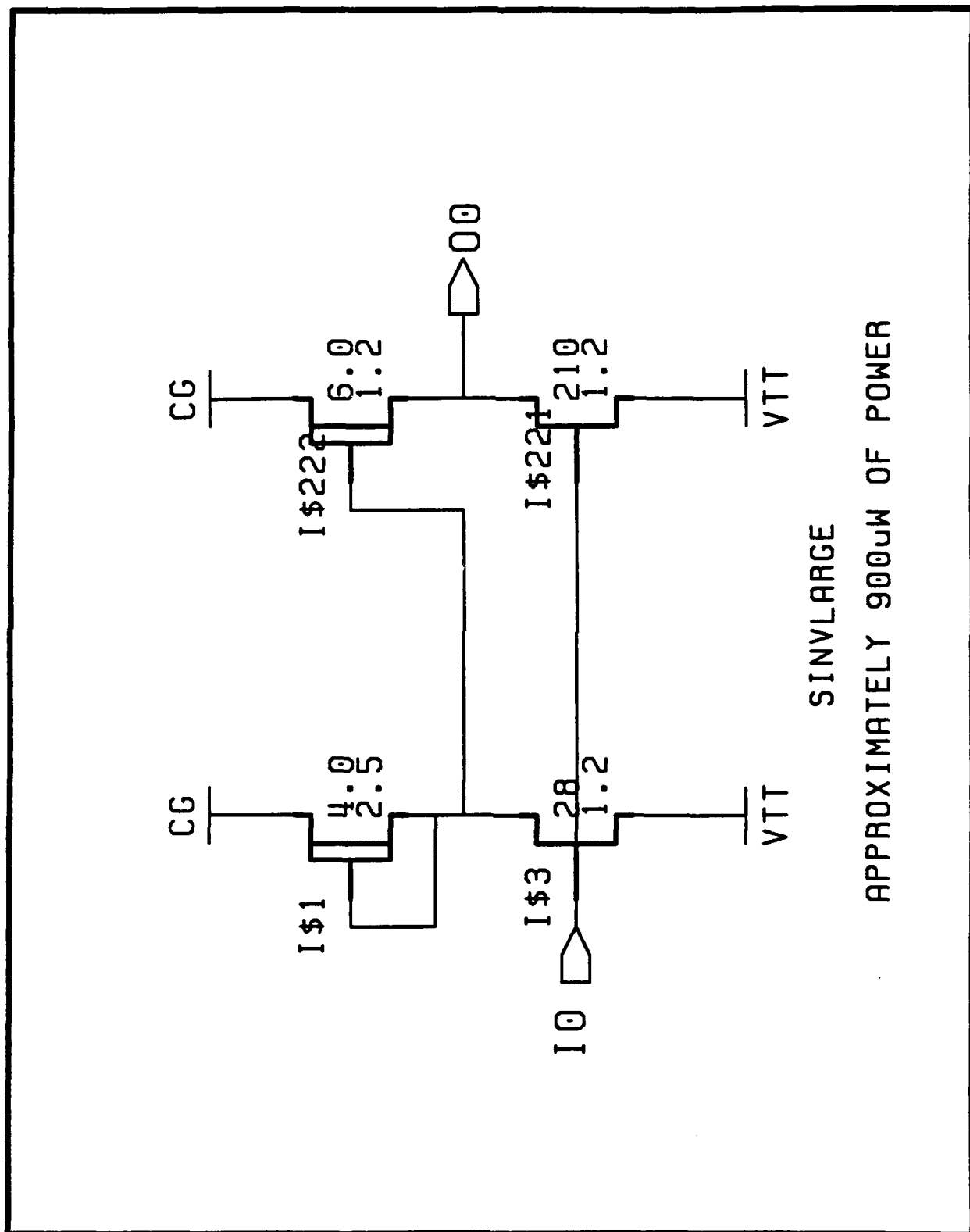


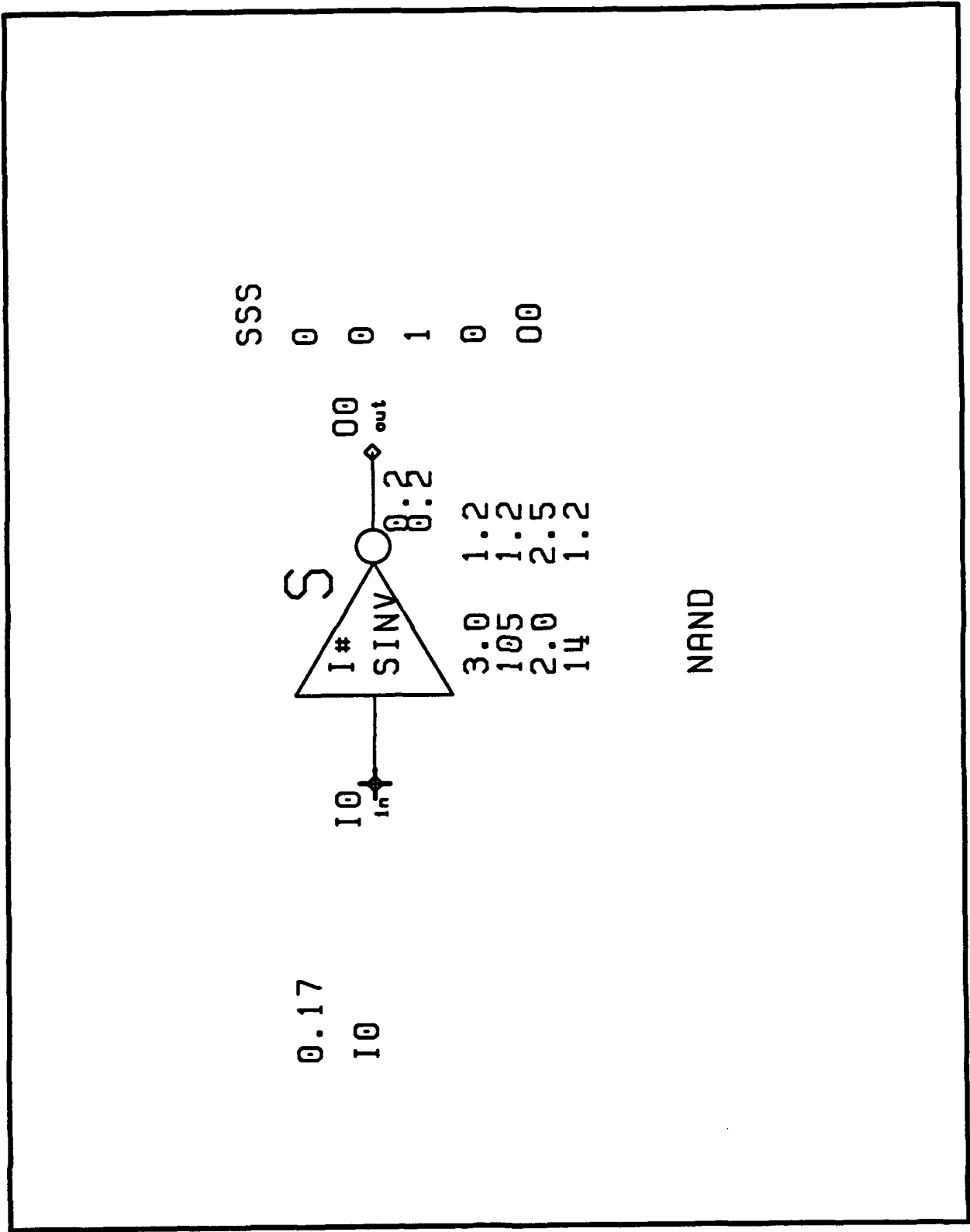


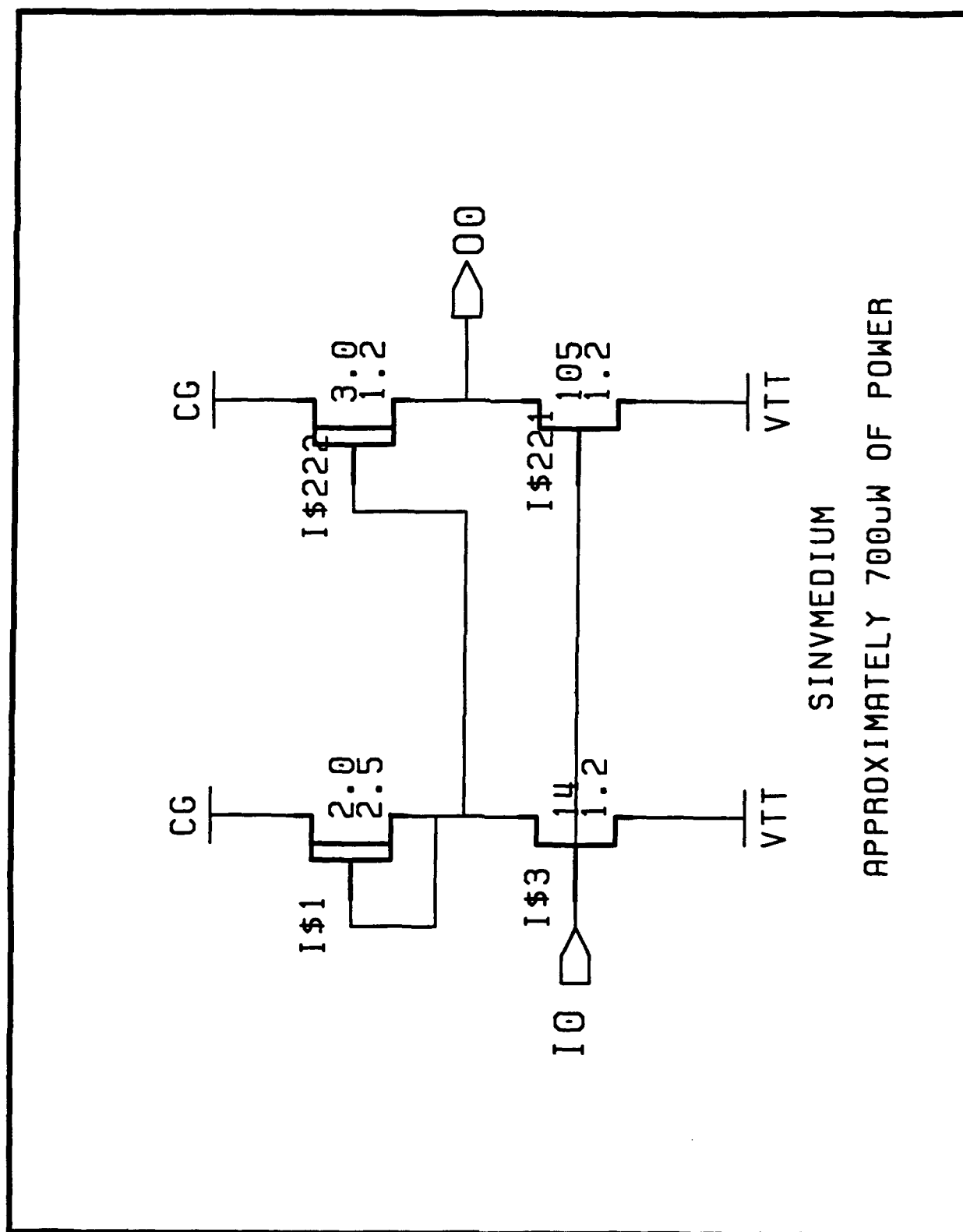




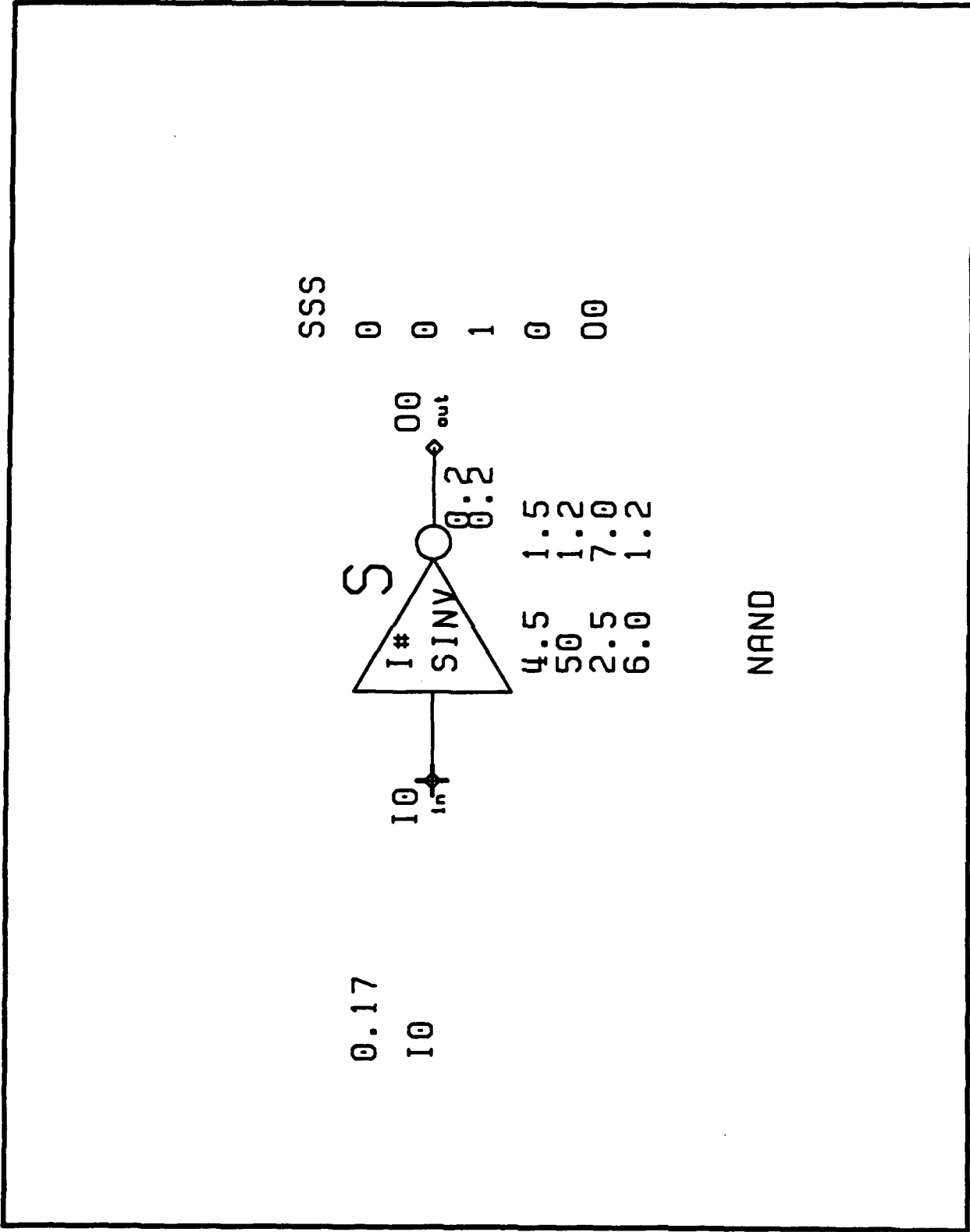


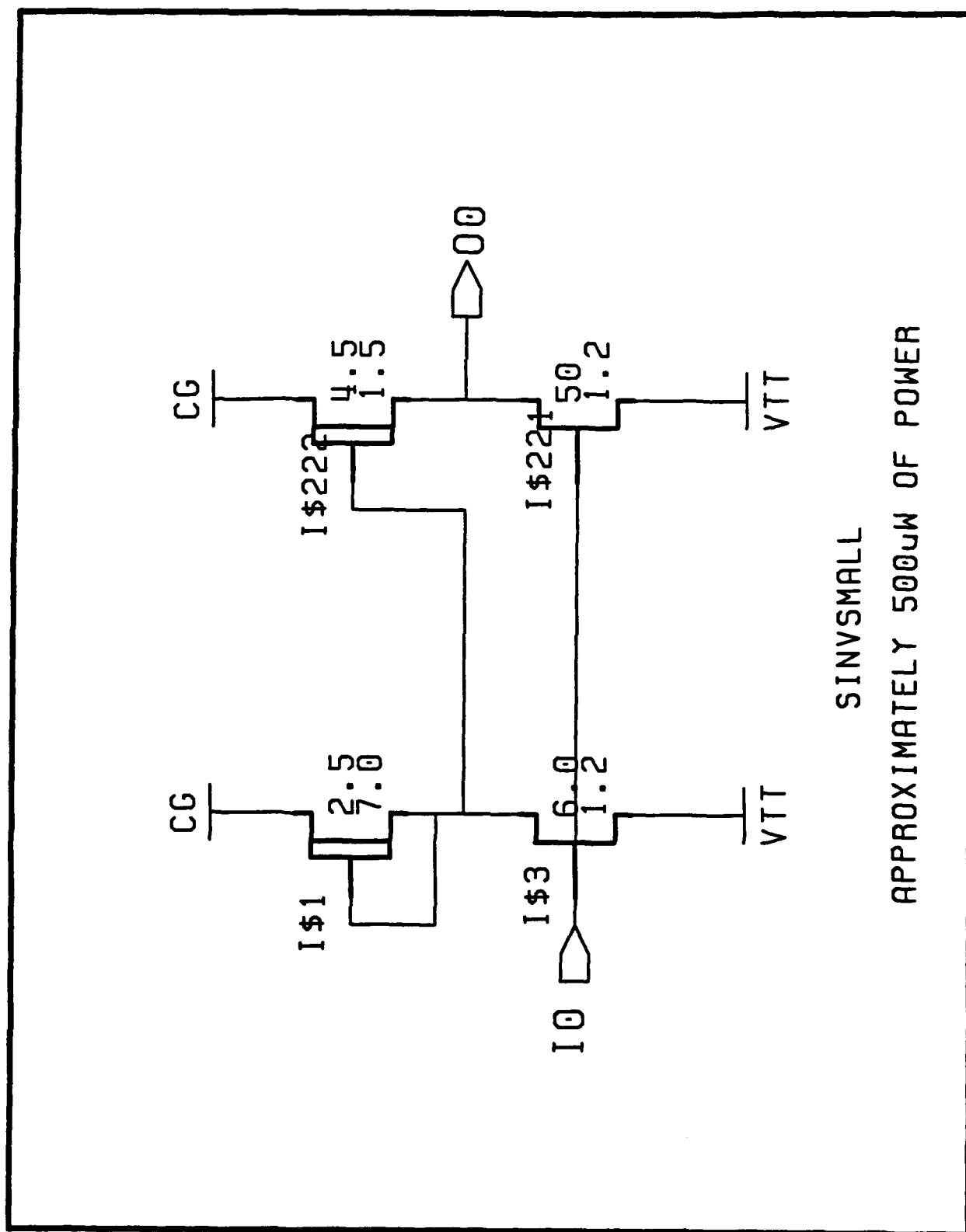


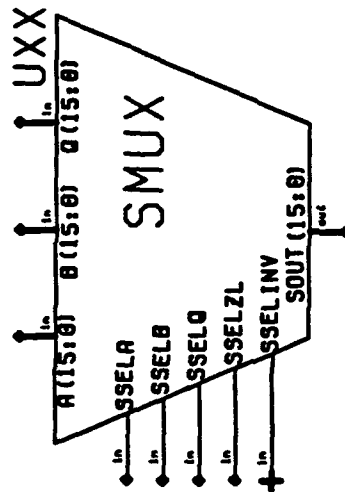


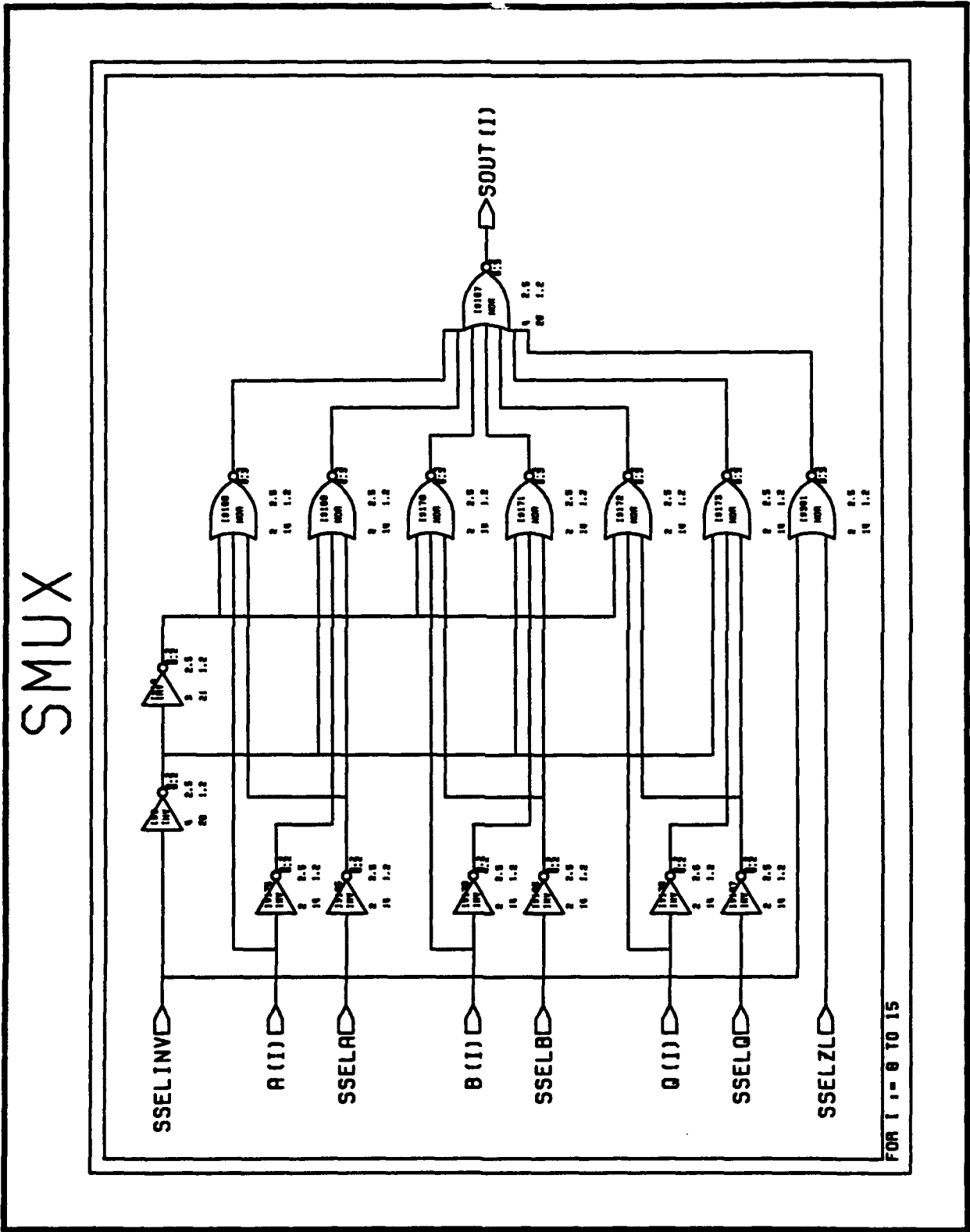


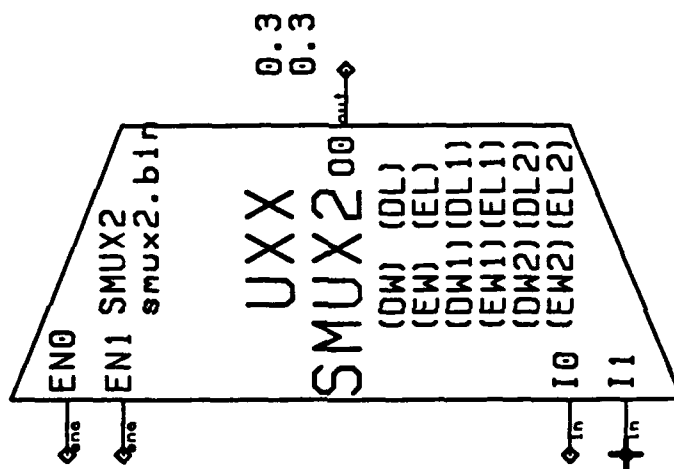


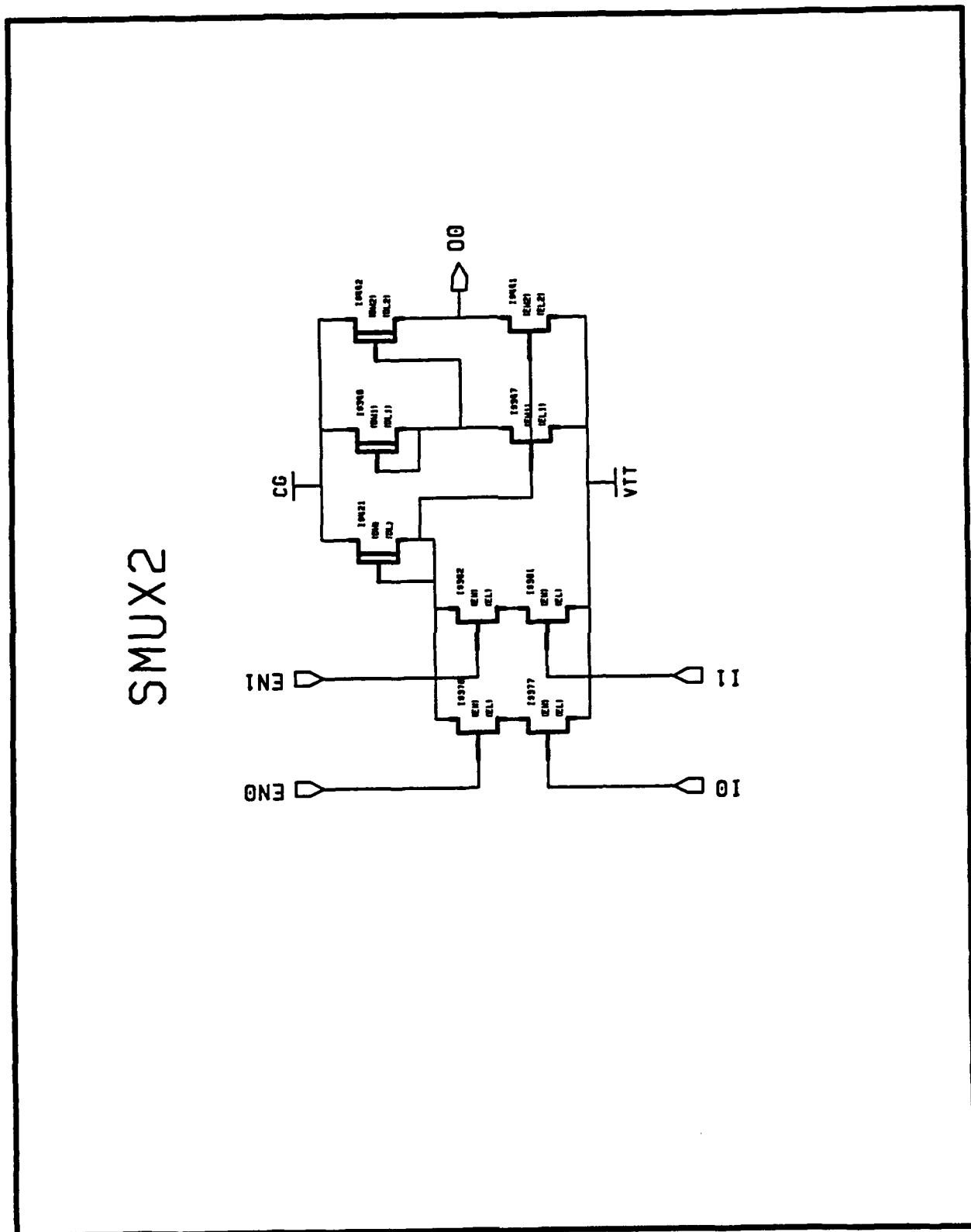


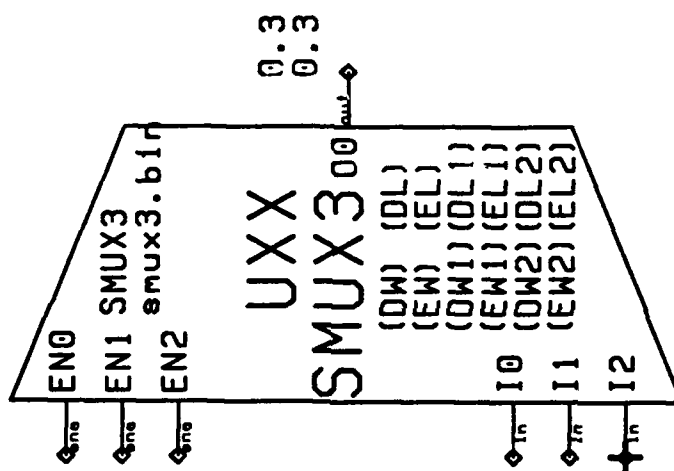


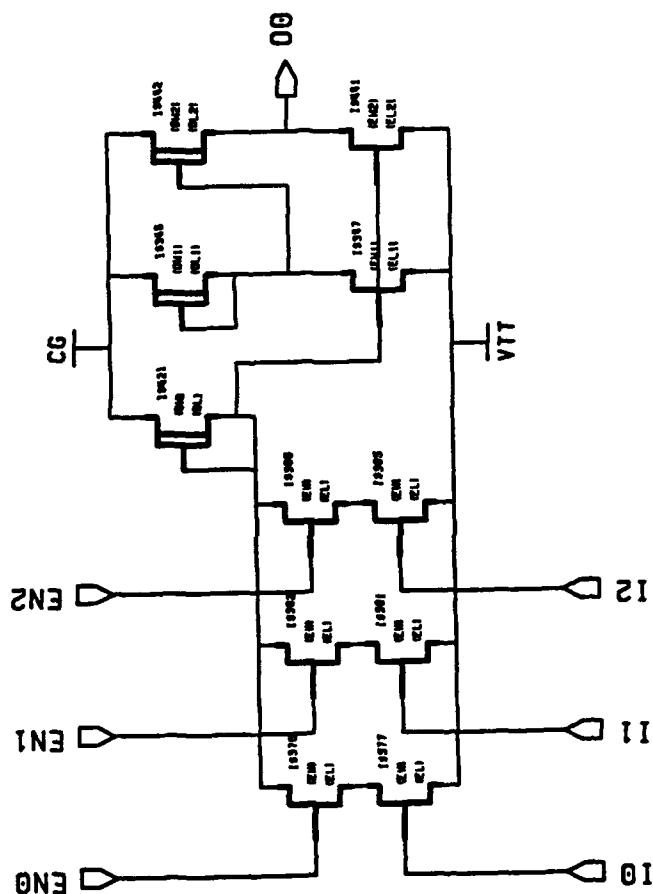




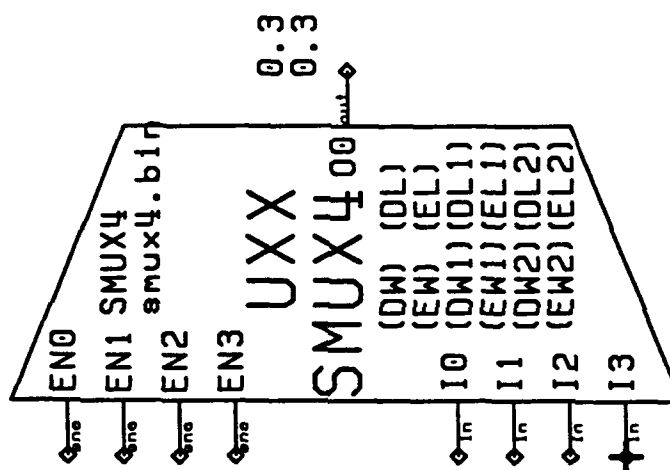


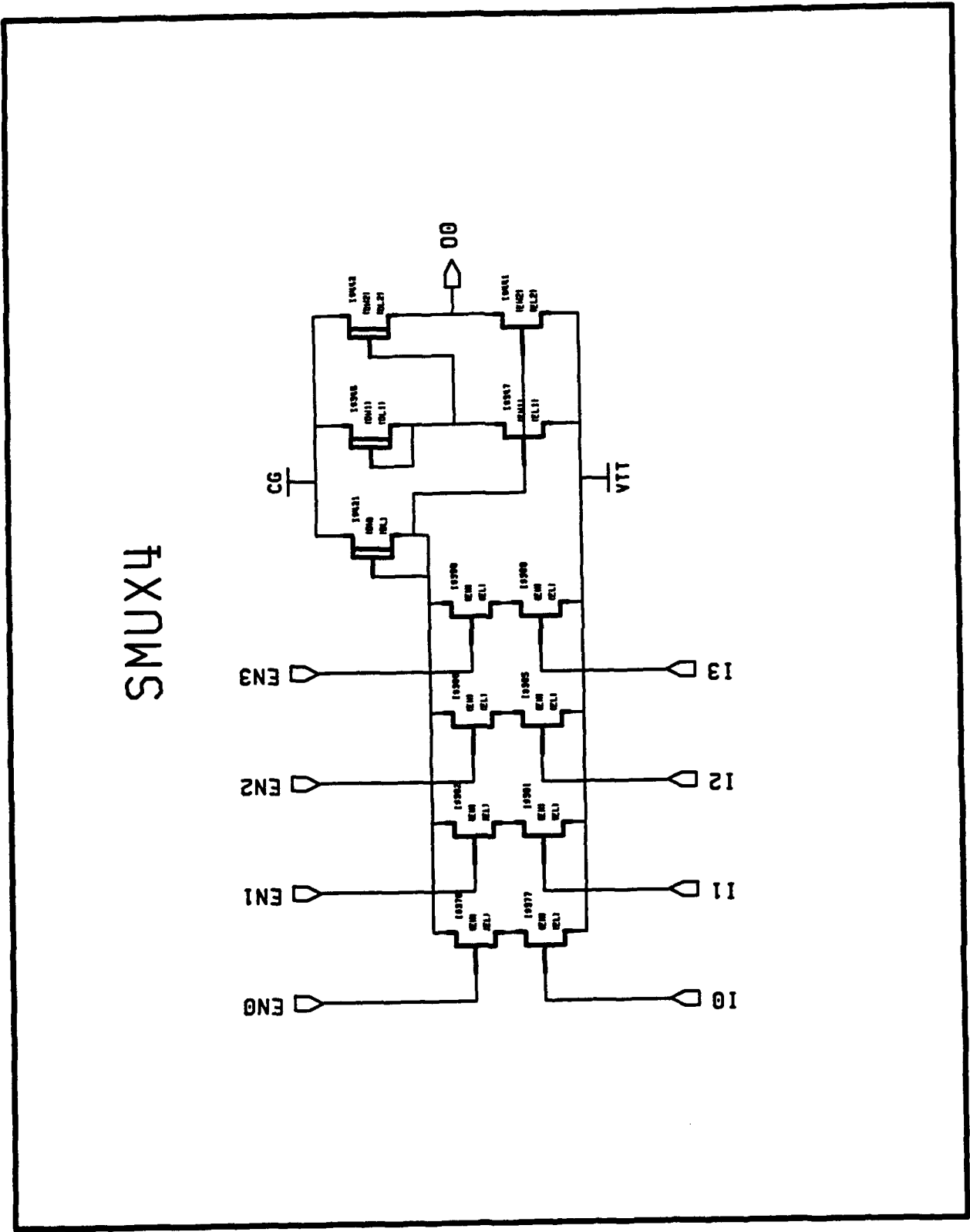


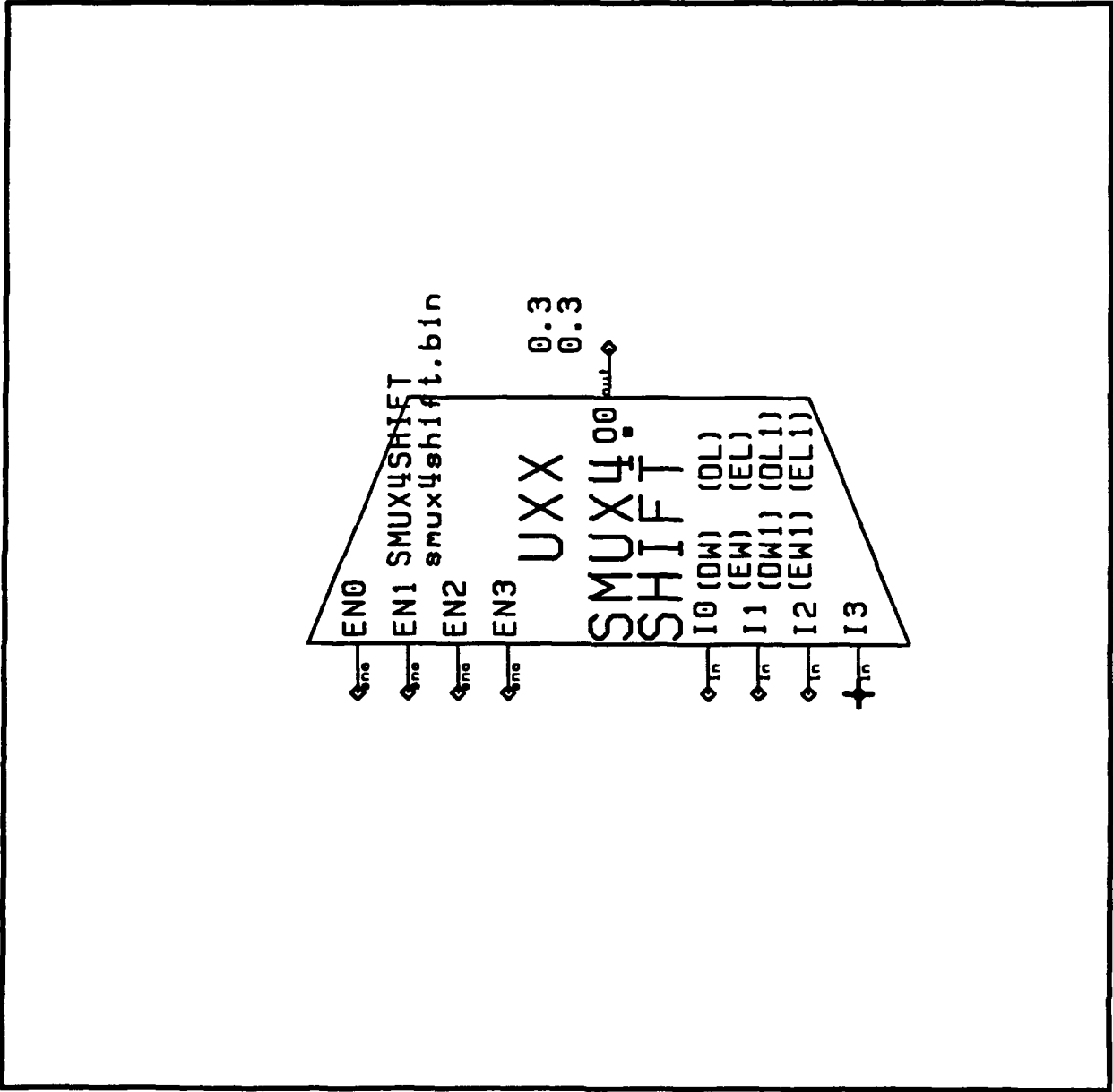


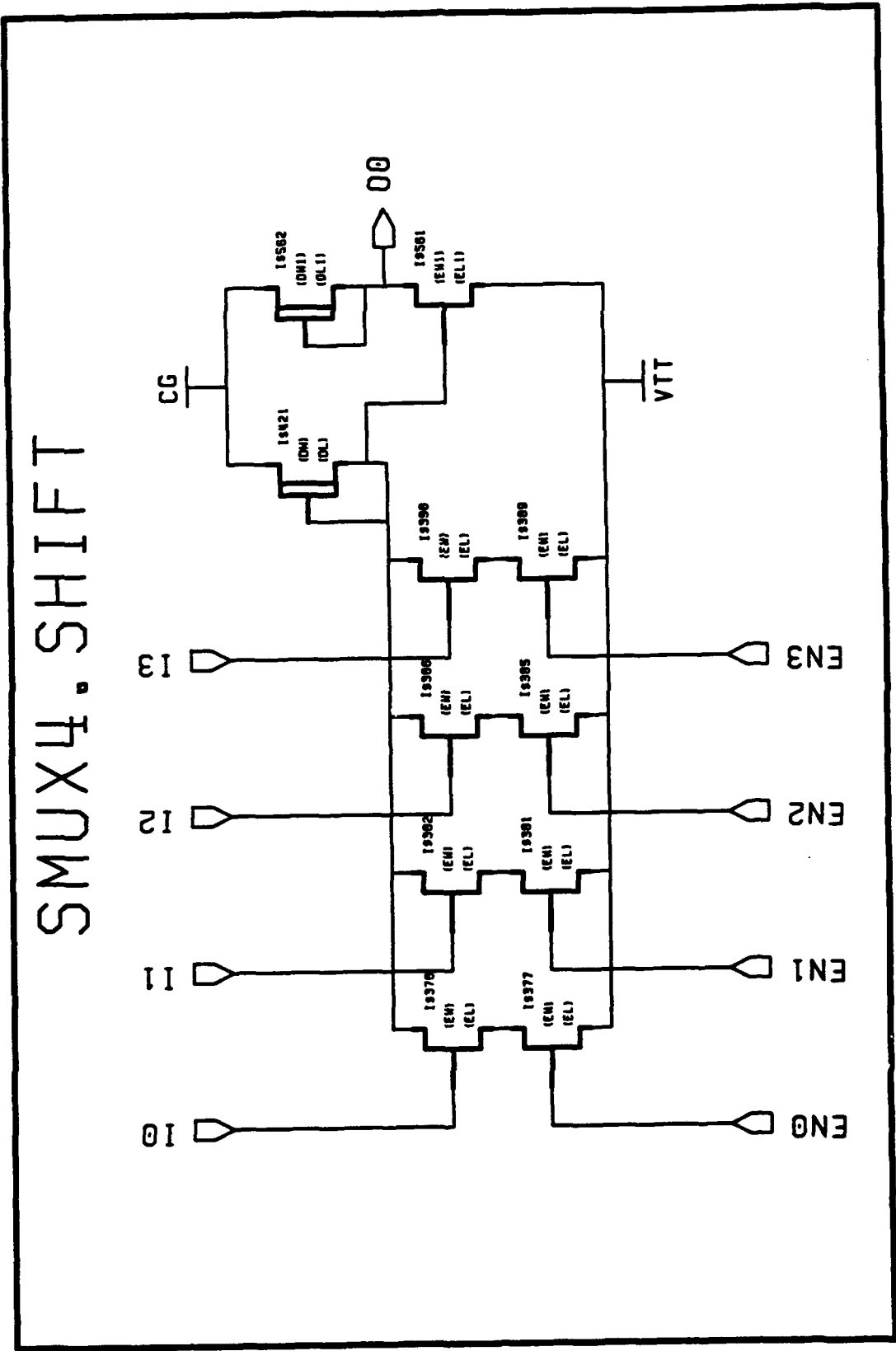


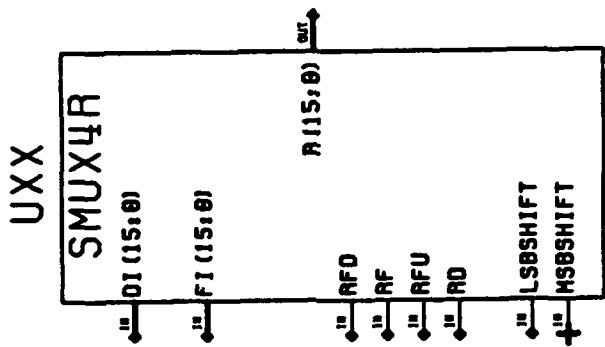


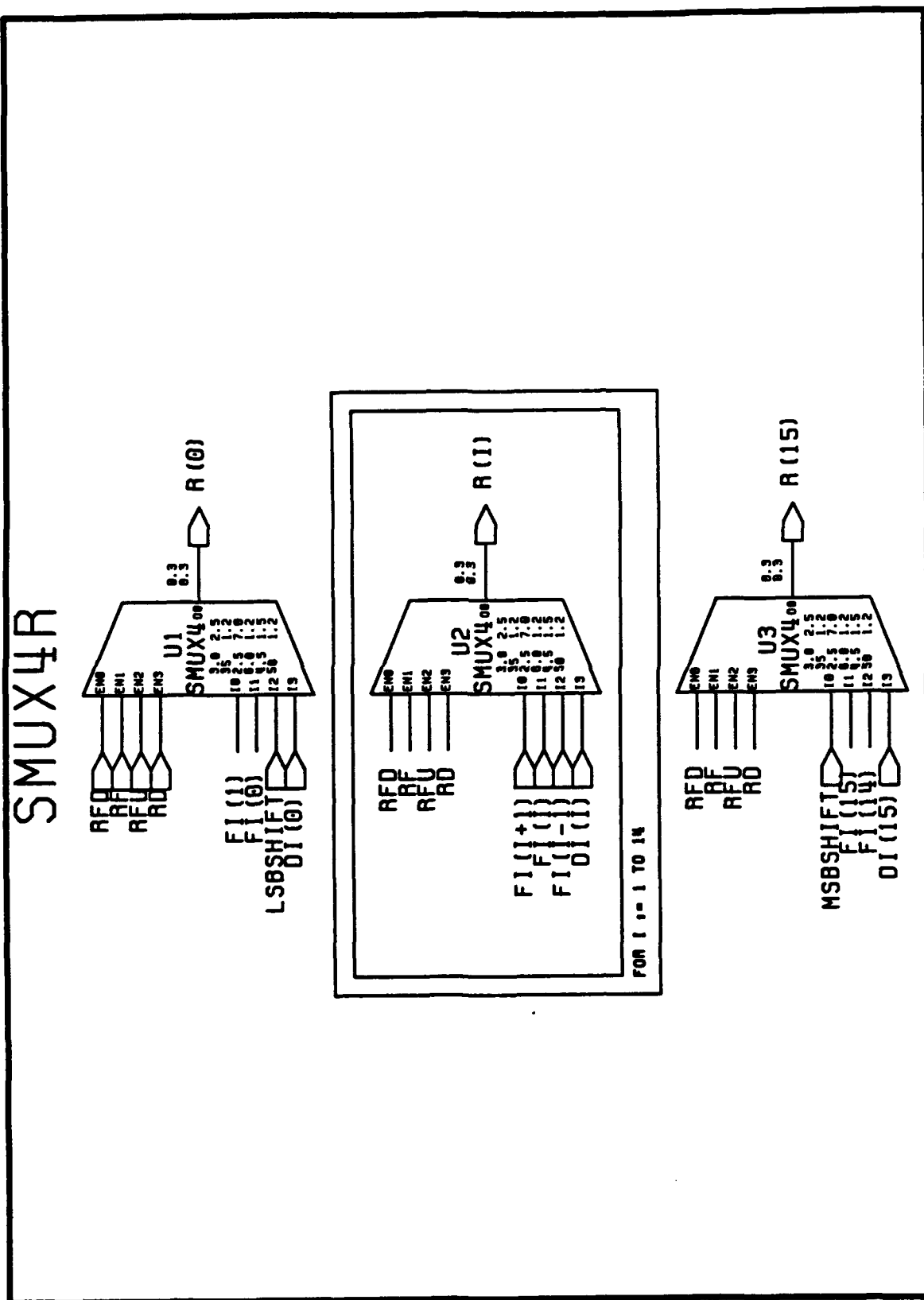


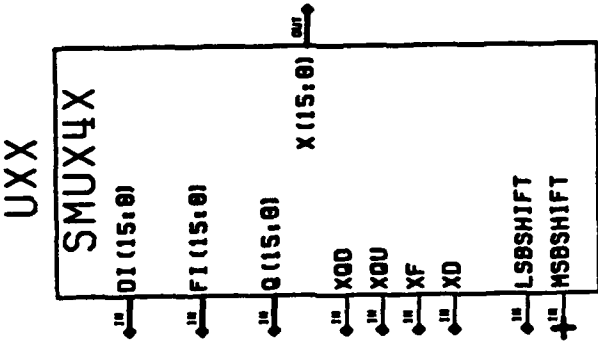


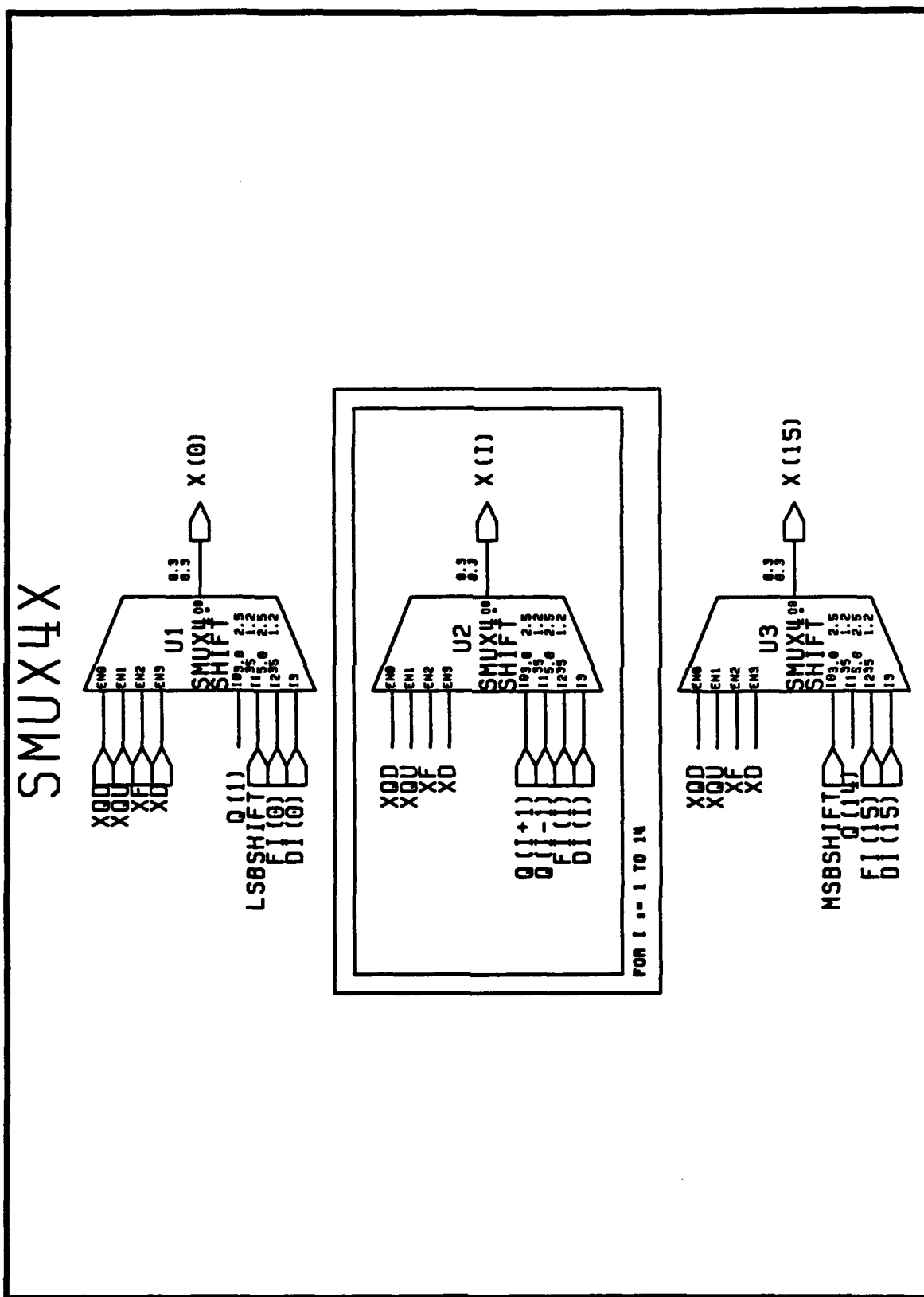




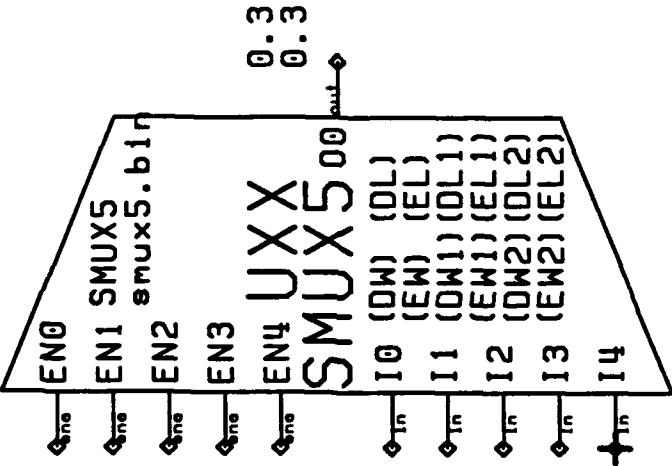


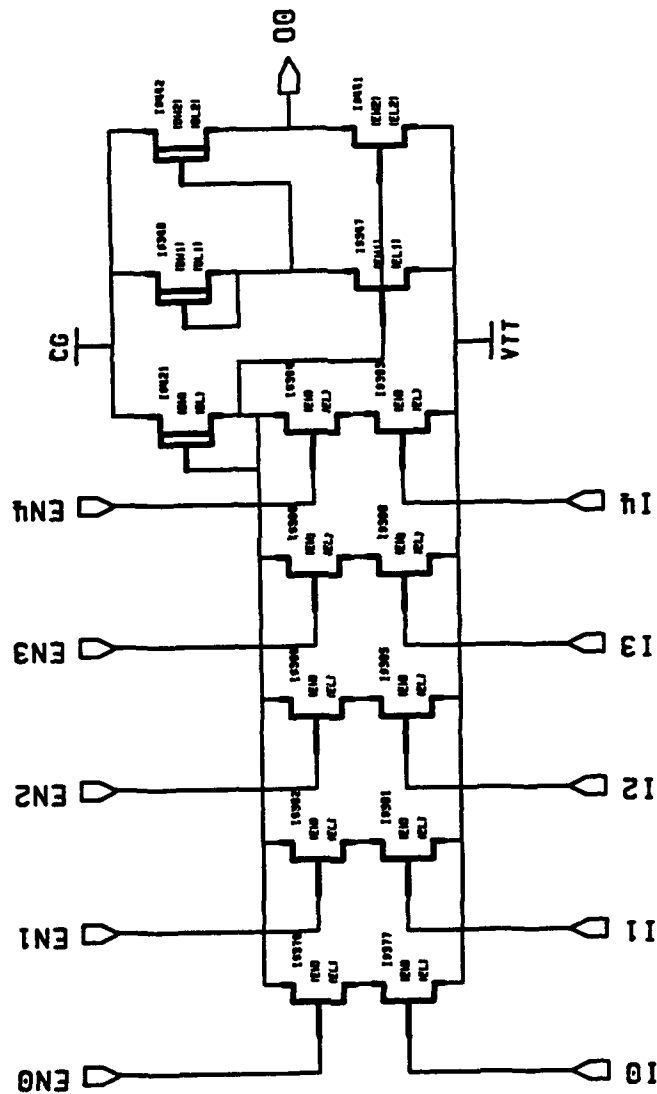


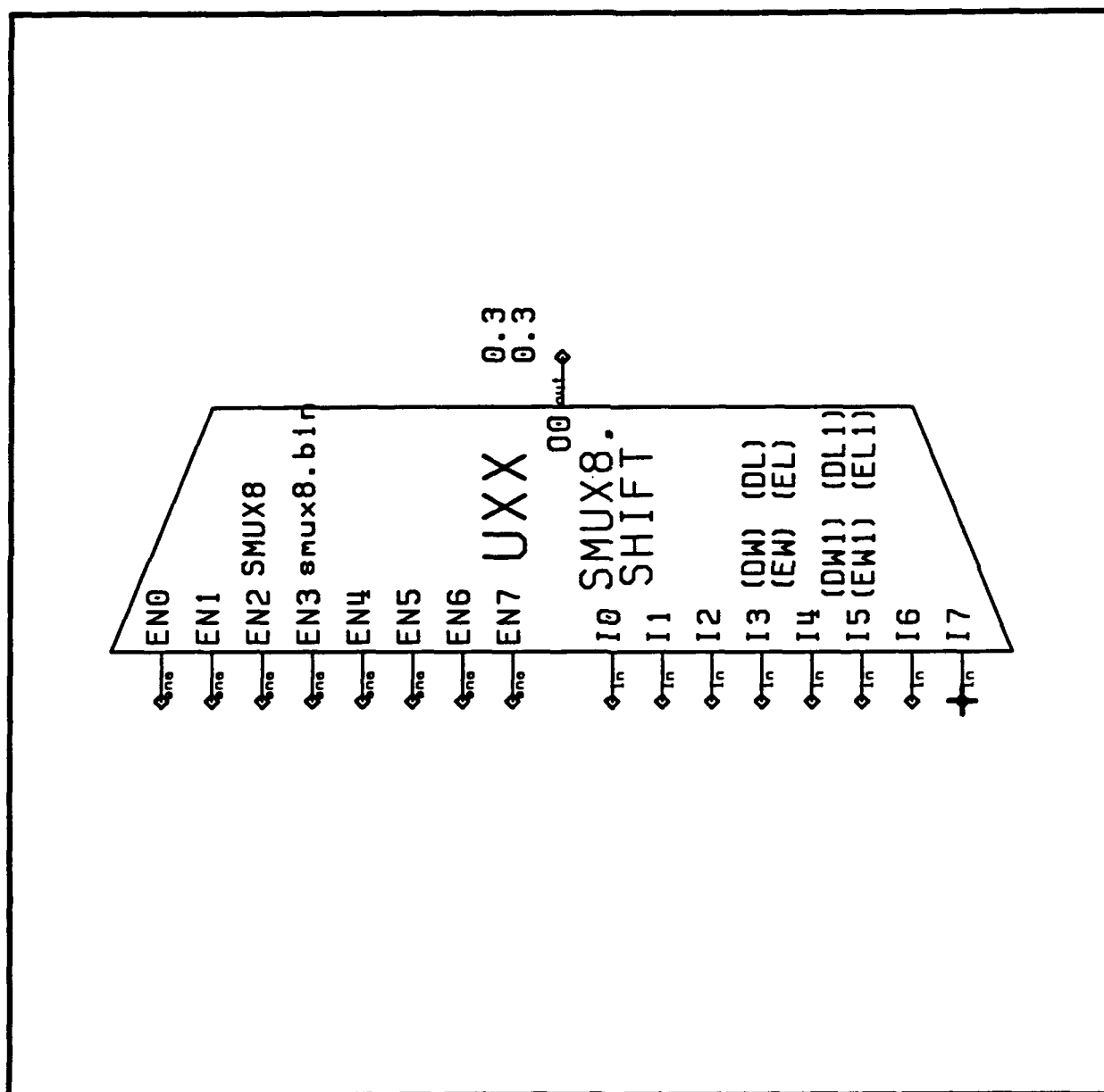


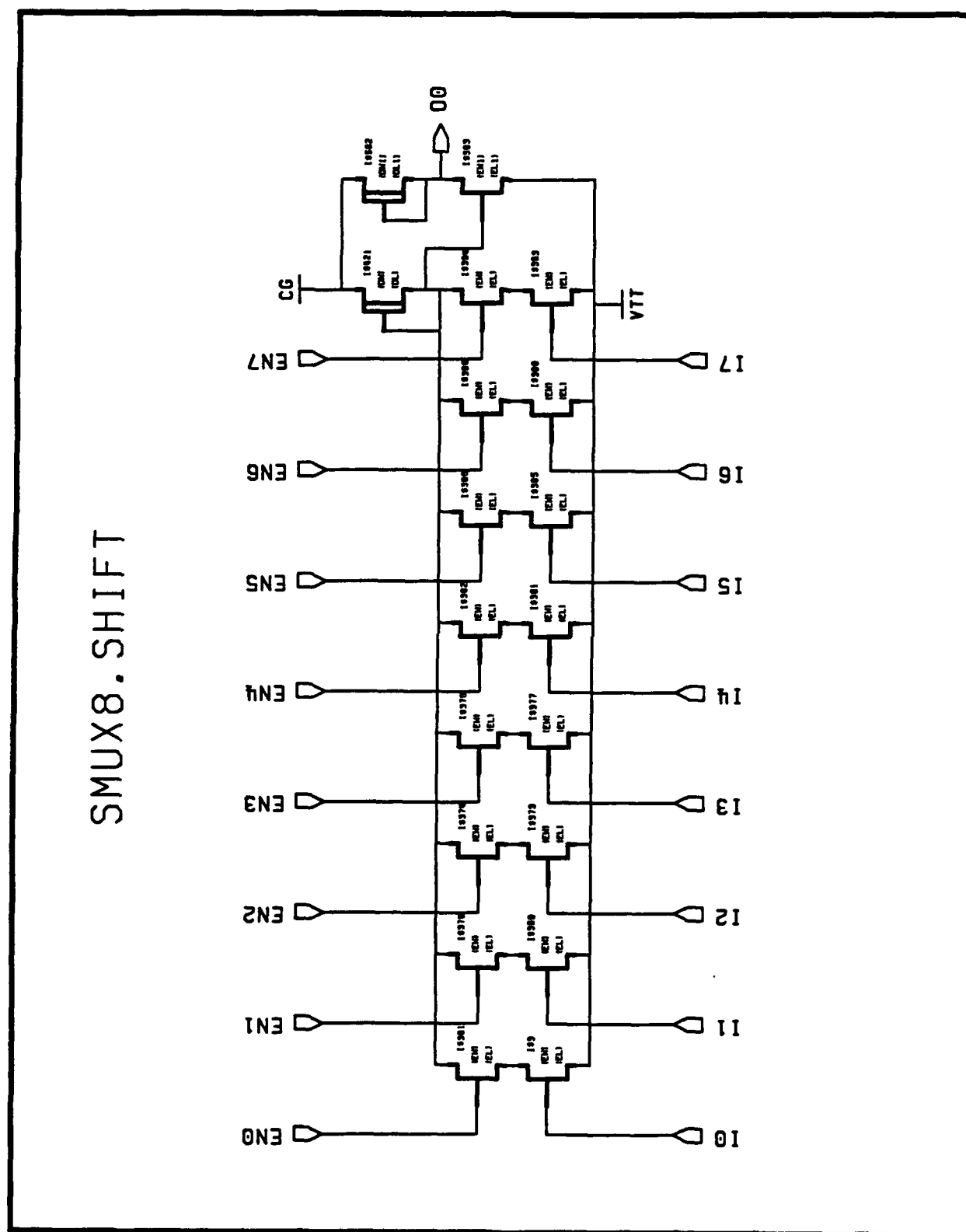


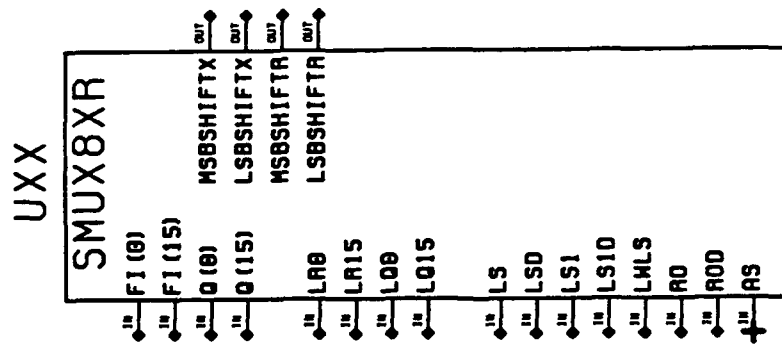


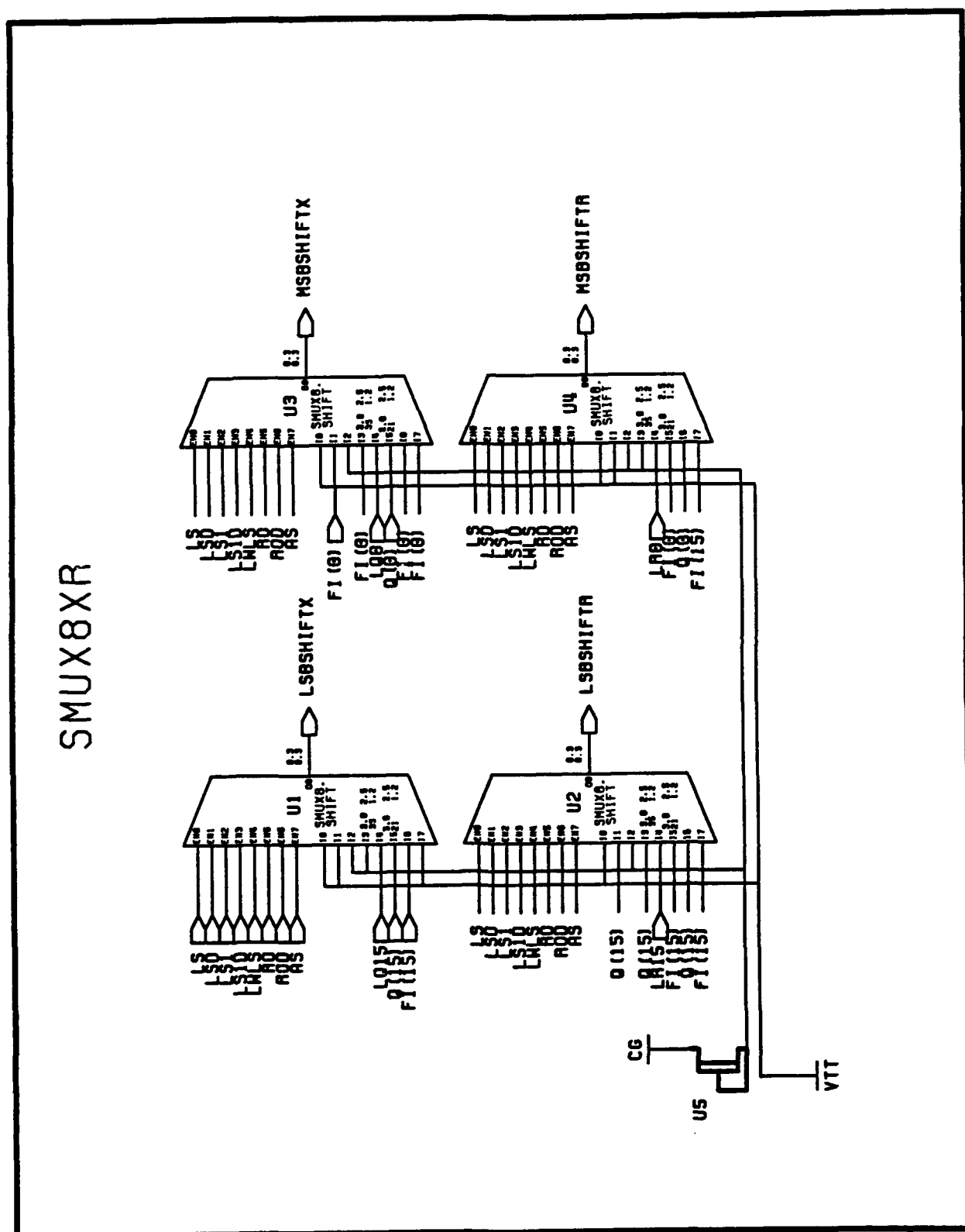


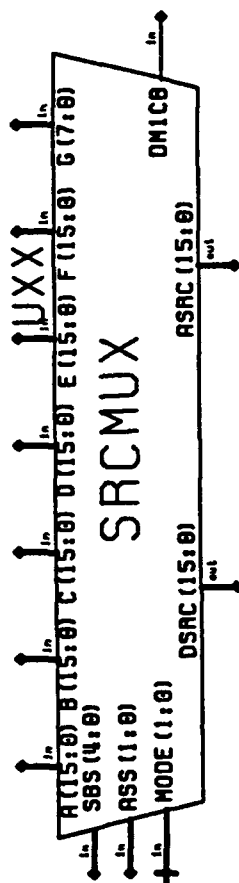


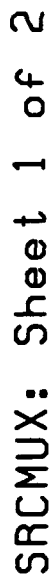




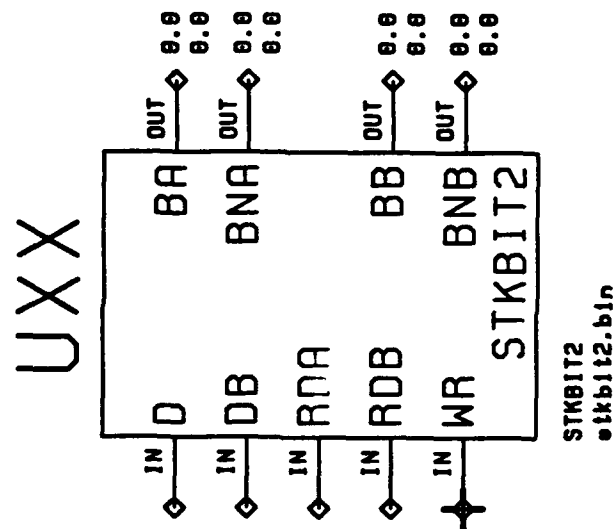


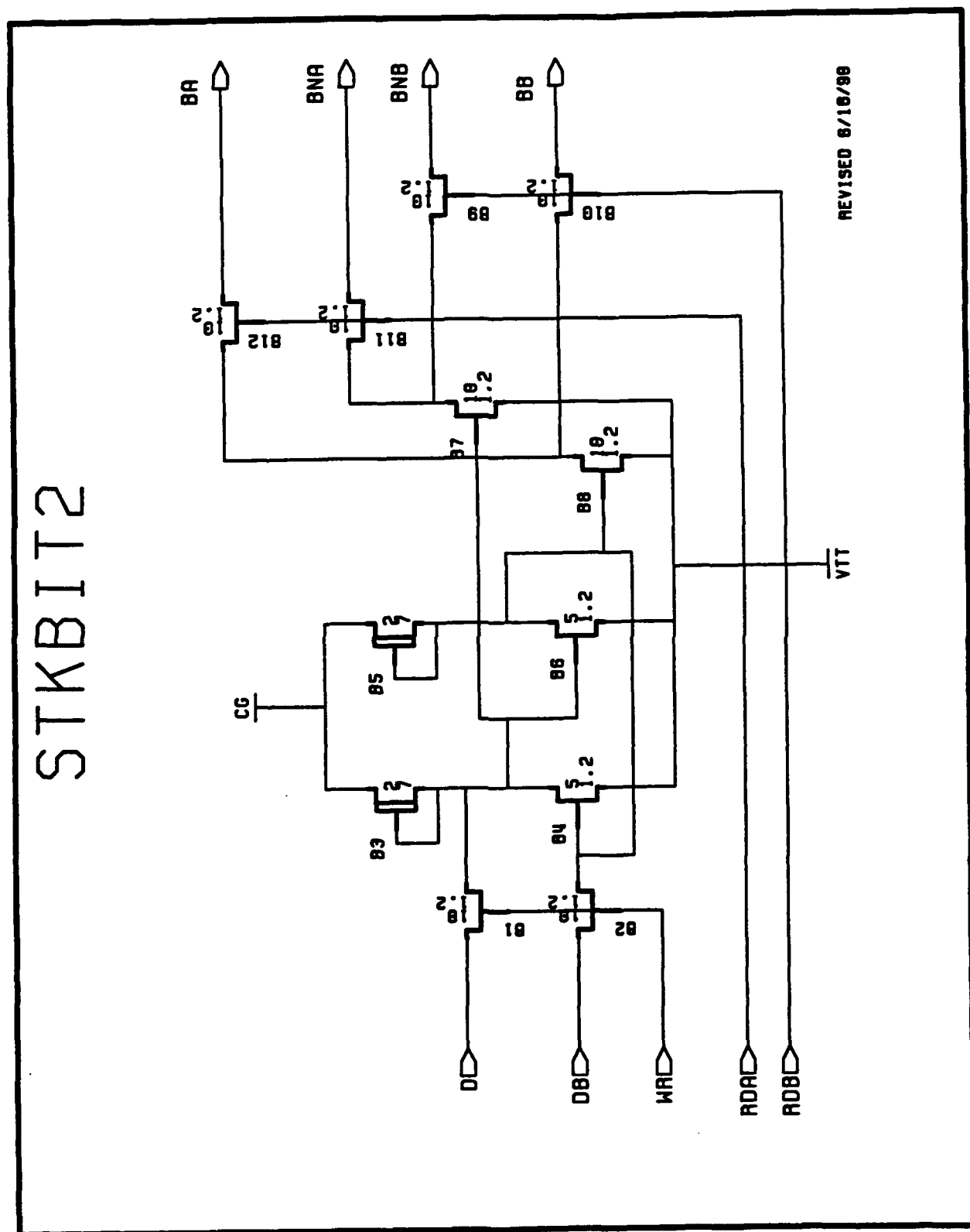


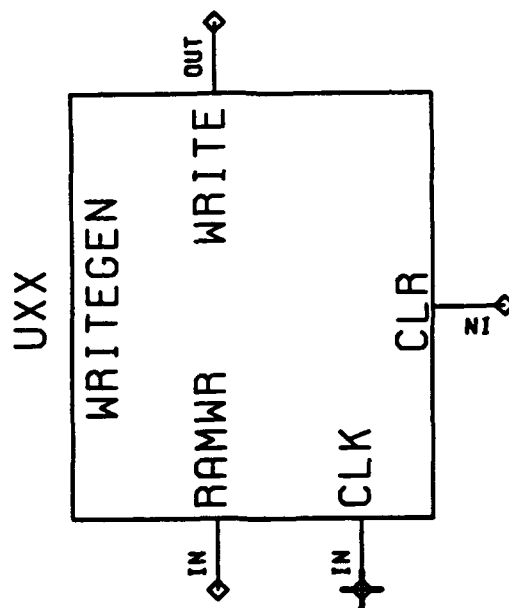




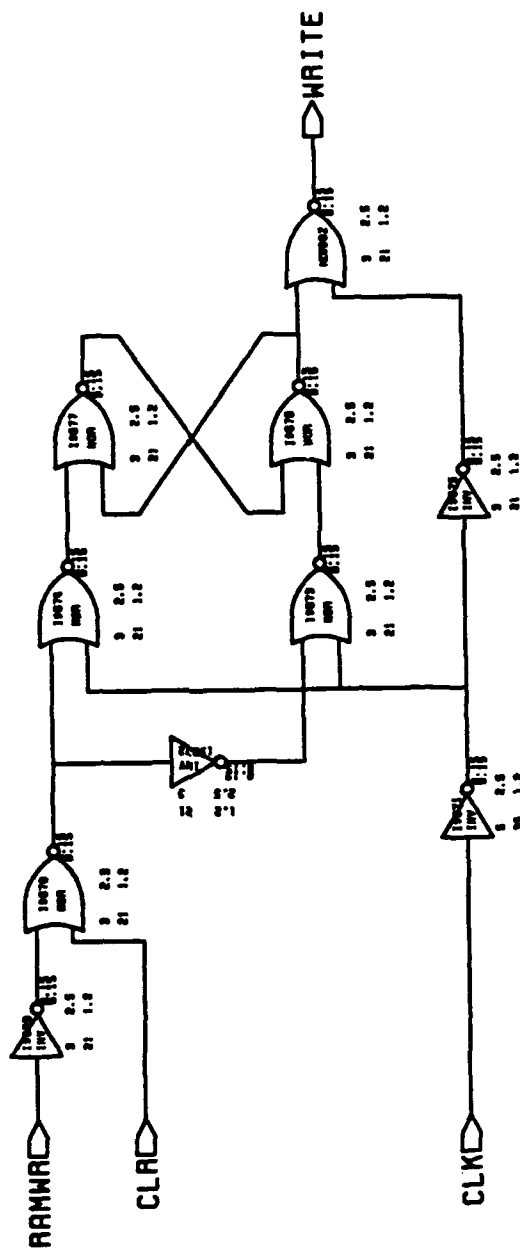


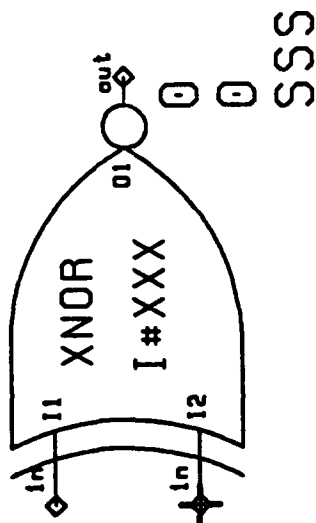


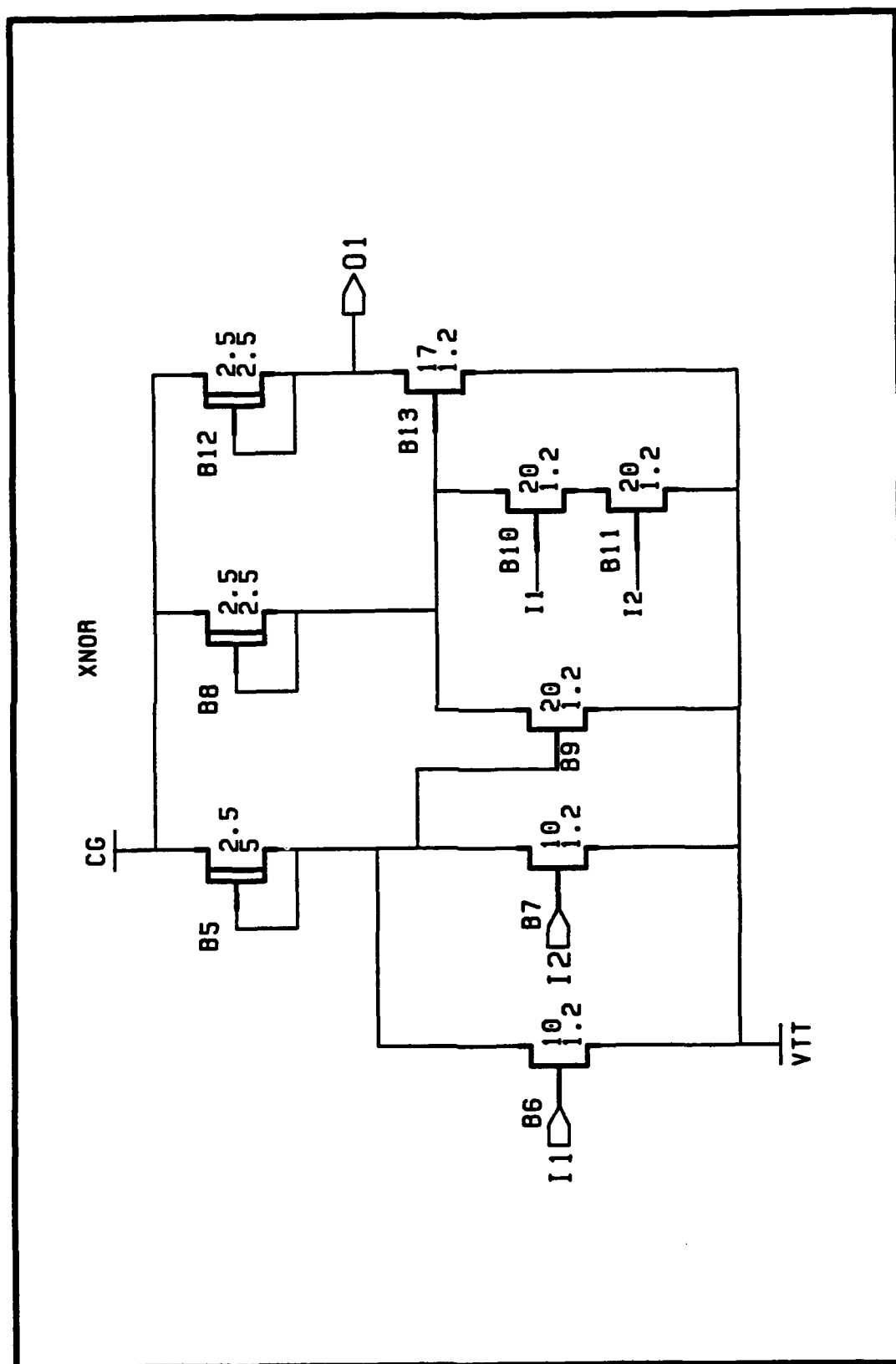


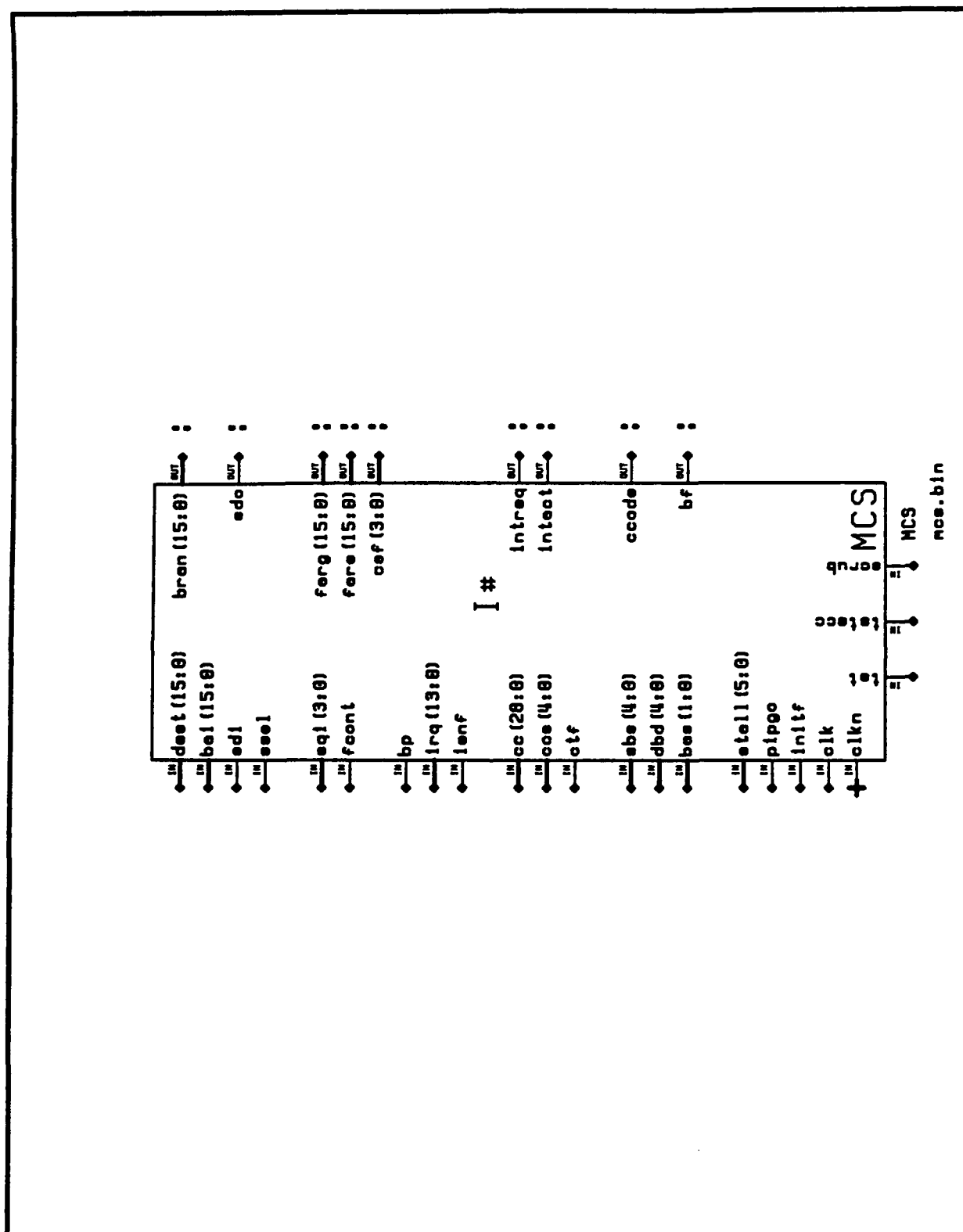


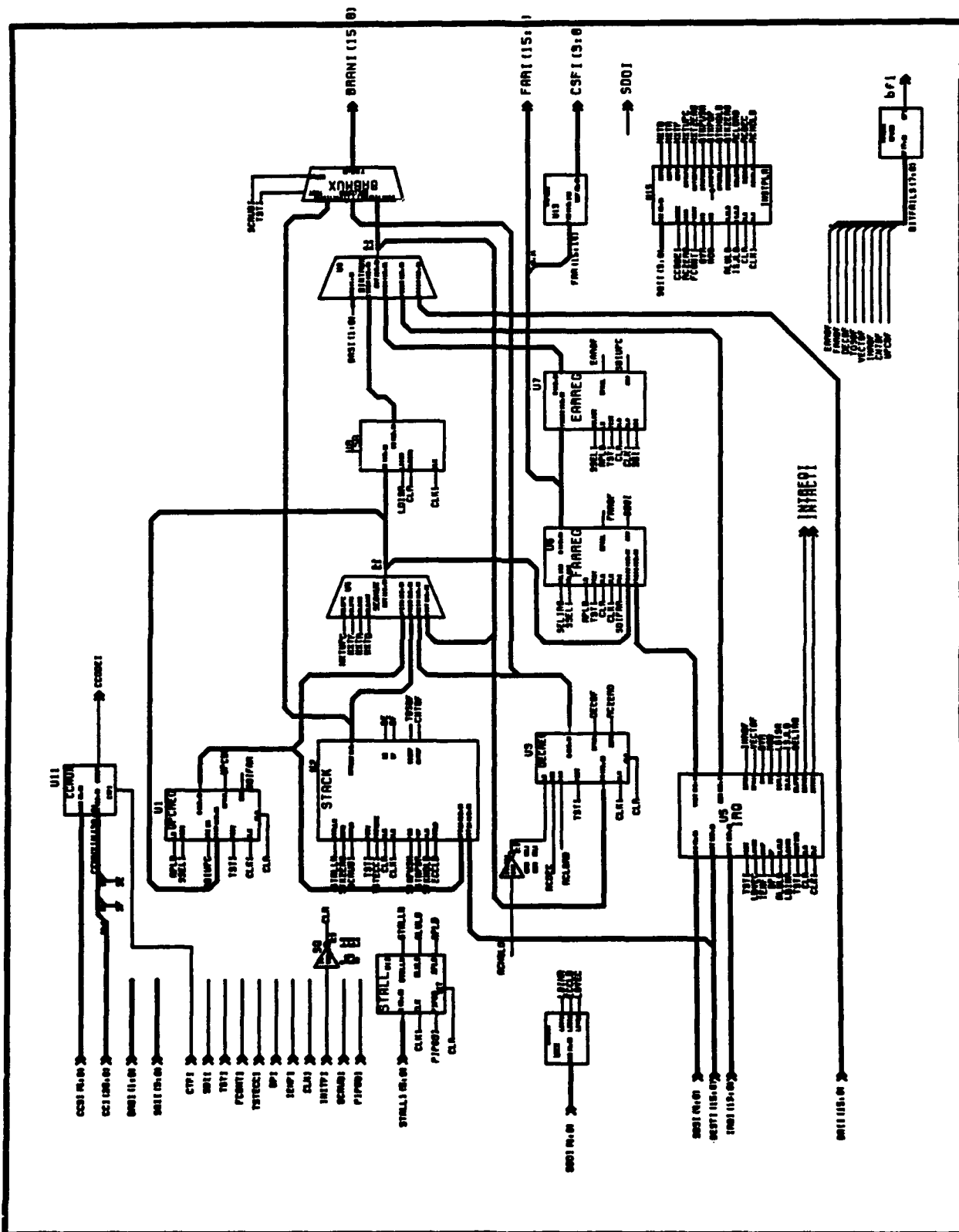
# WRITEGEN: RAM WRITE PULSE GENERATOR



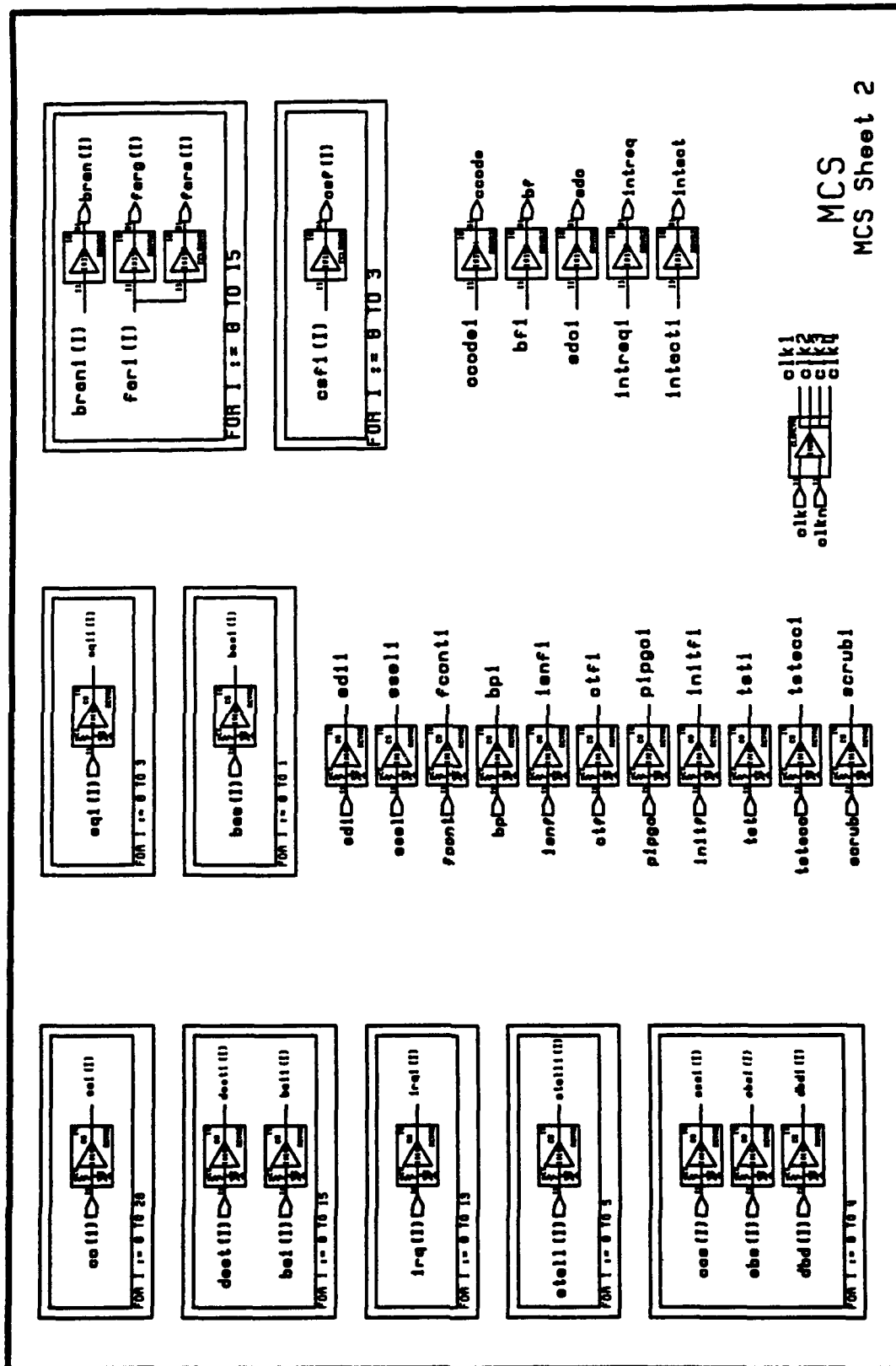


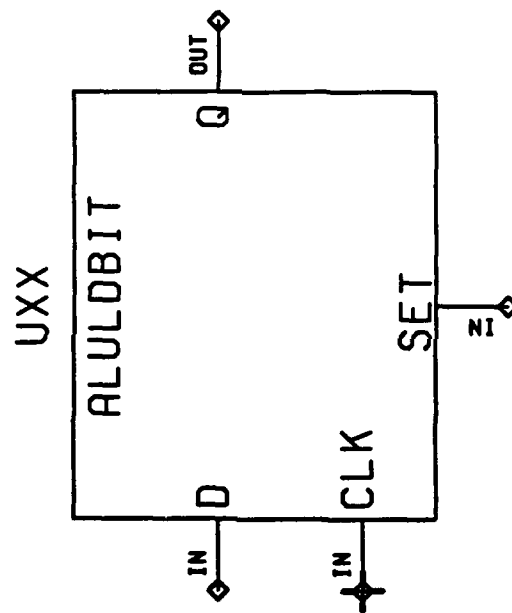


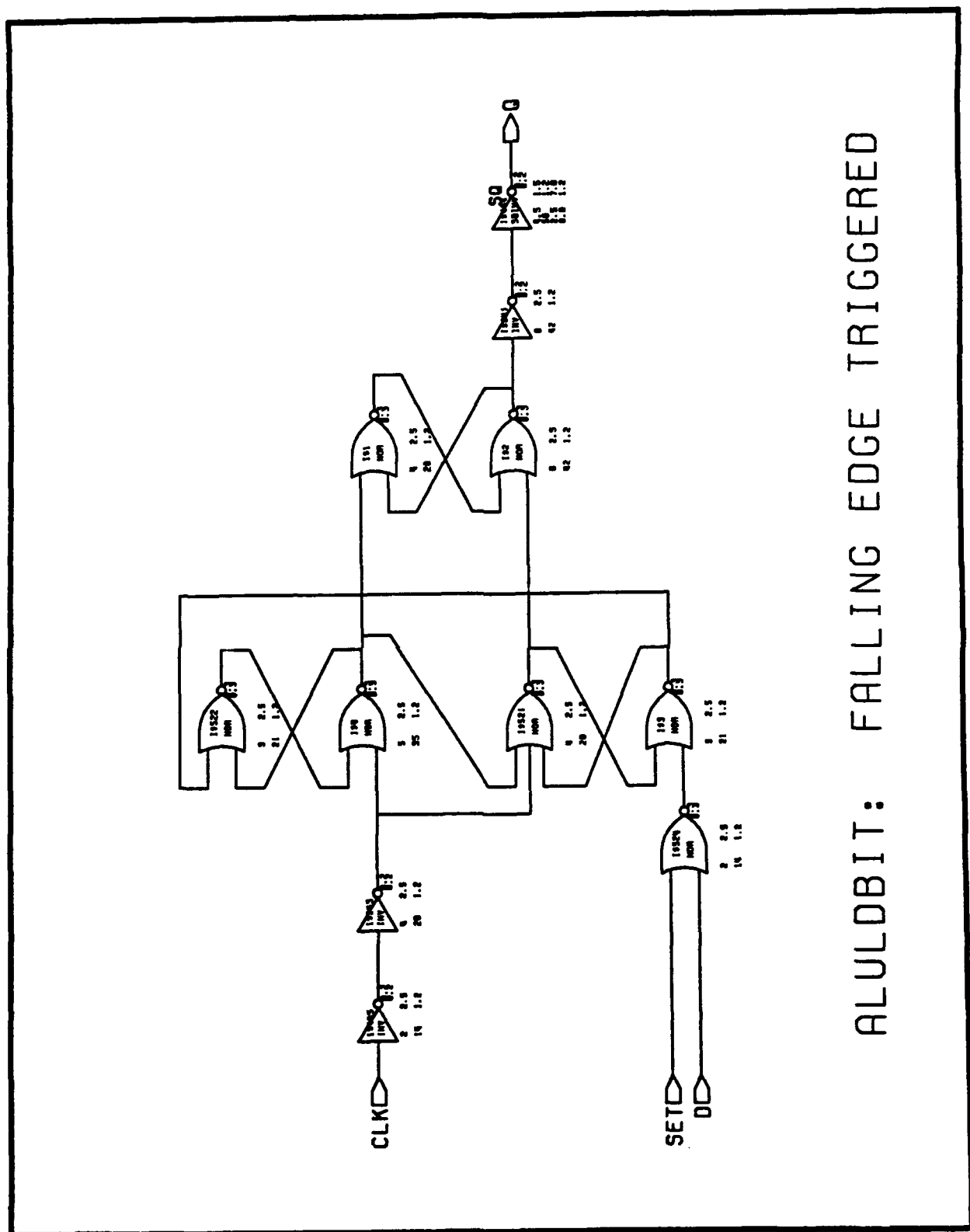


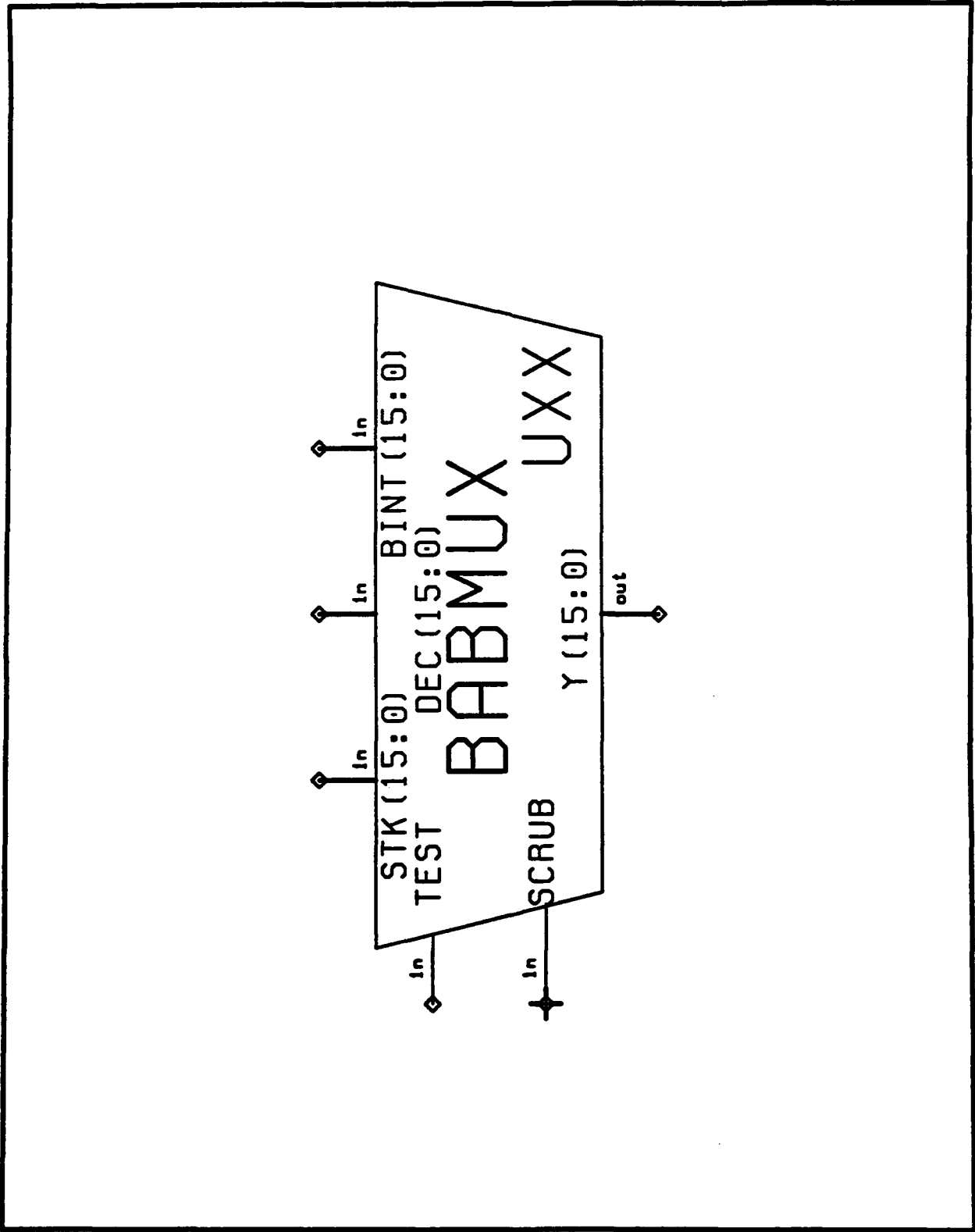


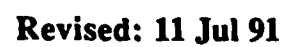


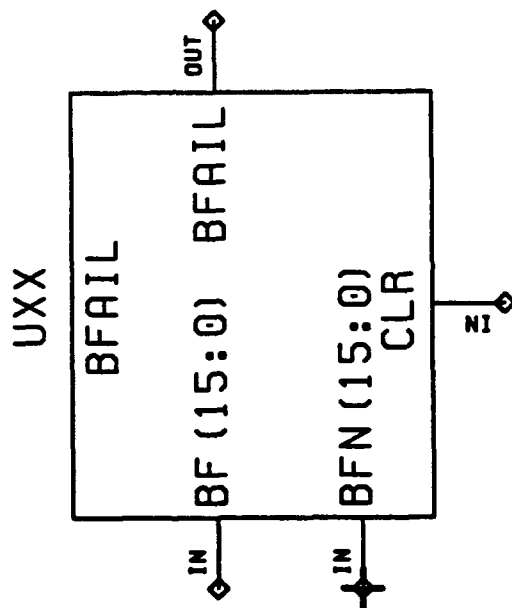


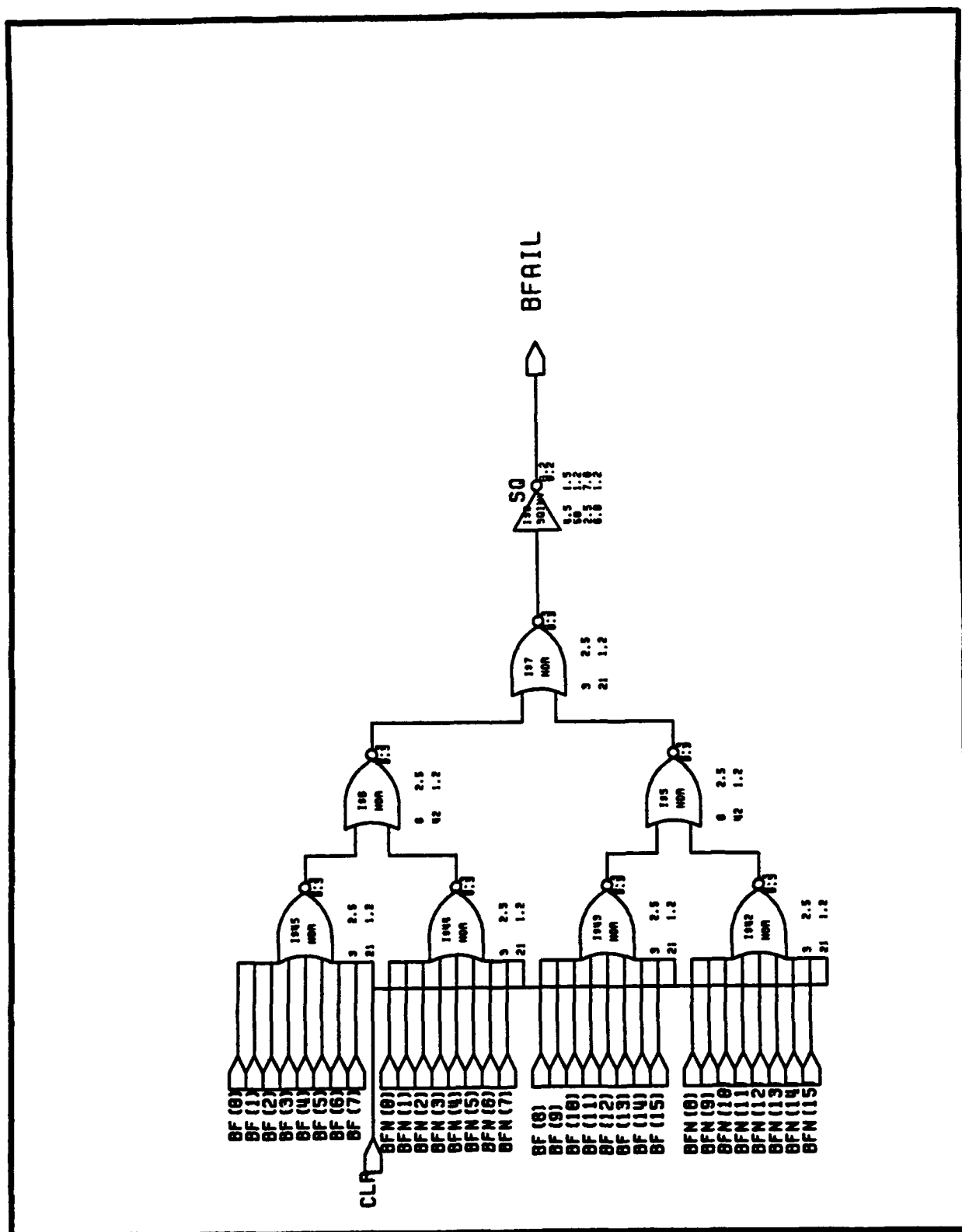


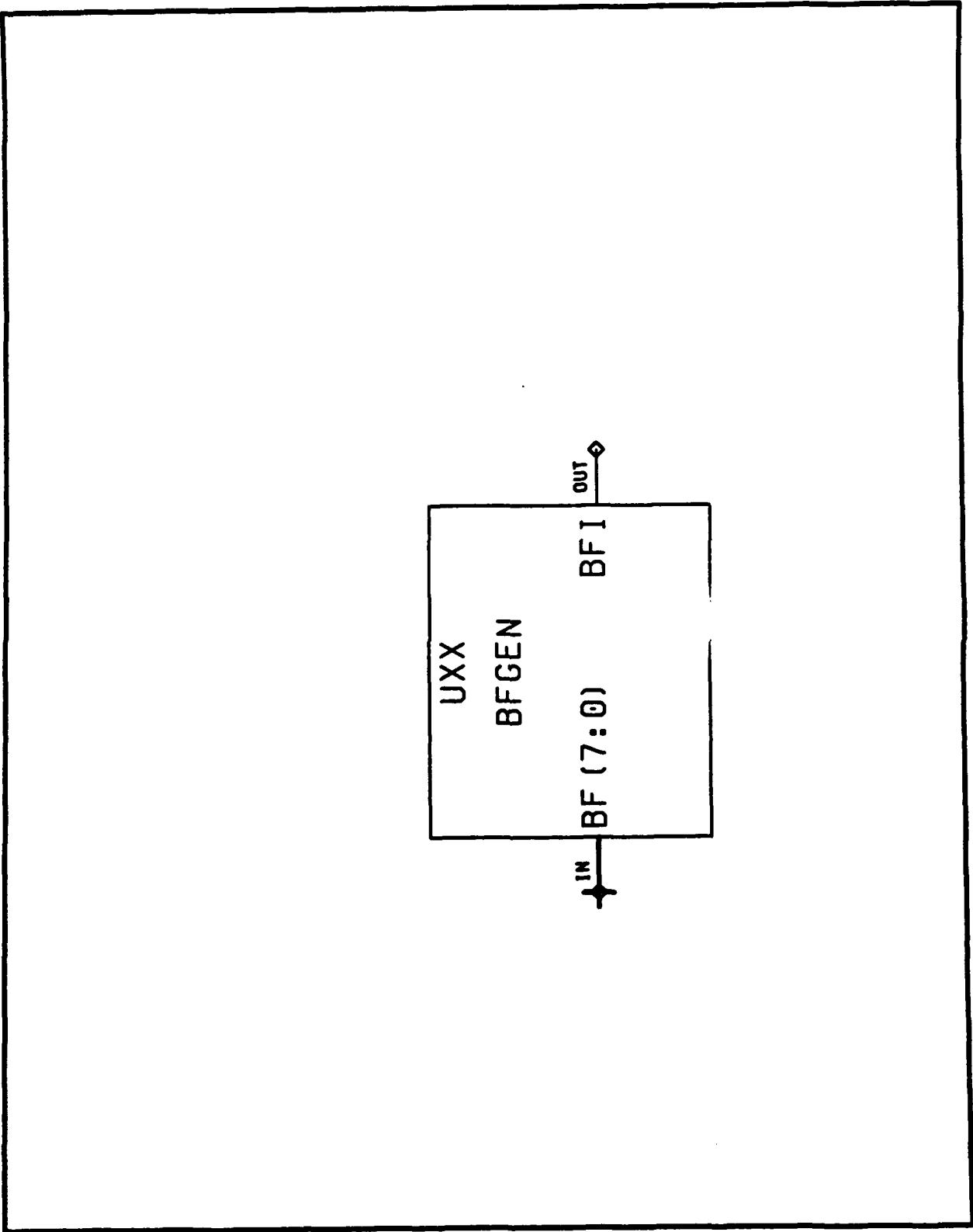






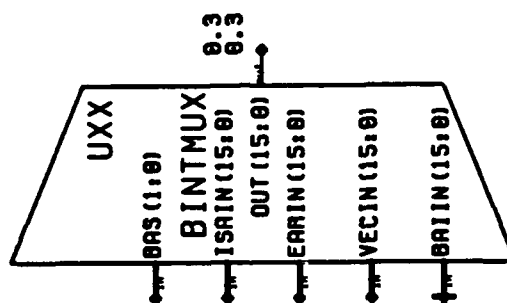


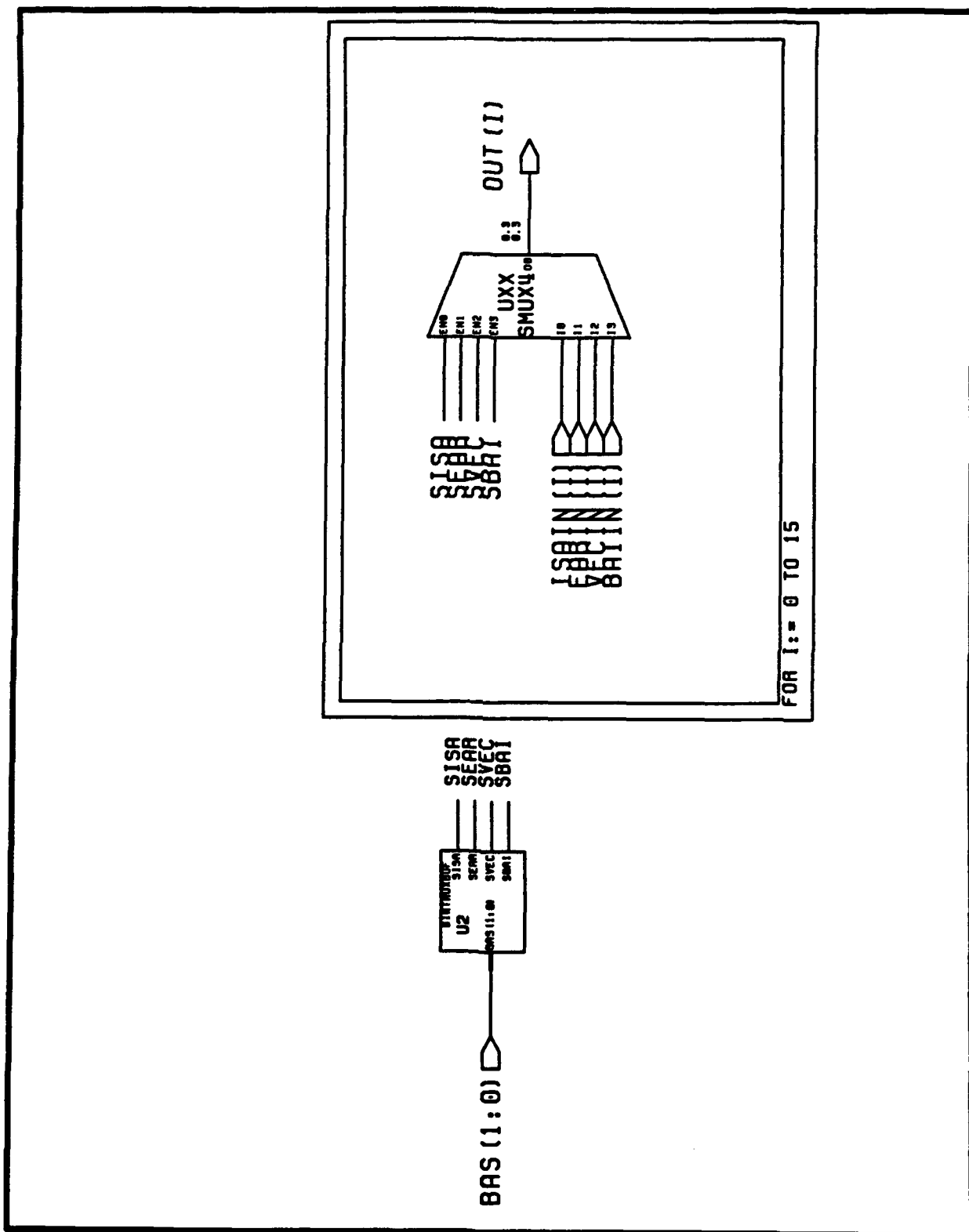


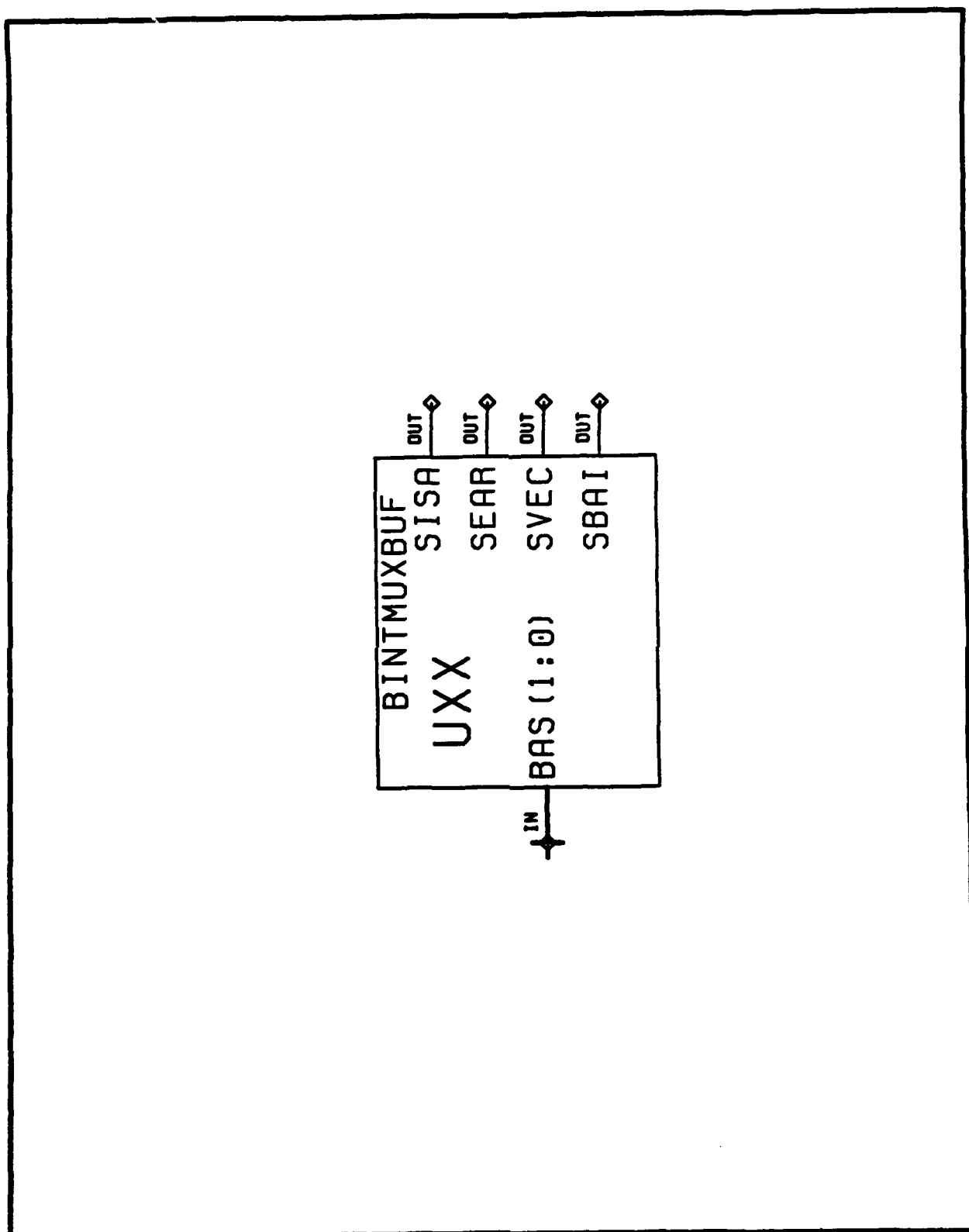


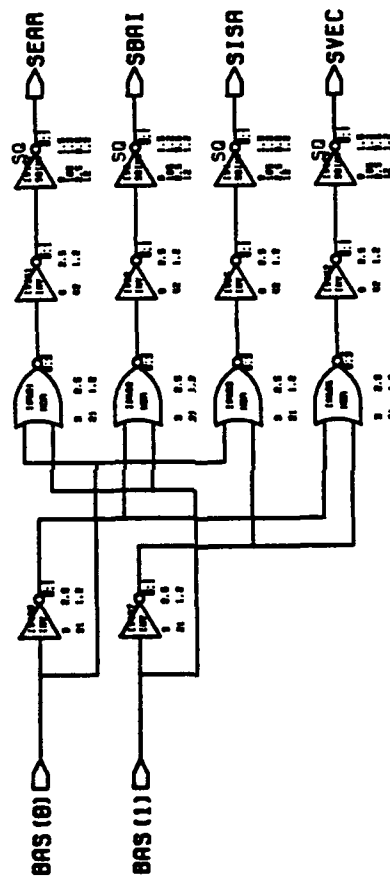


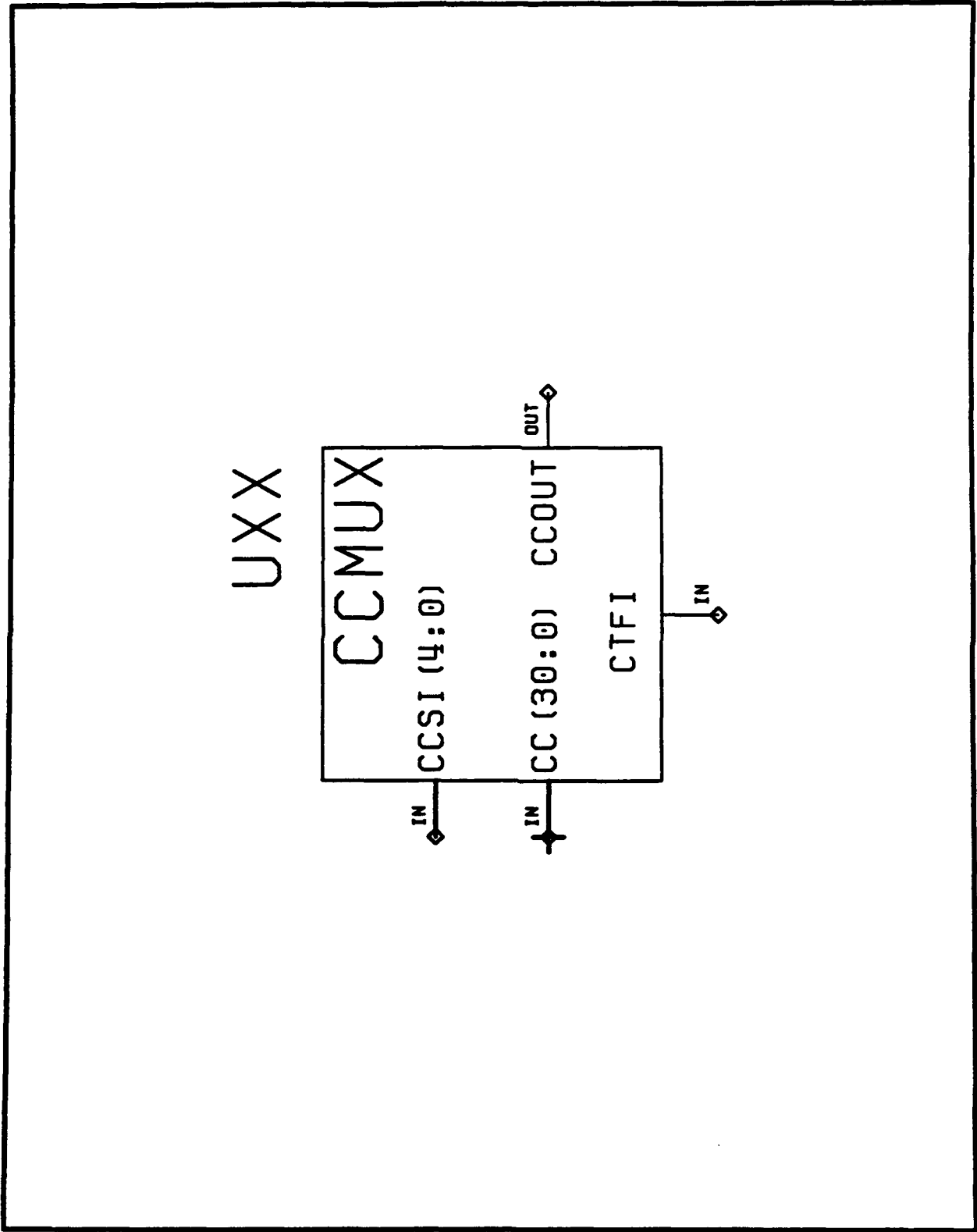


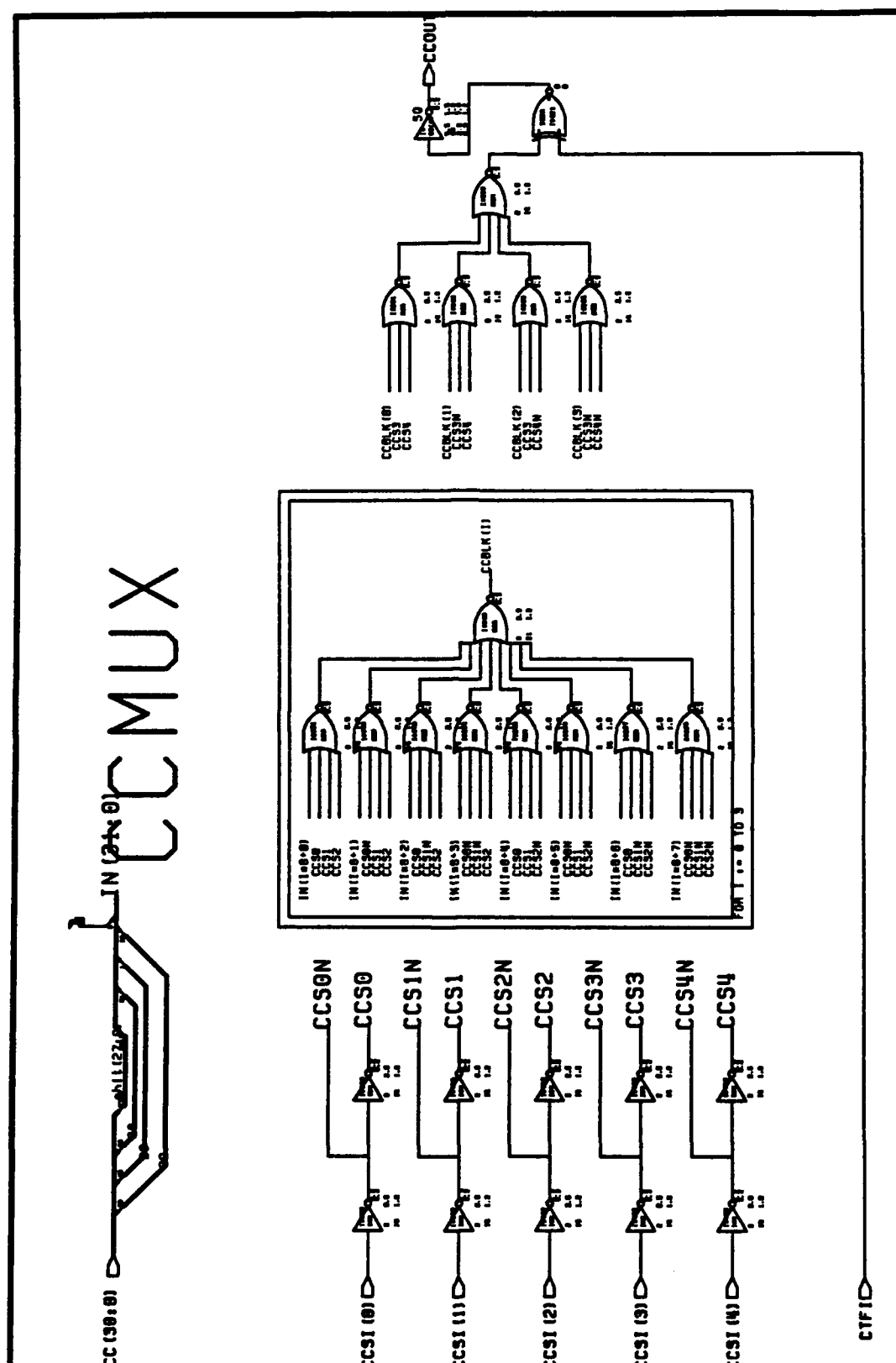






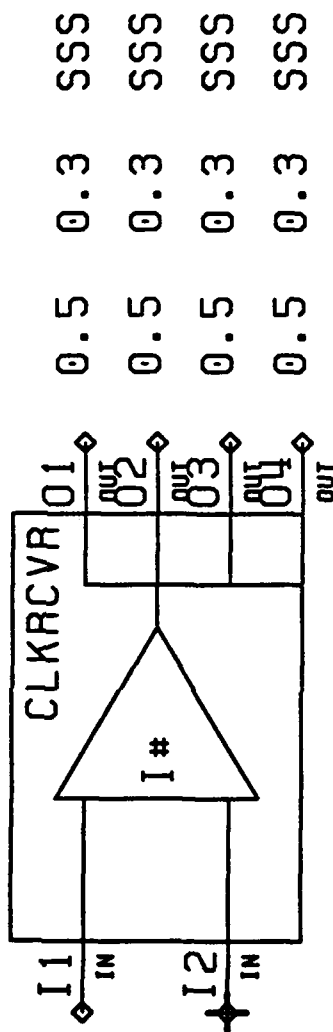






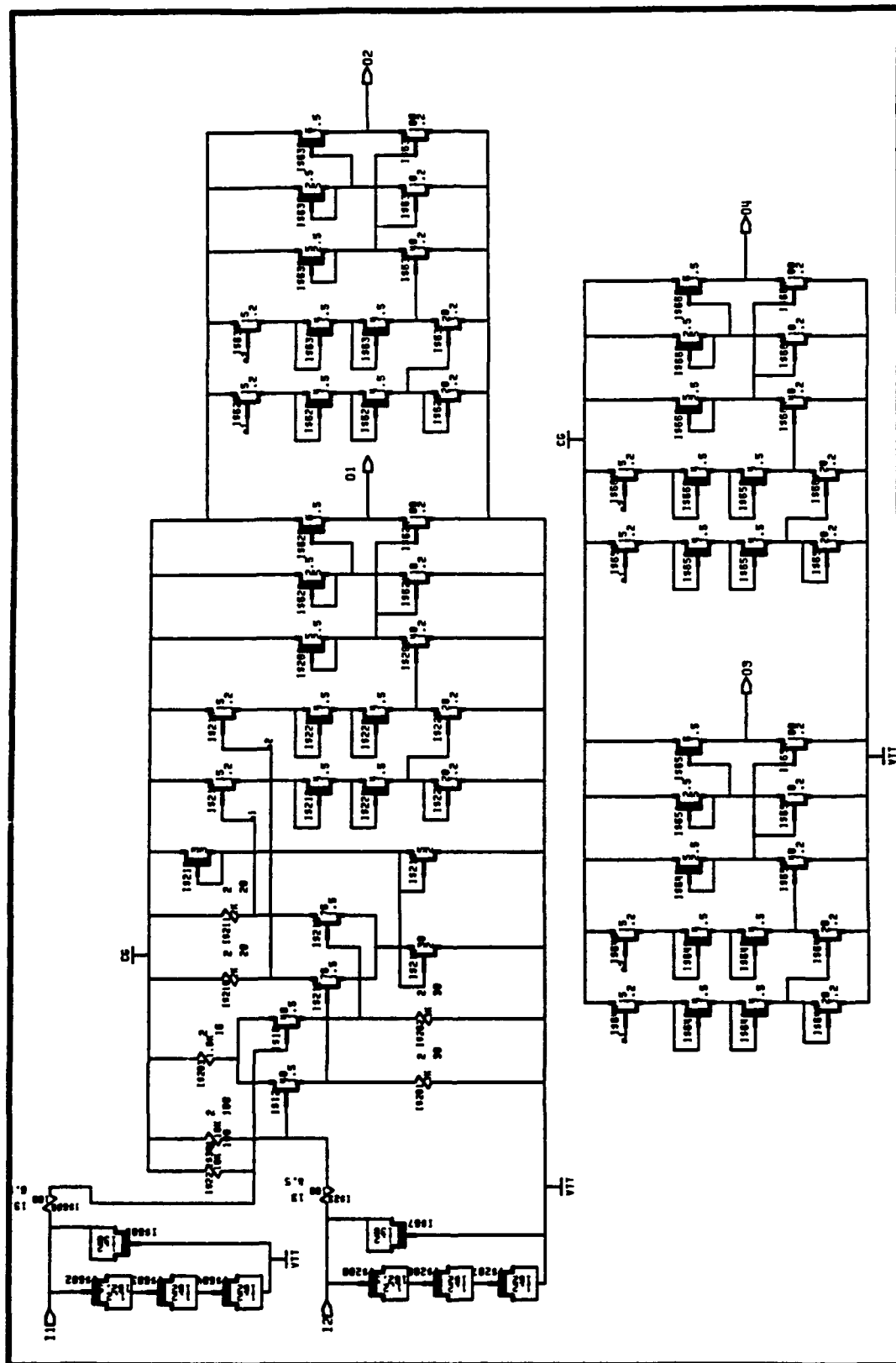
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Version 0.8

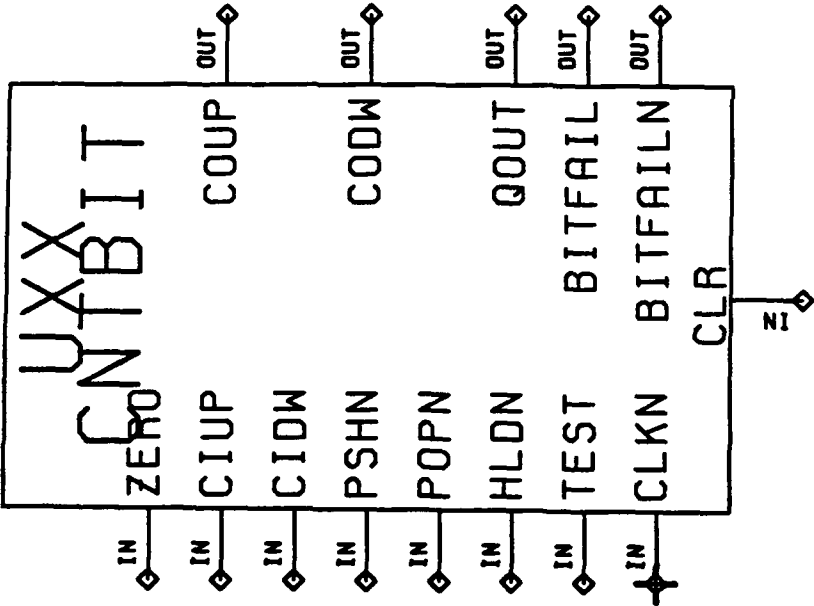
NAME: CLKRCVR  
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER

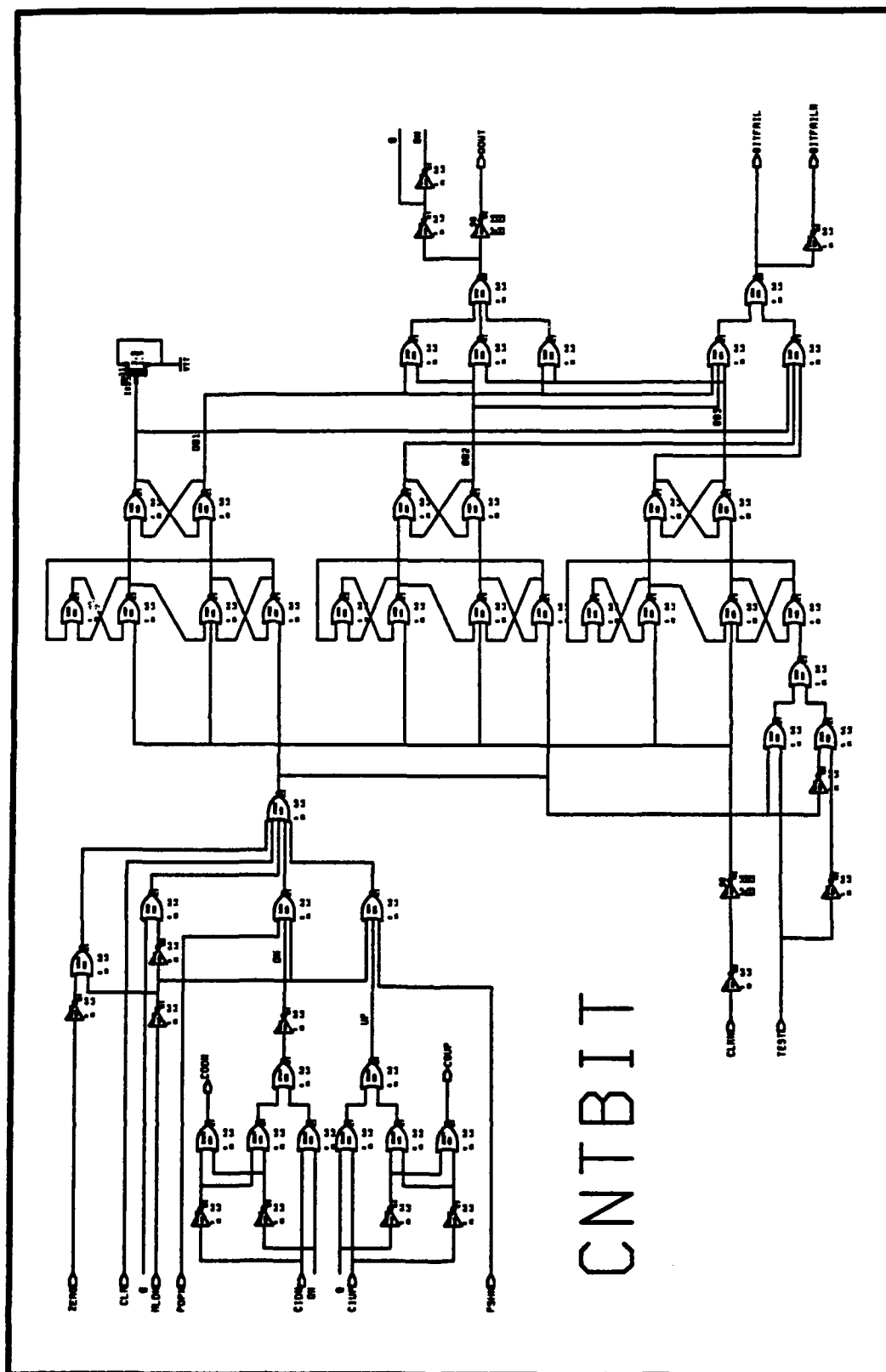


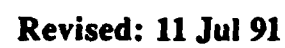
CLKRCVR  
clkrcvr.bin

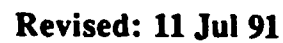


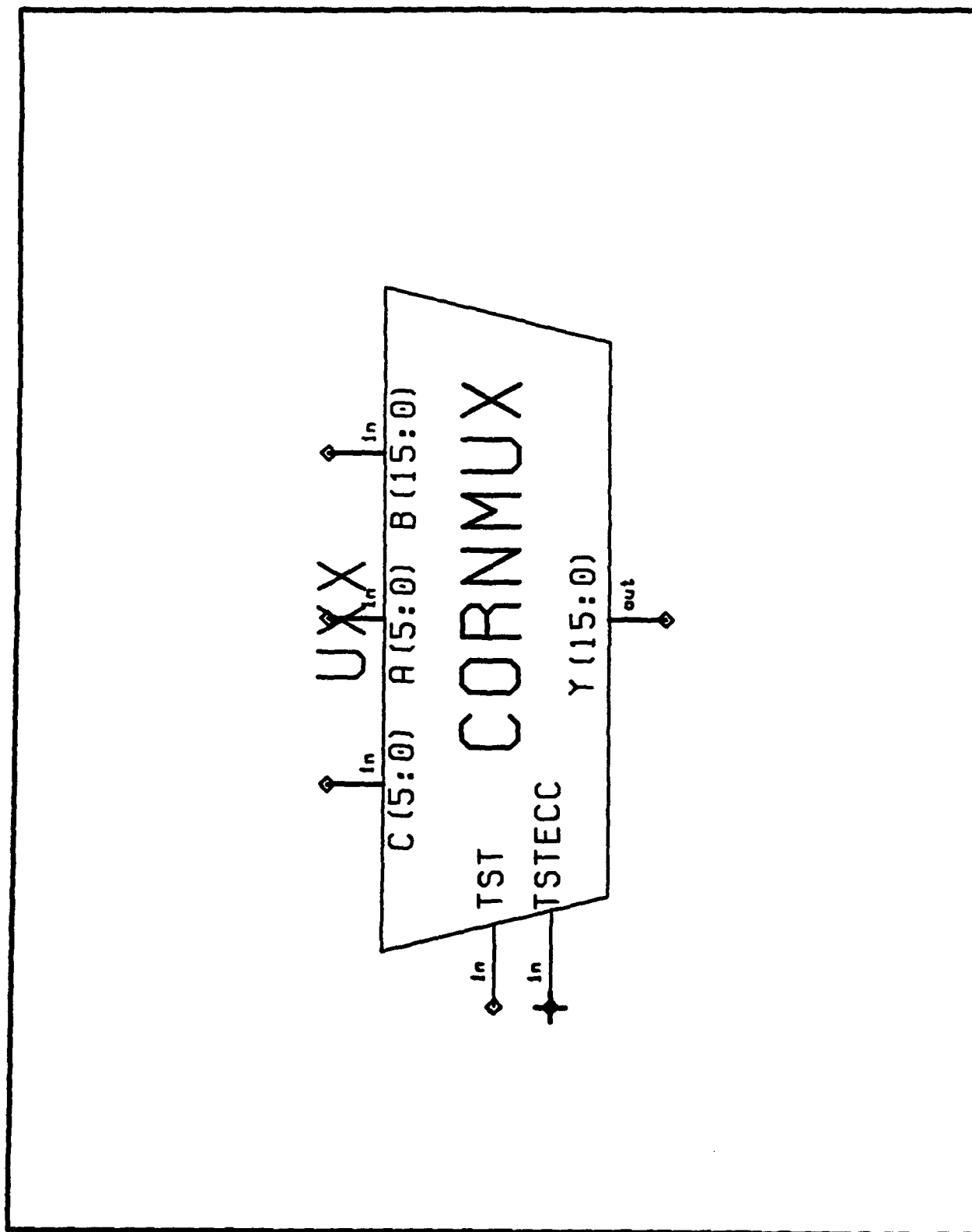




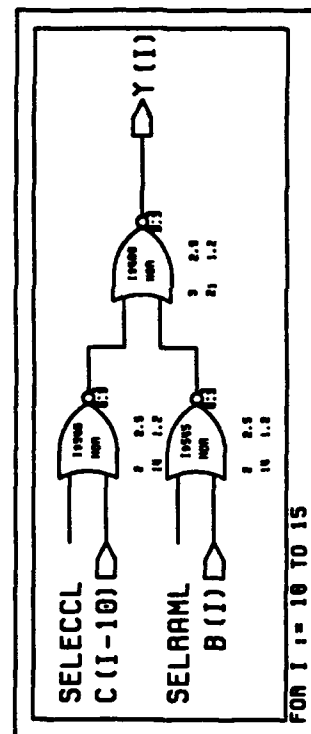
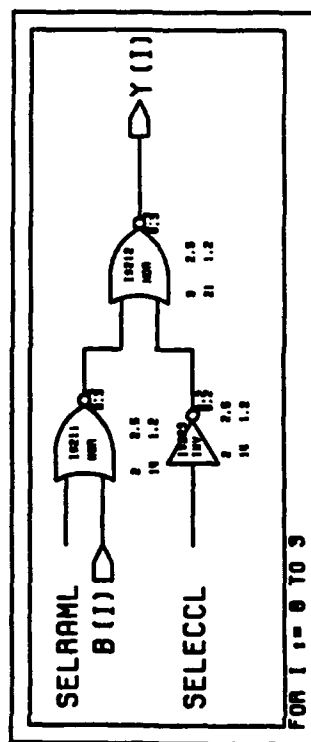
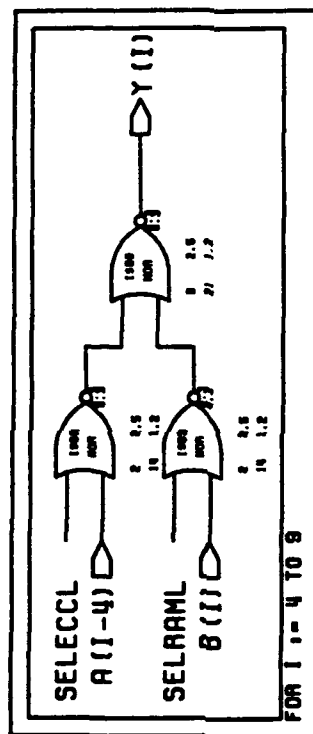
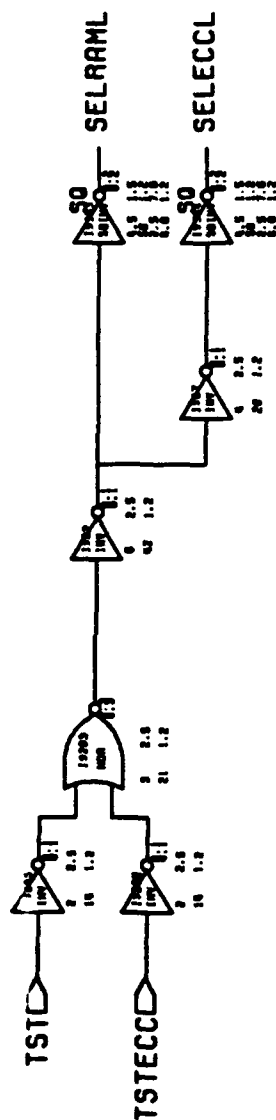


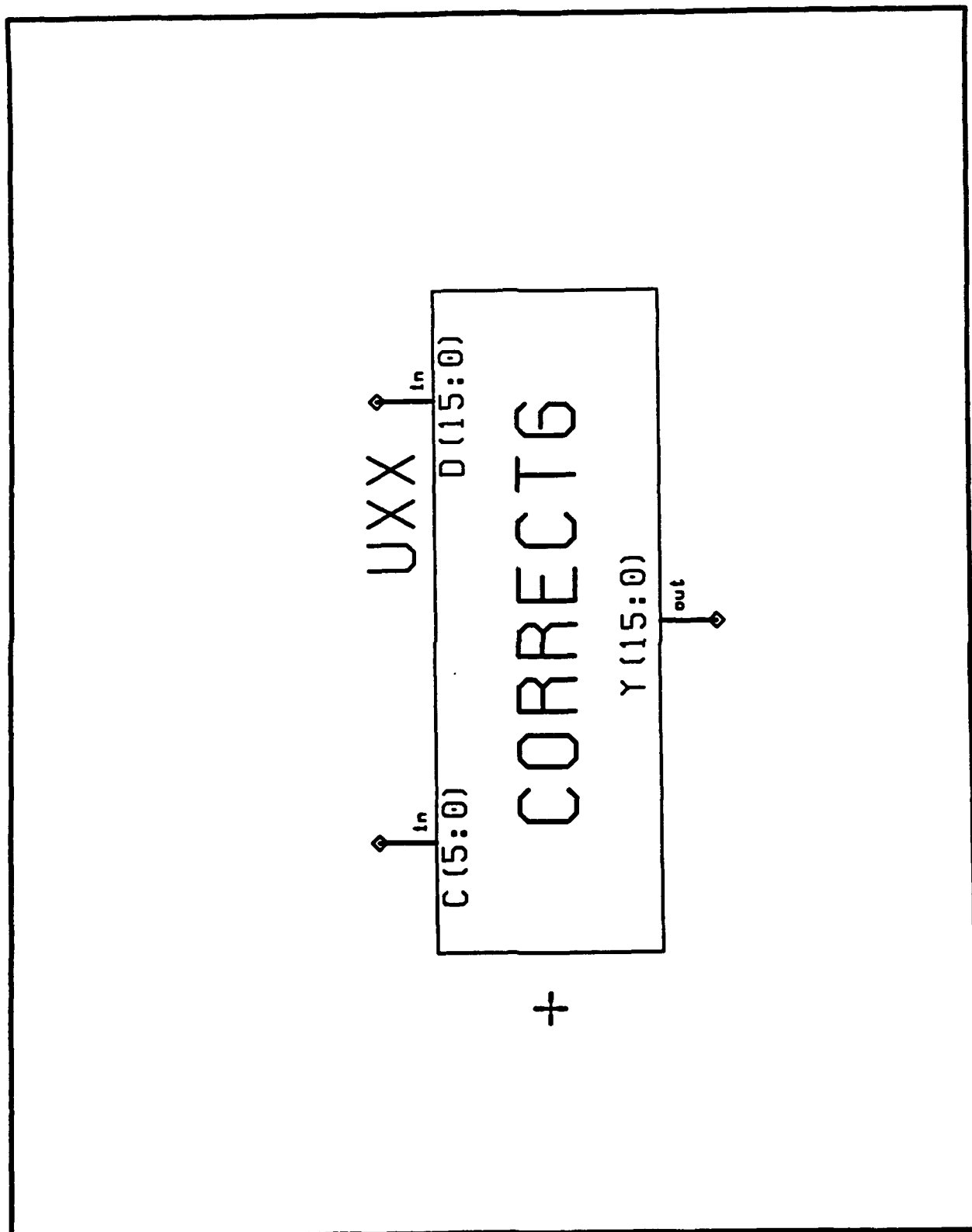




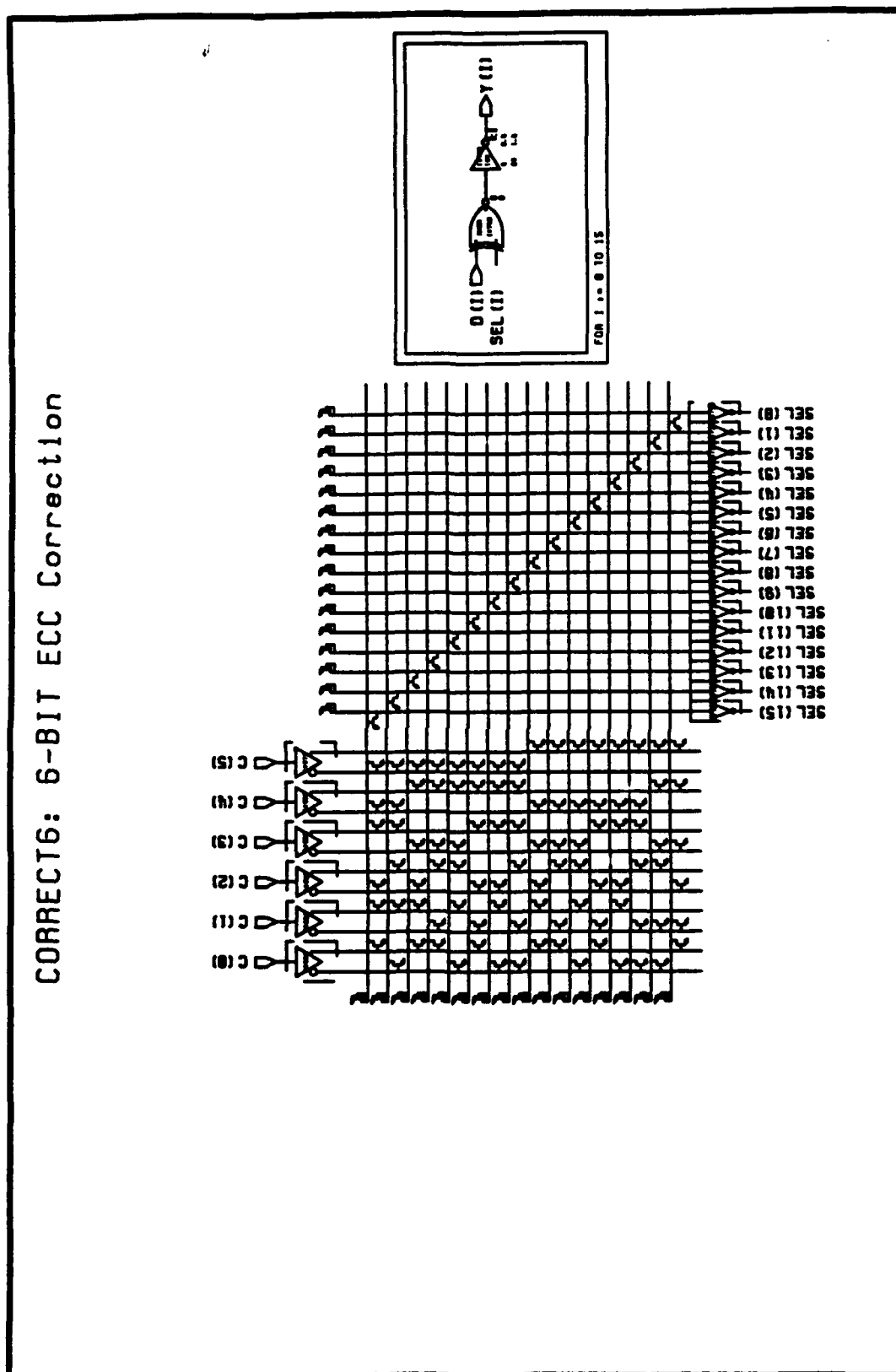


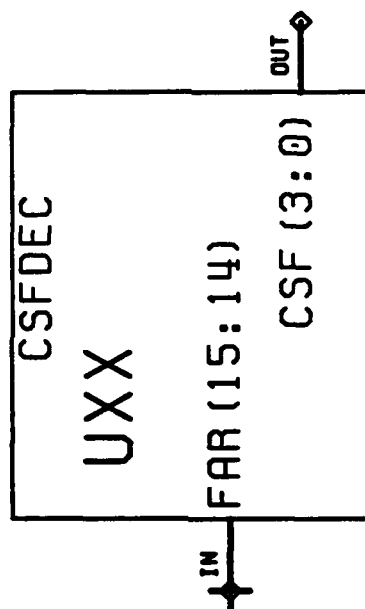
CORNMUX: CORRECTION MUX

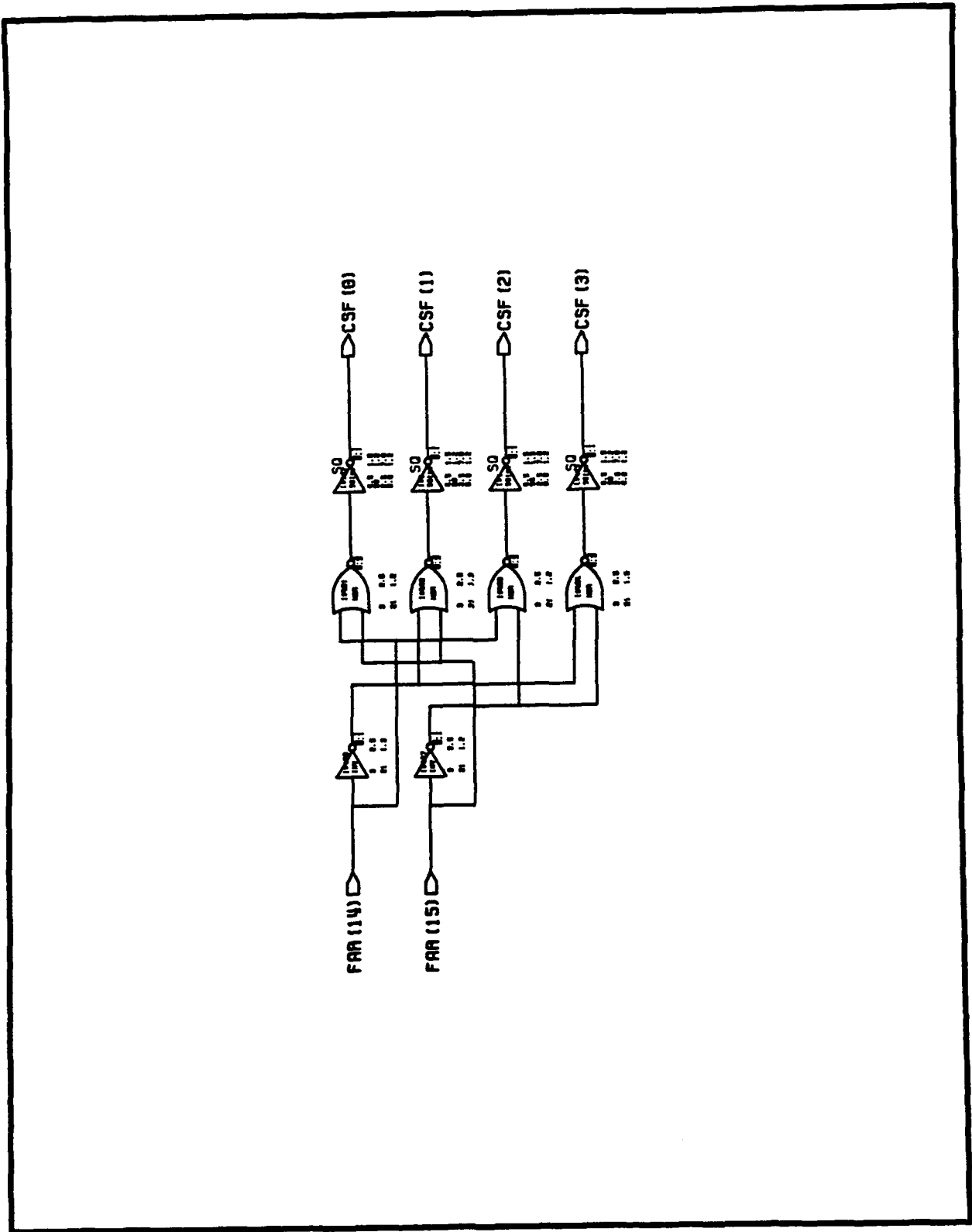


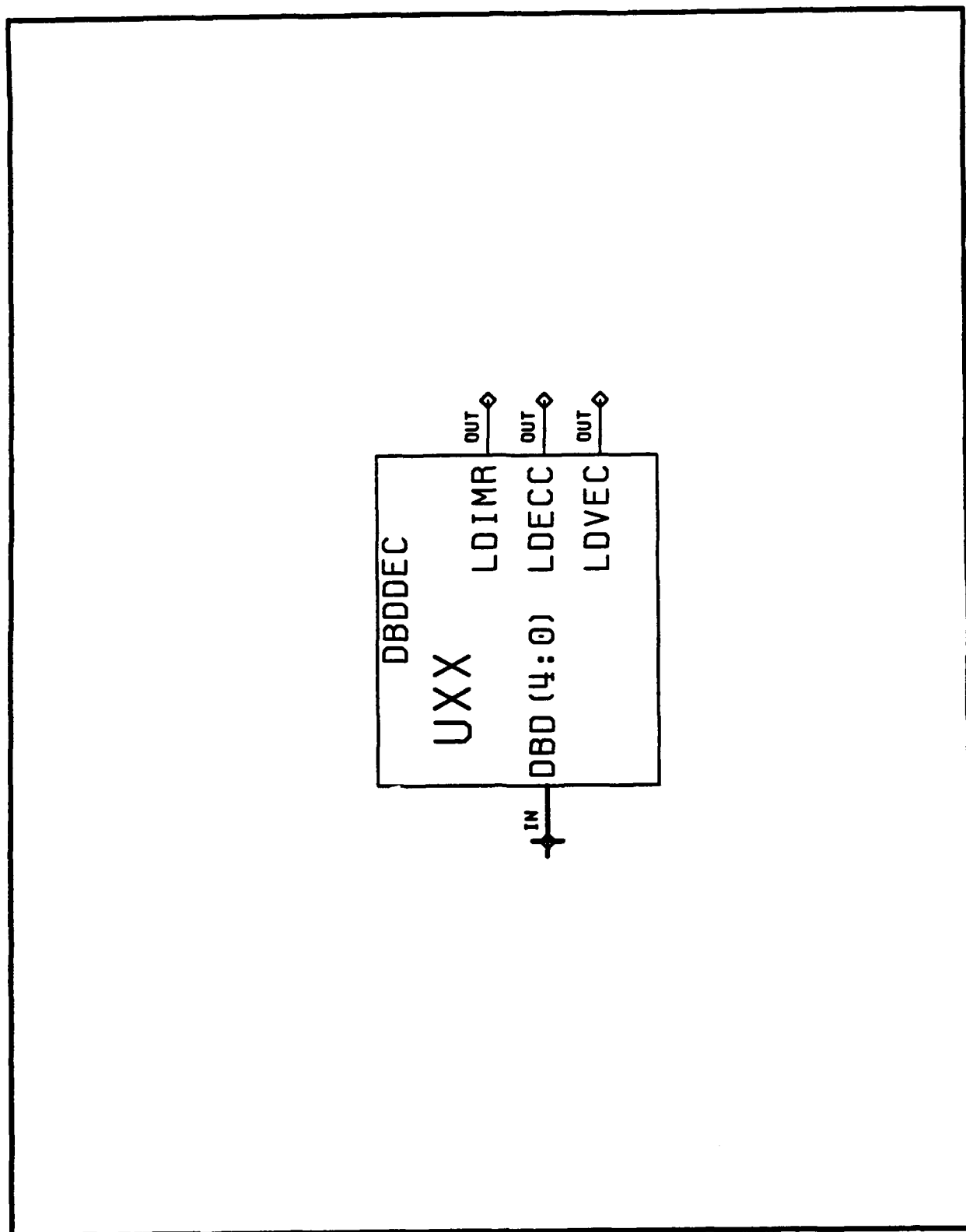


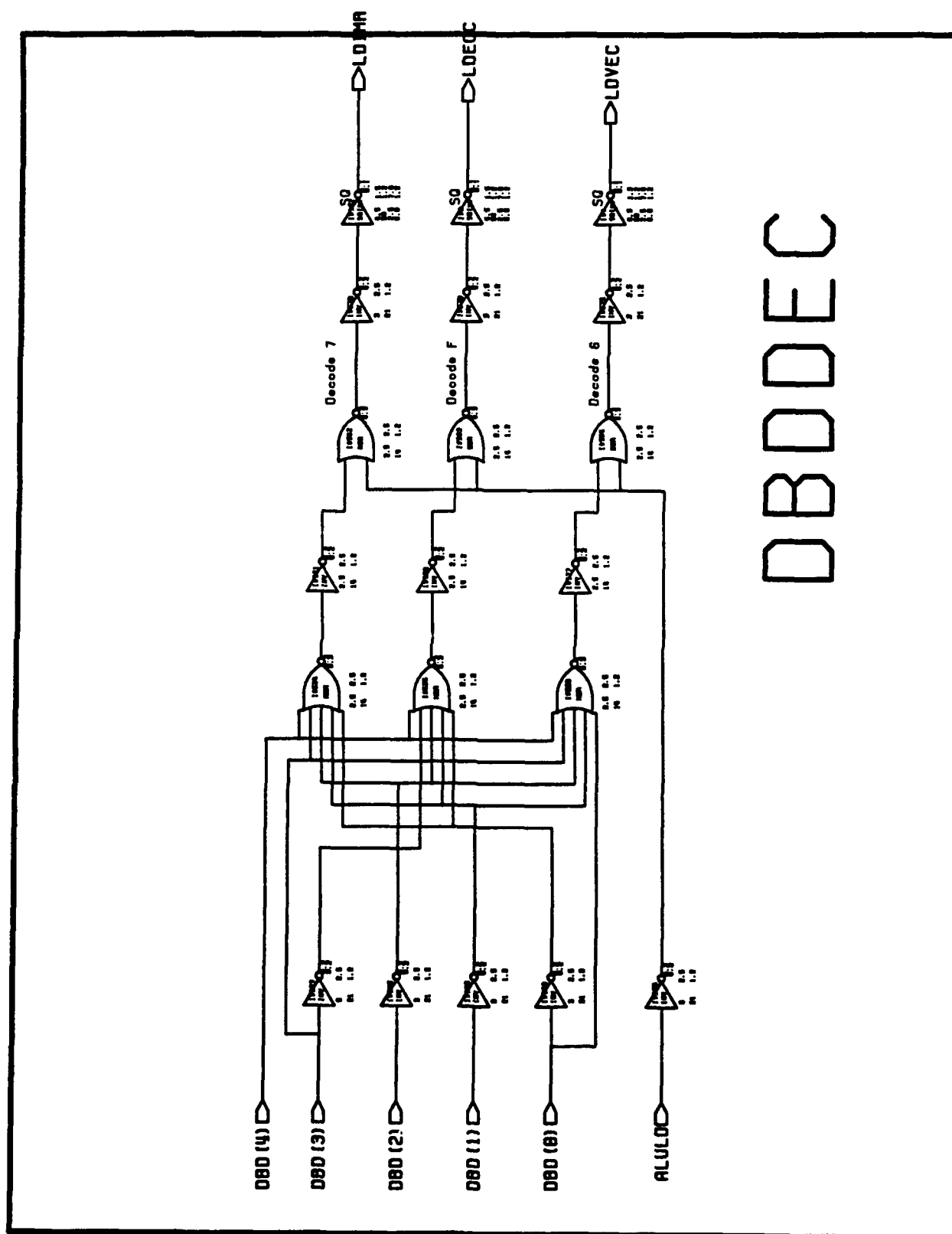


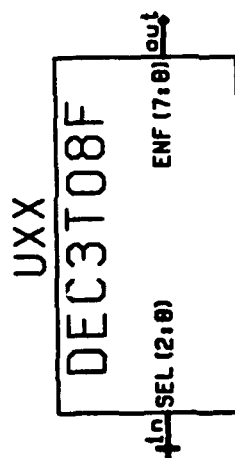


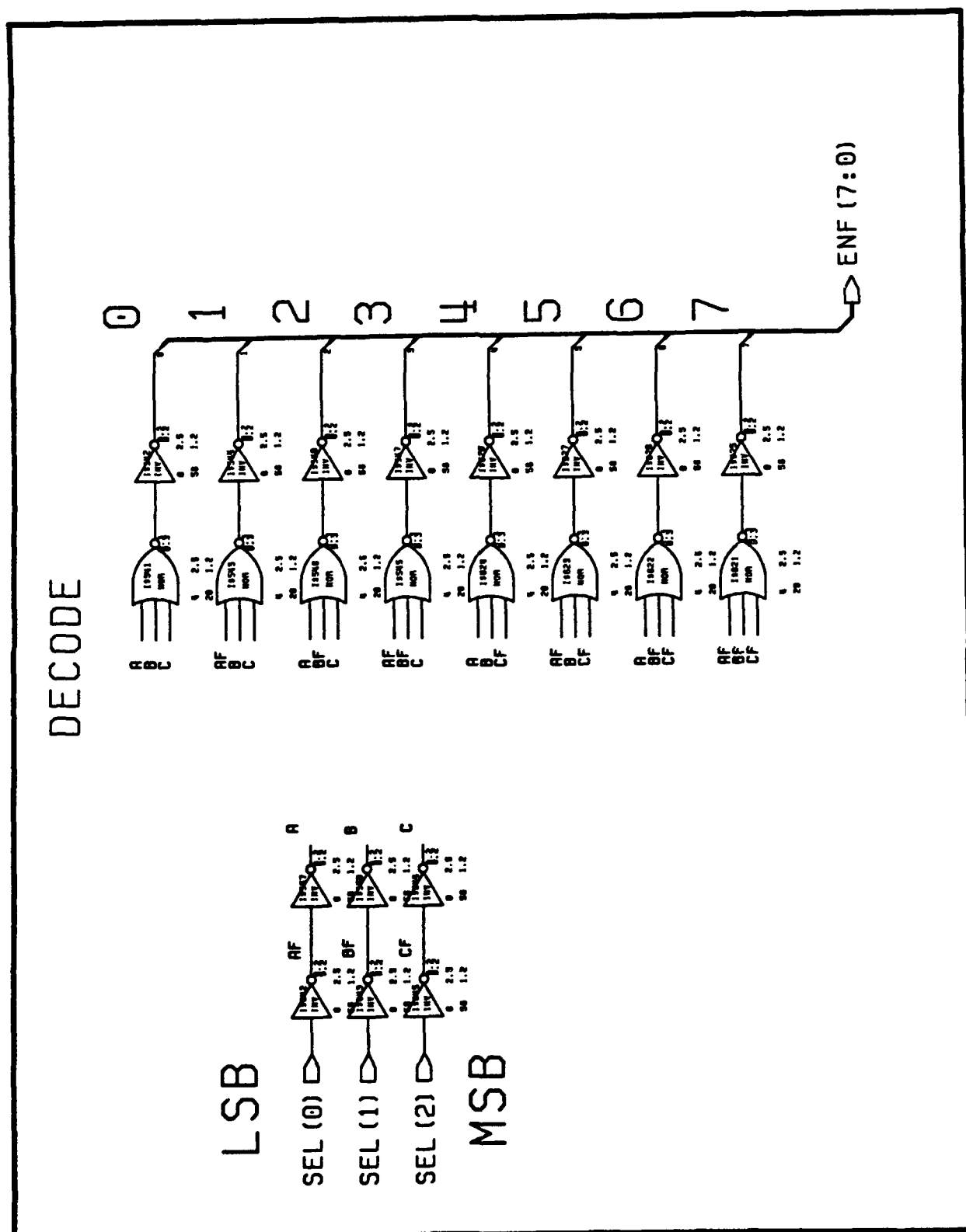


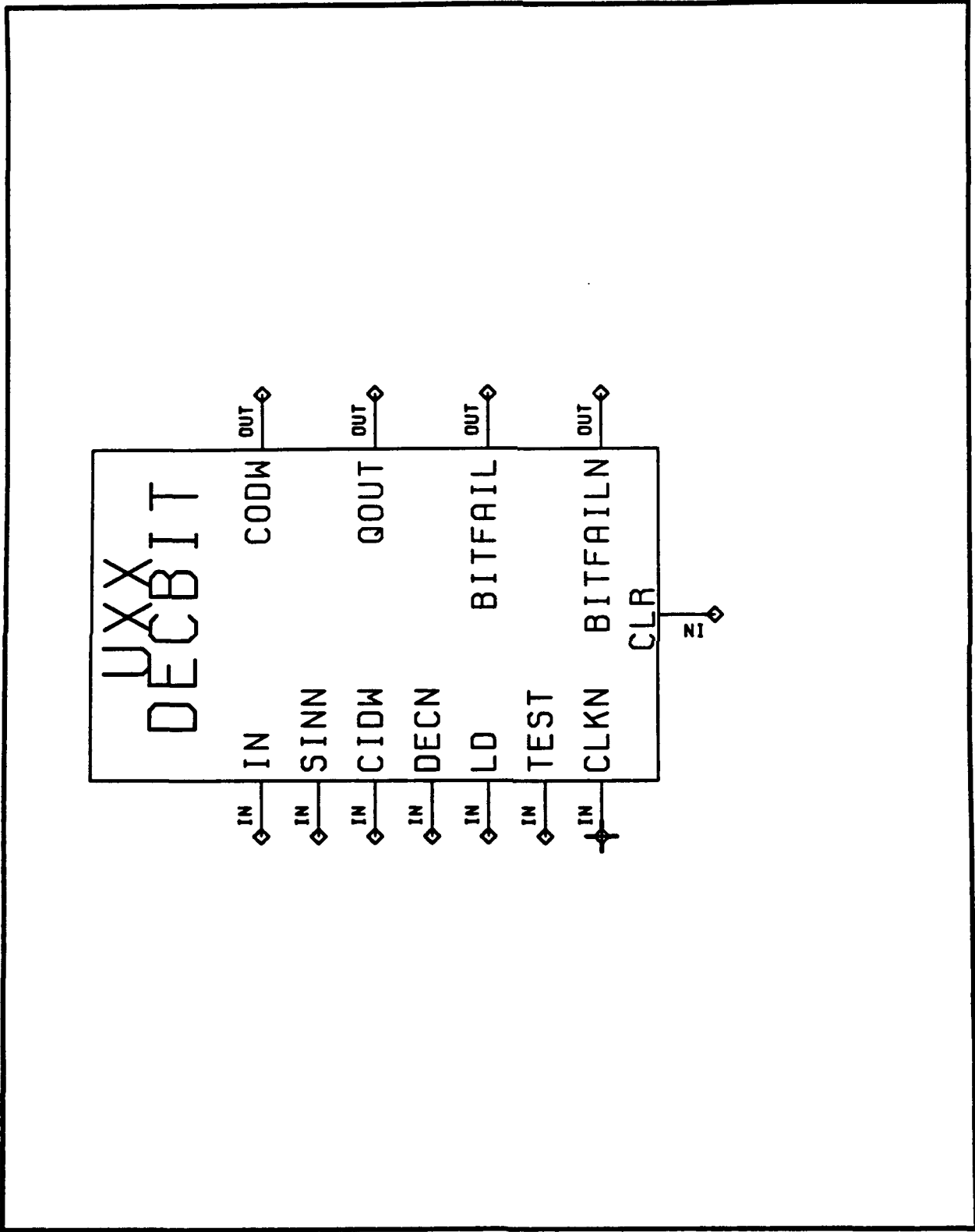




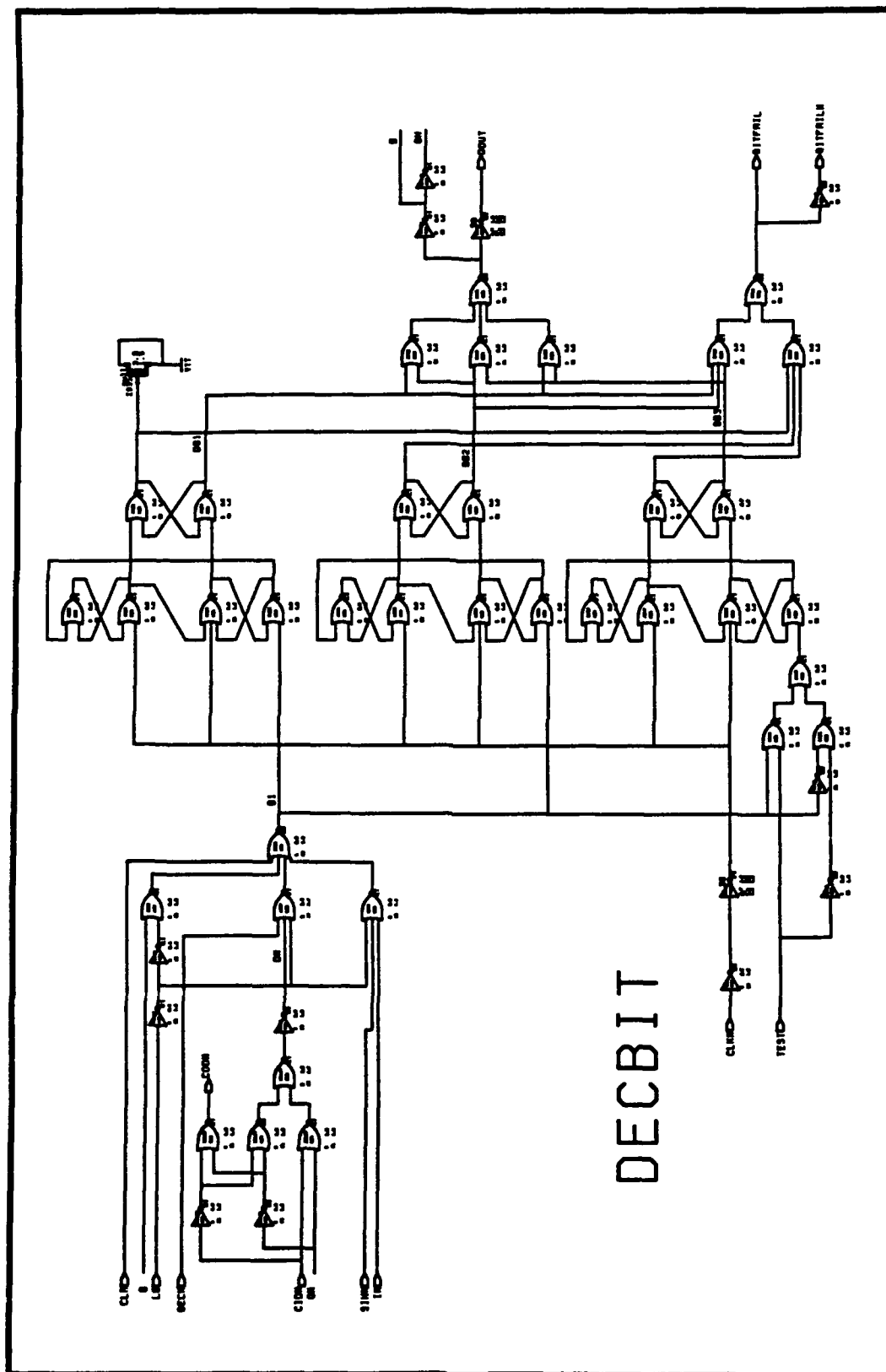


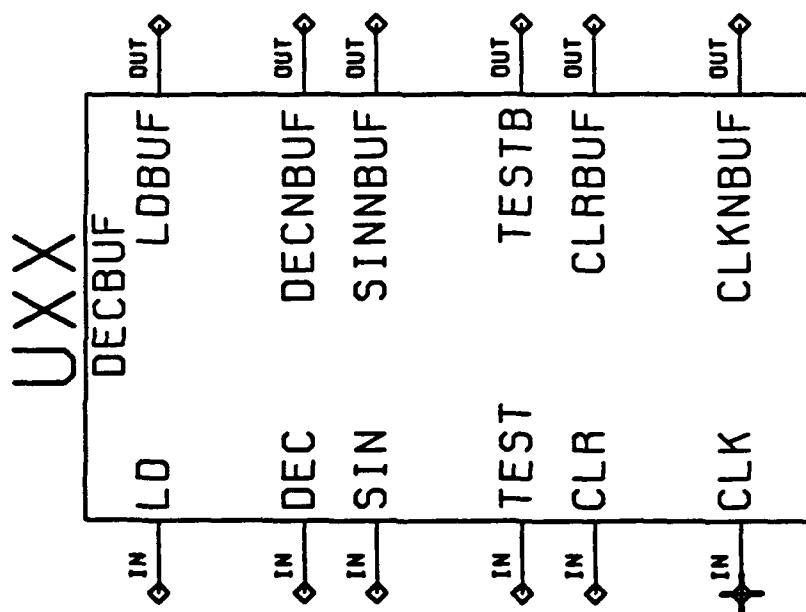


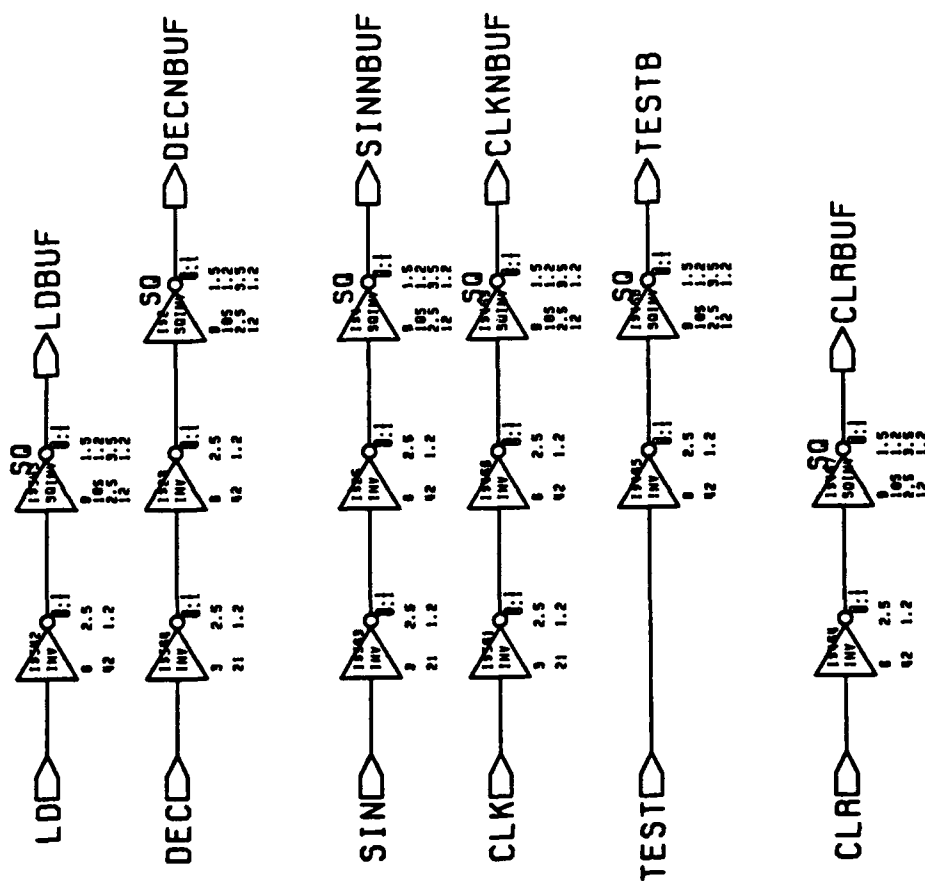


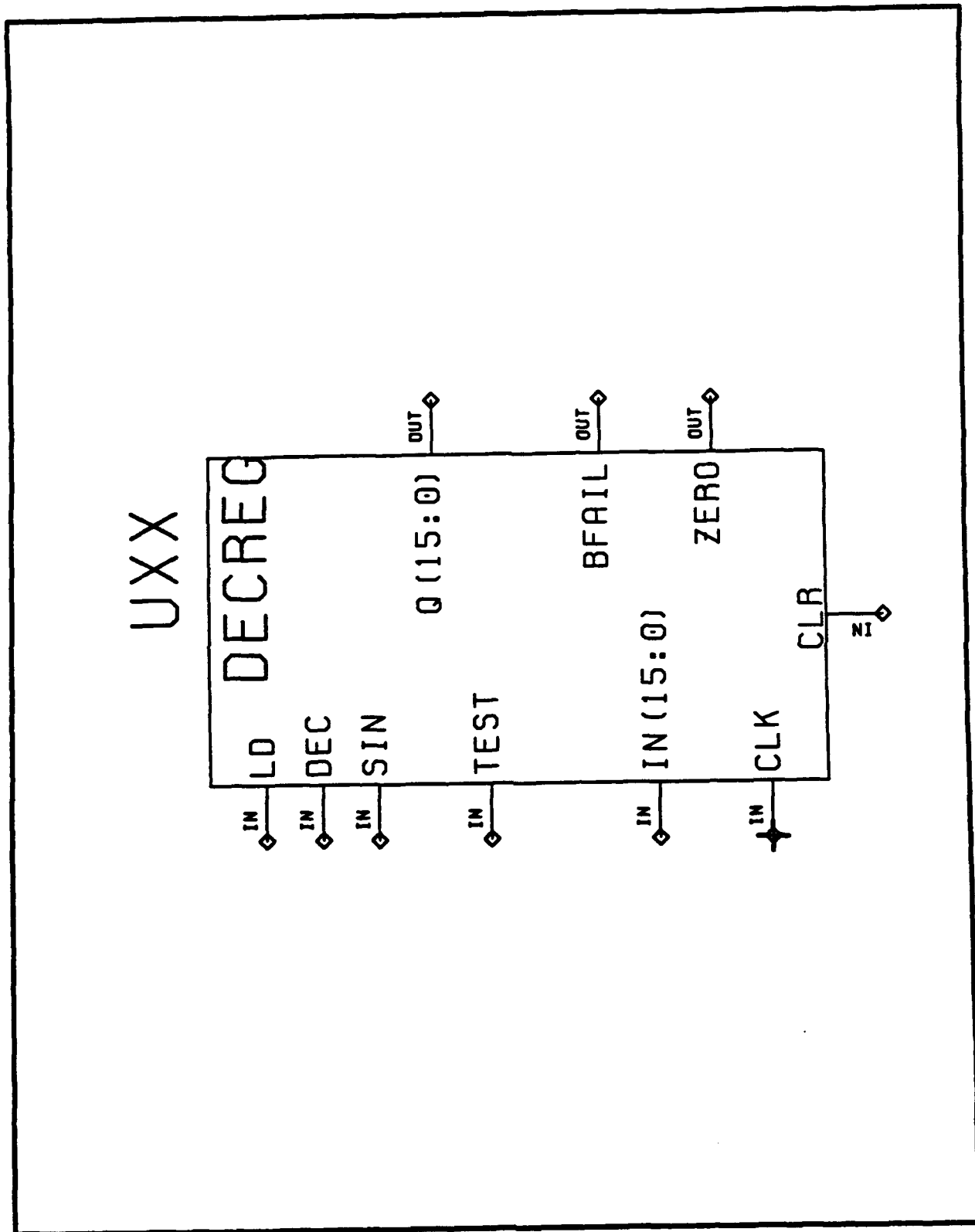




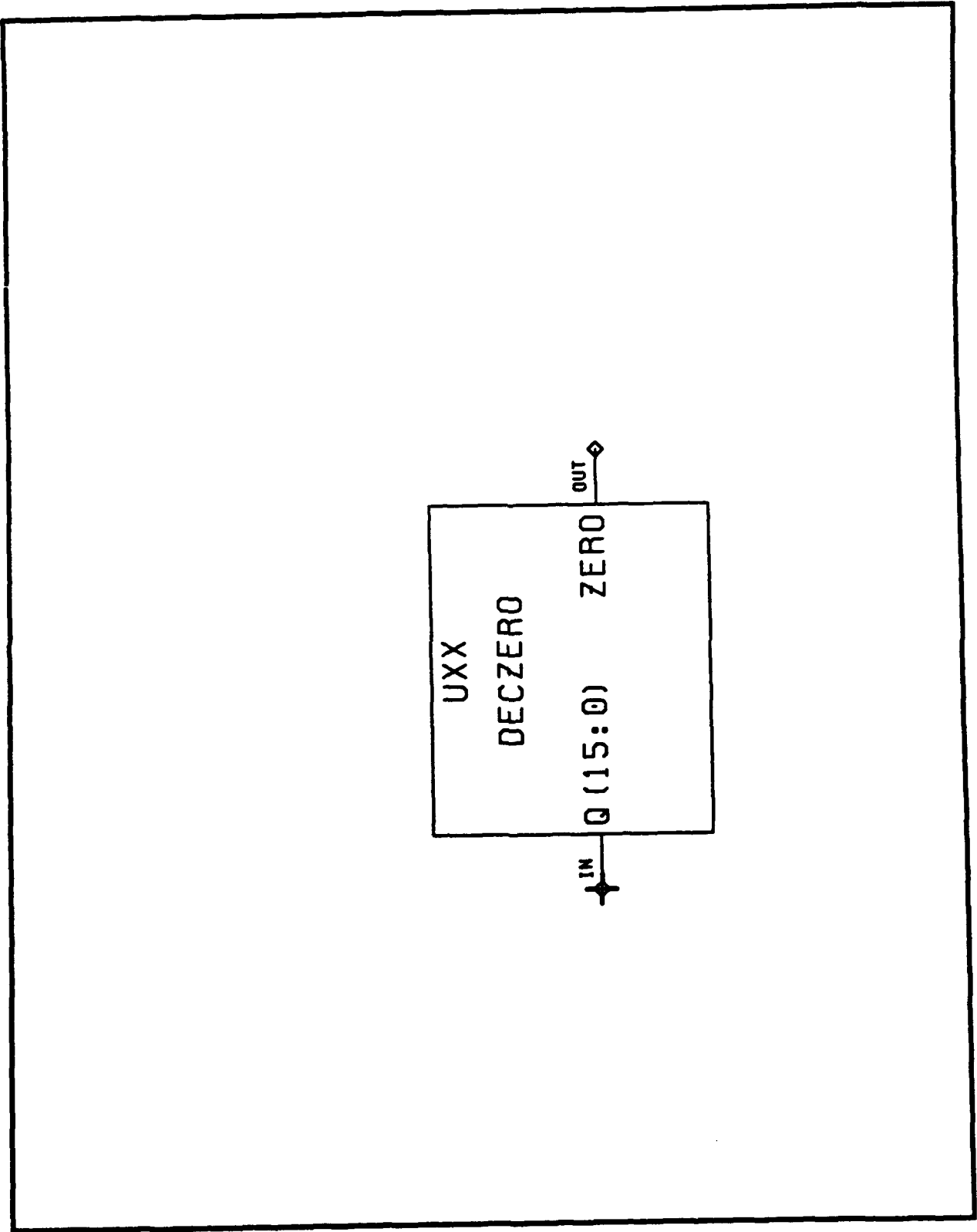


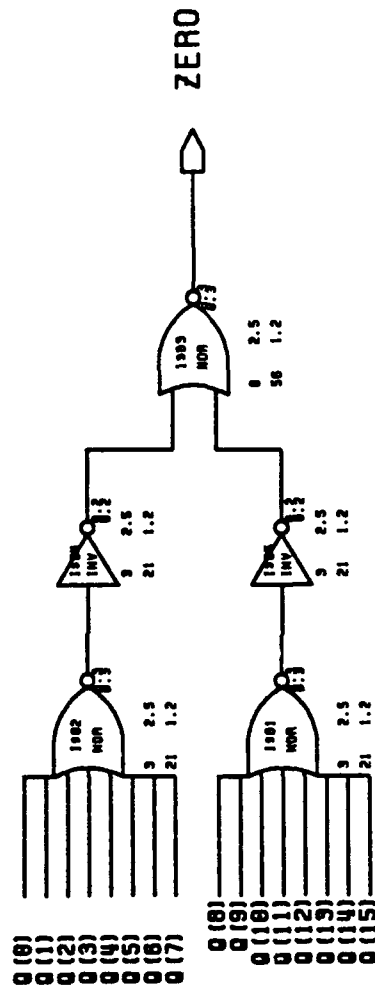












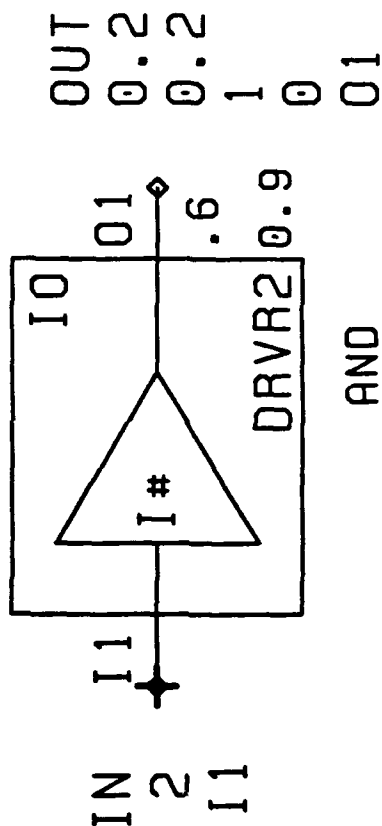
# VITESSE GAAS CELL LIBRARY

Version 0.8

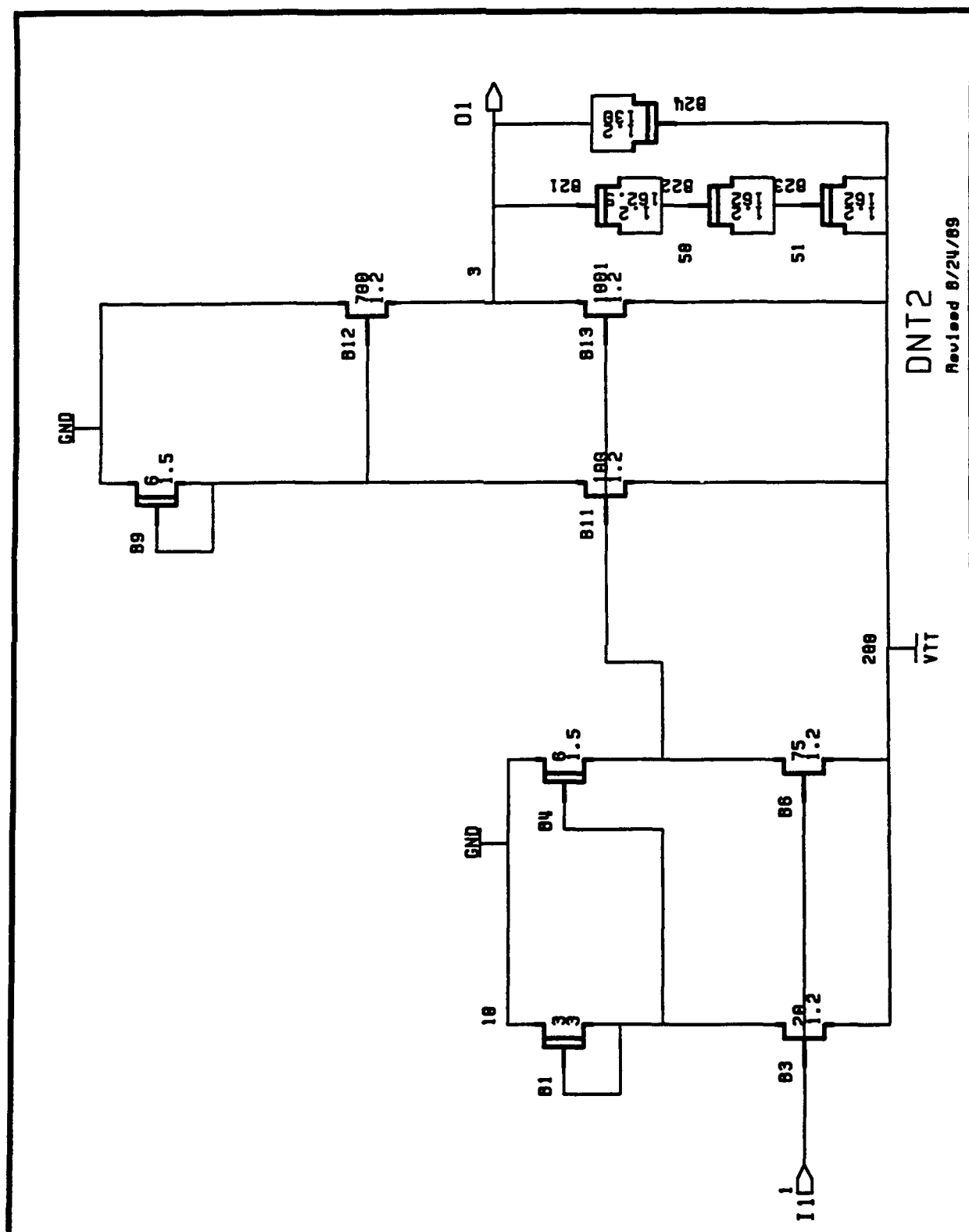
NAME:

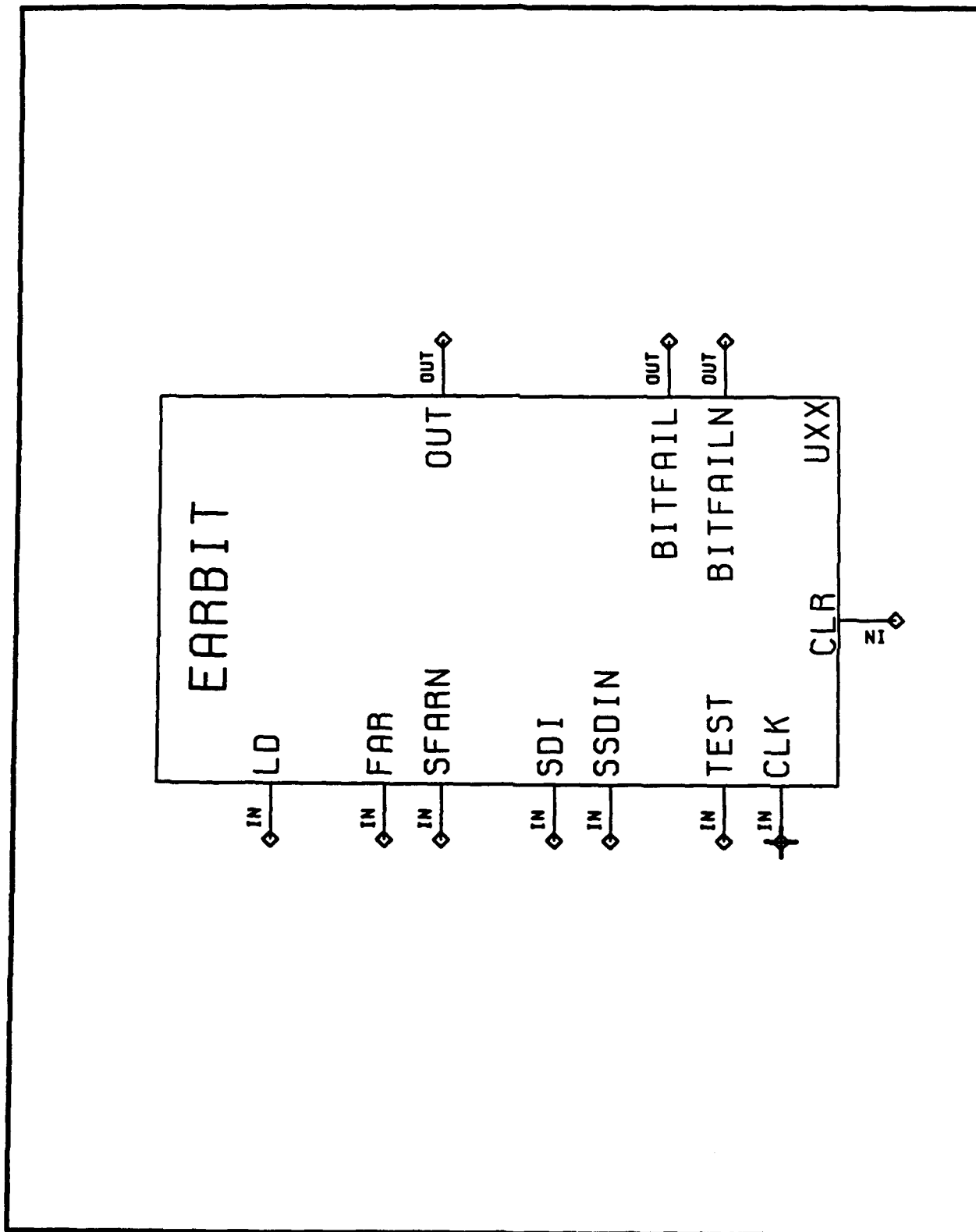
DRV2

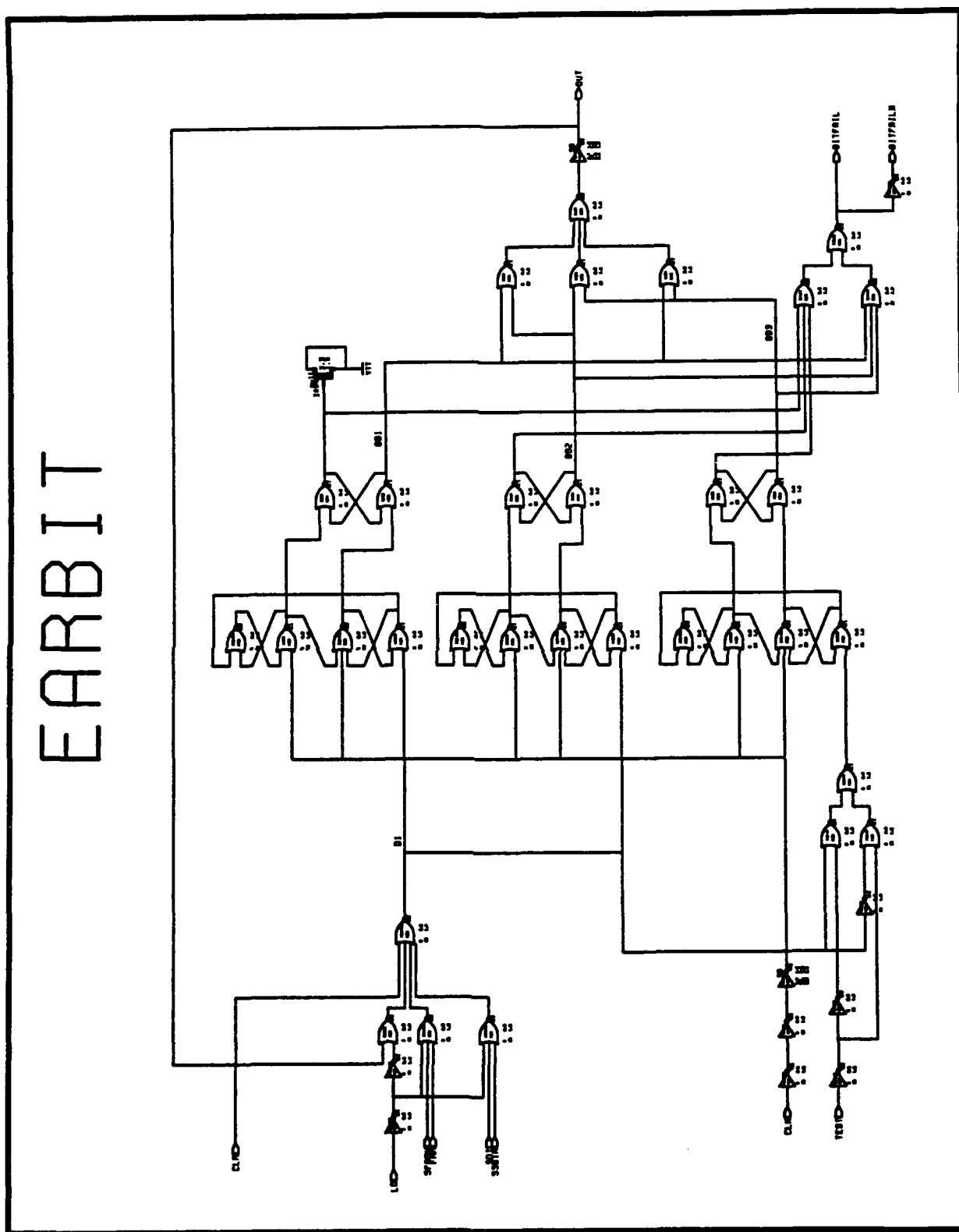
DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD

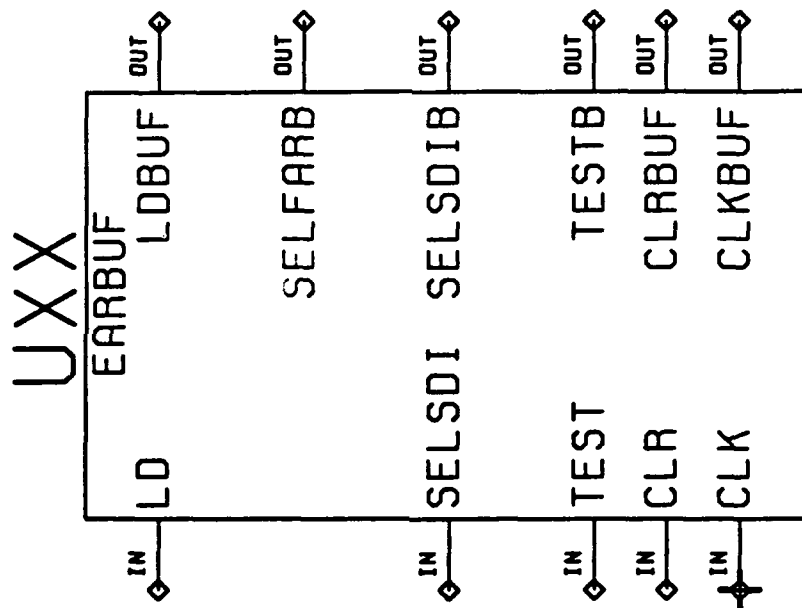


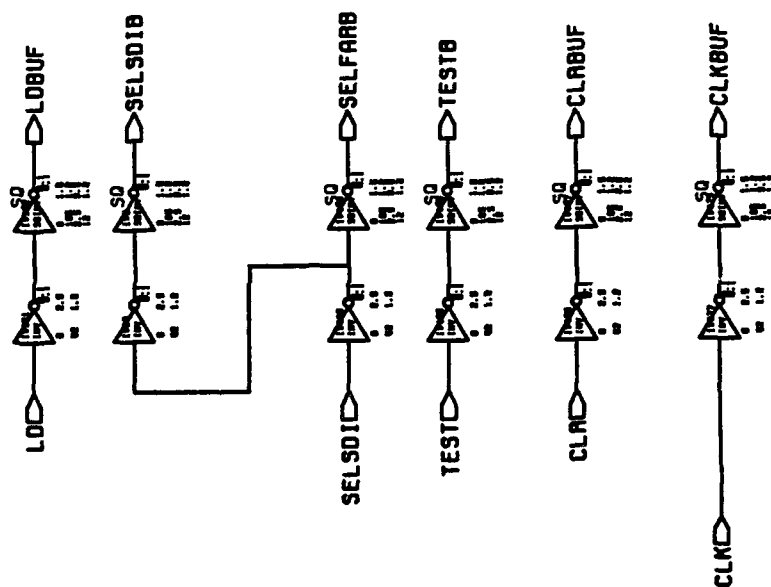


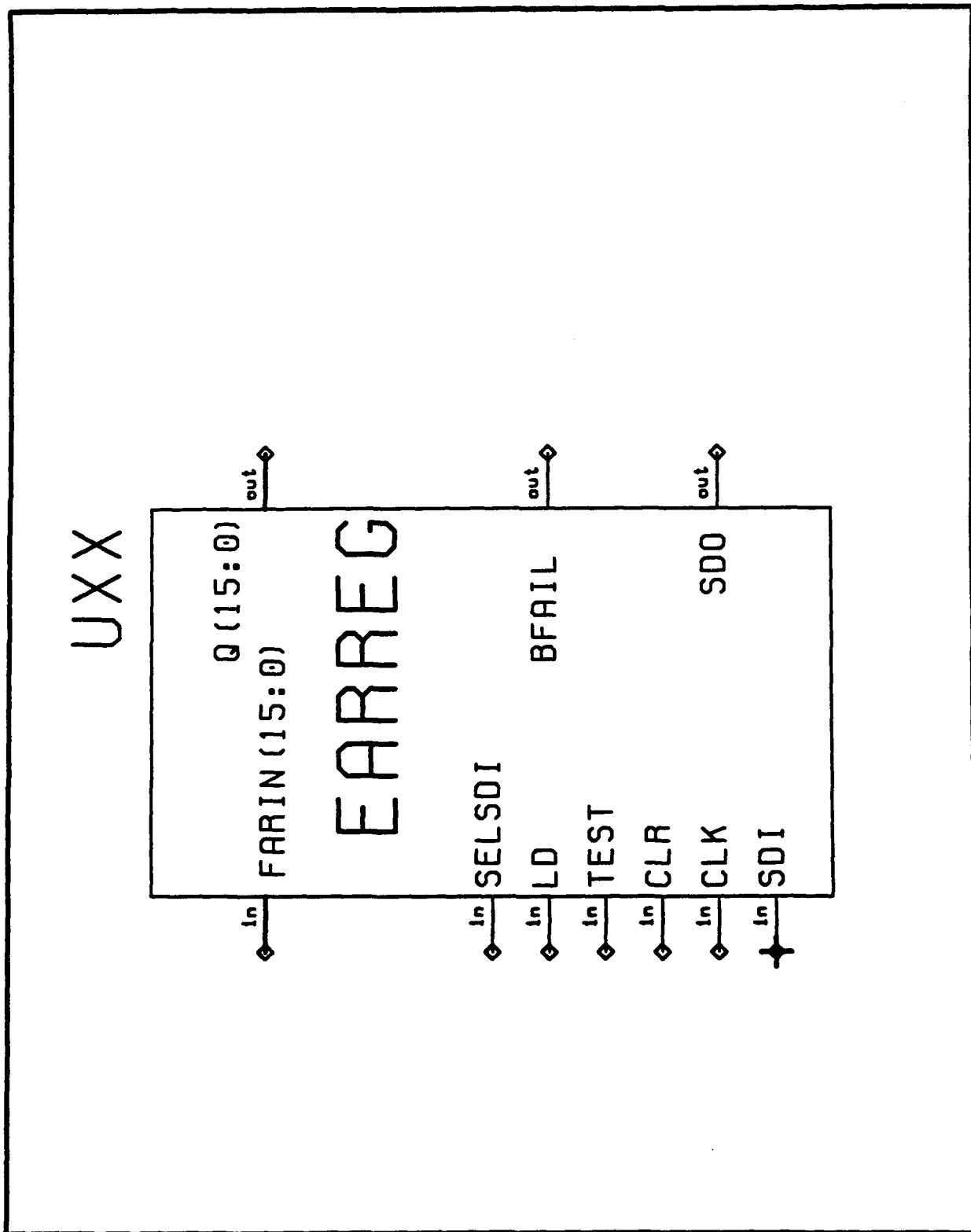


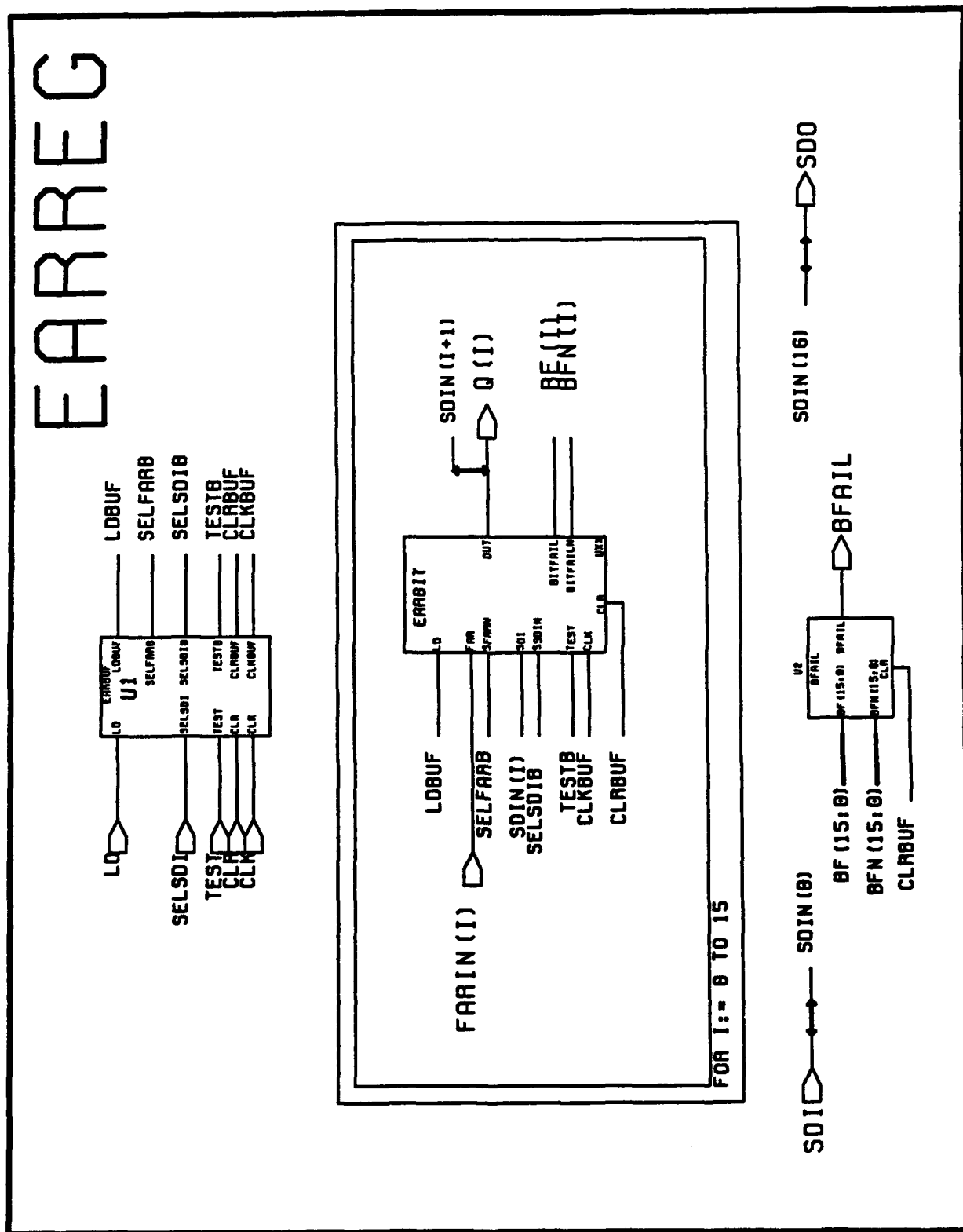


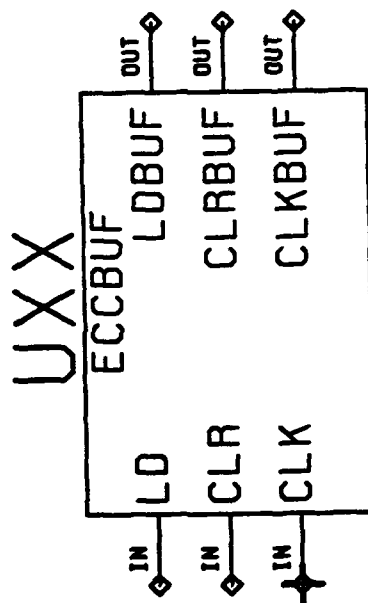




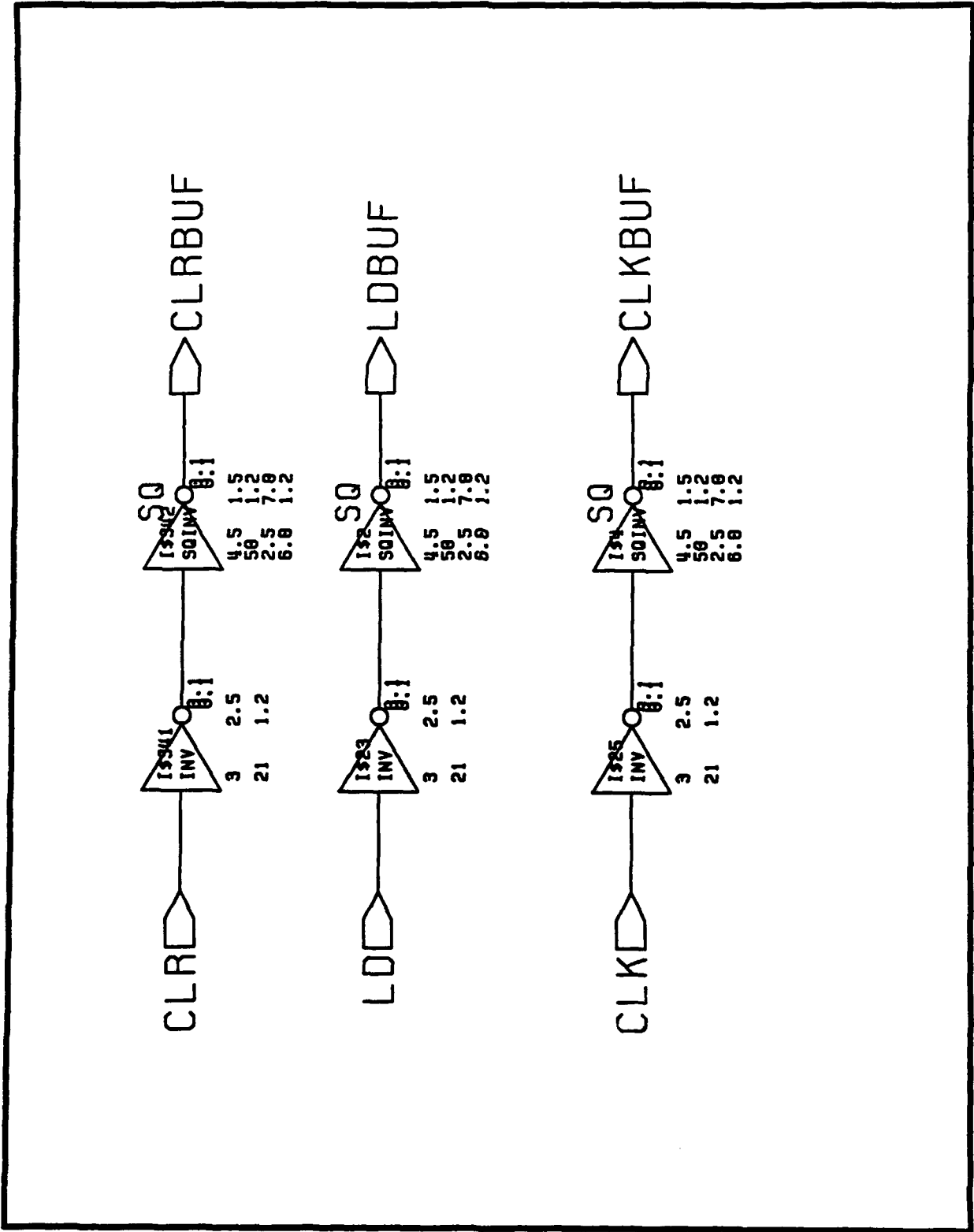


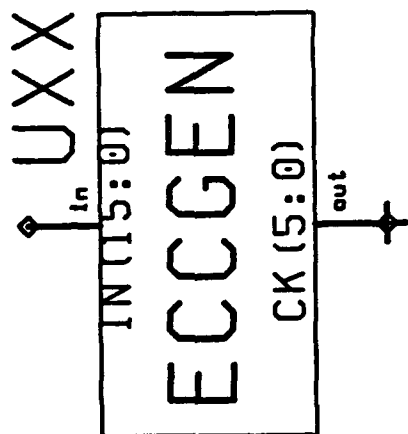




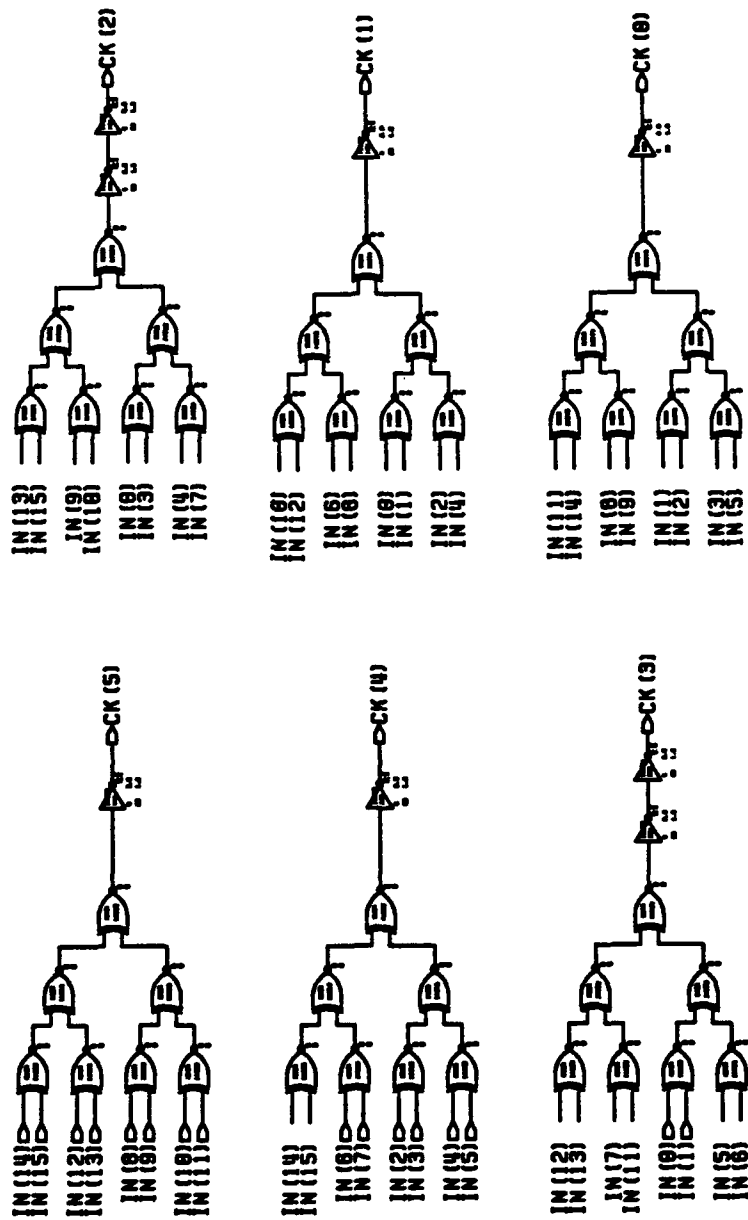


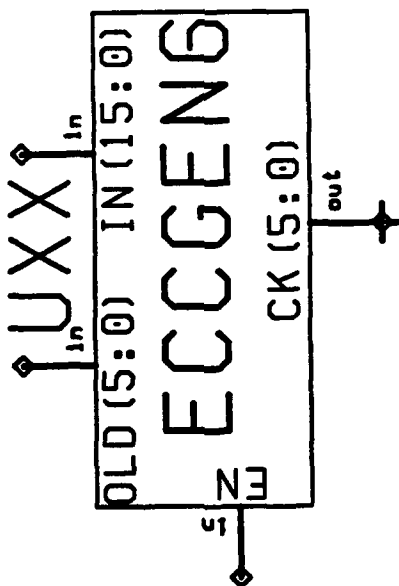




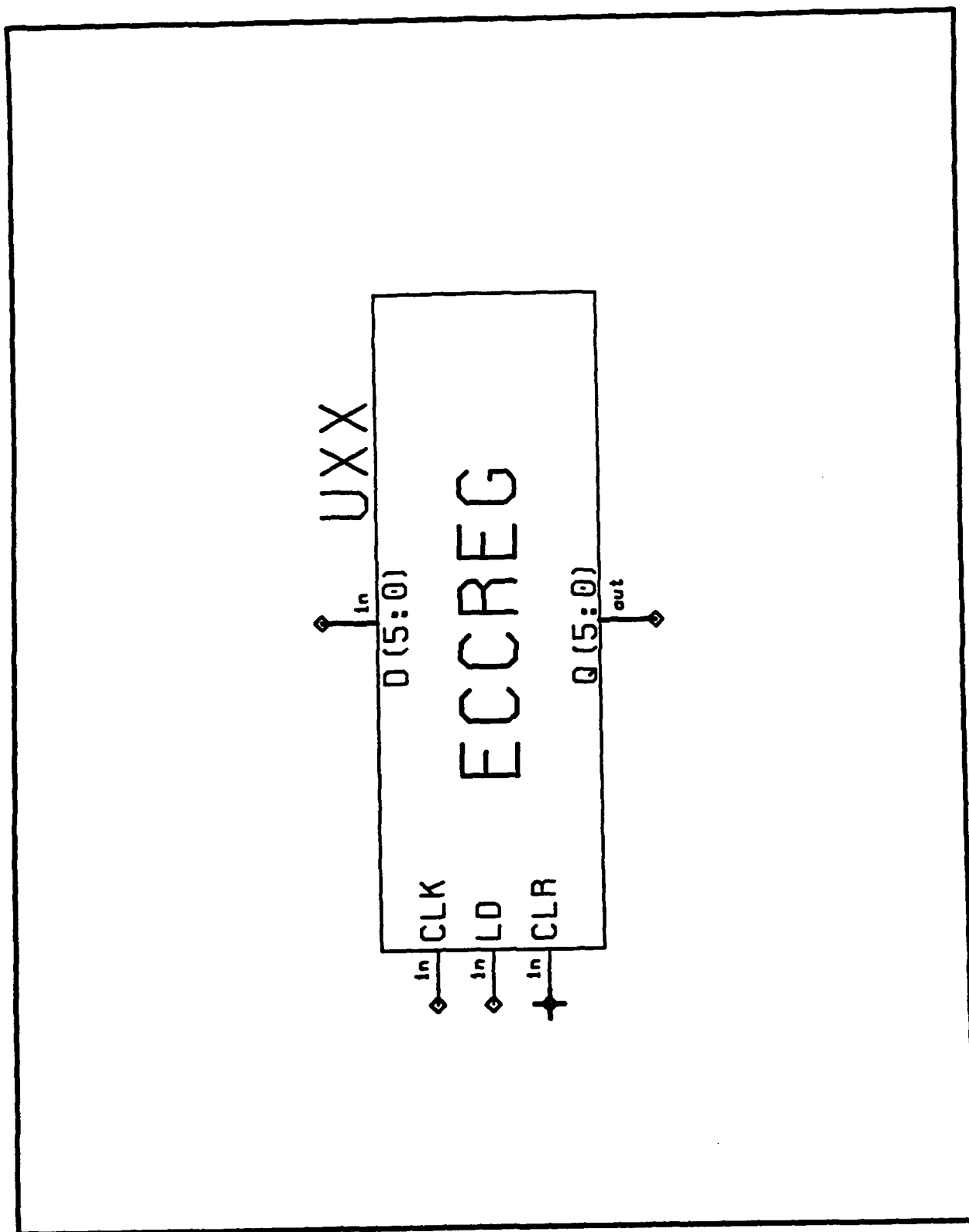


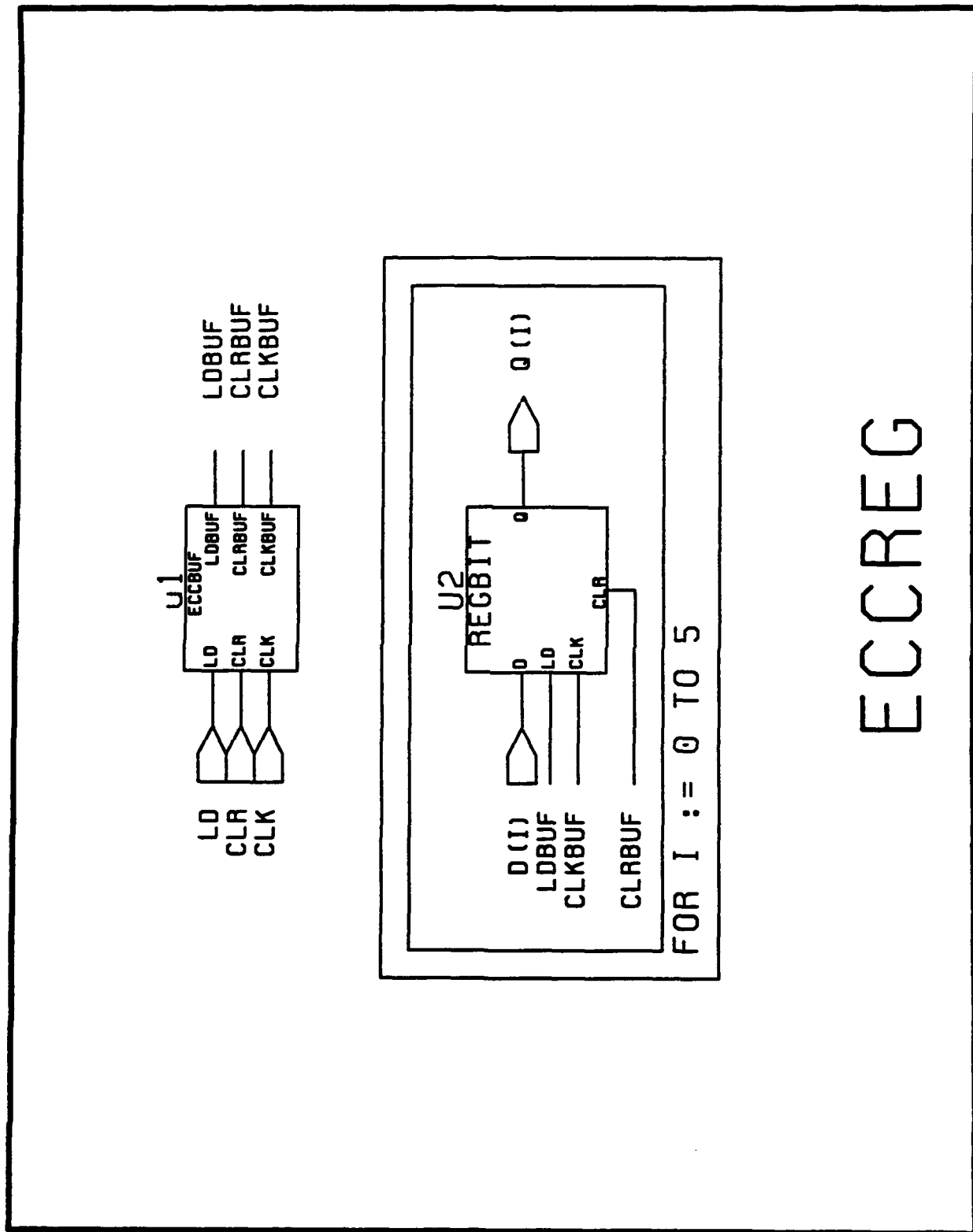
ECCGEN6: ECC CHECK BIT GENERATION









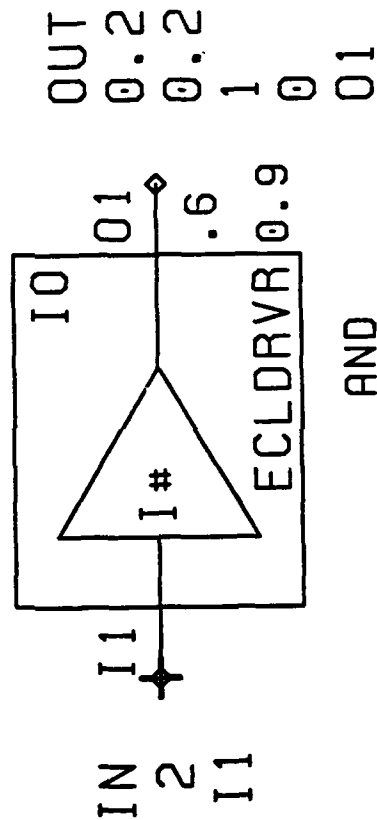


ECCREG

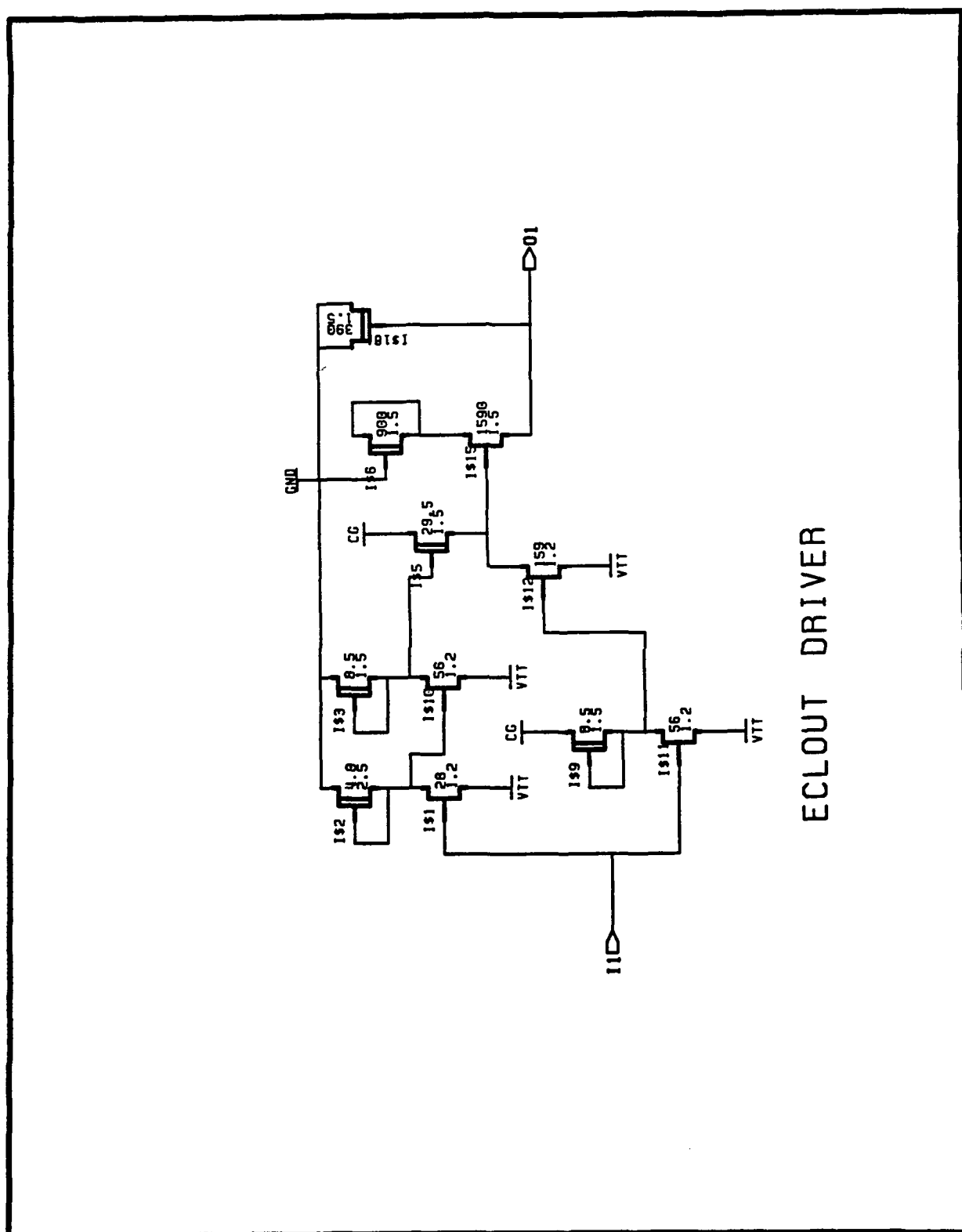
# VITESSE GAAS CELL LIBRARY

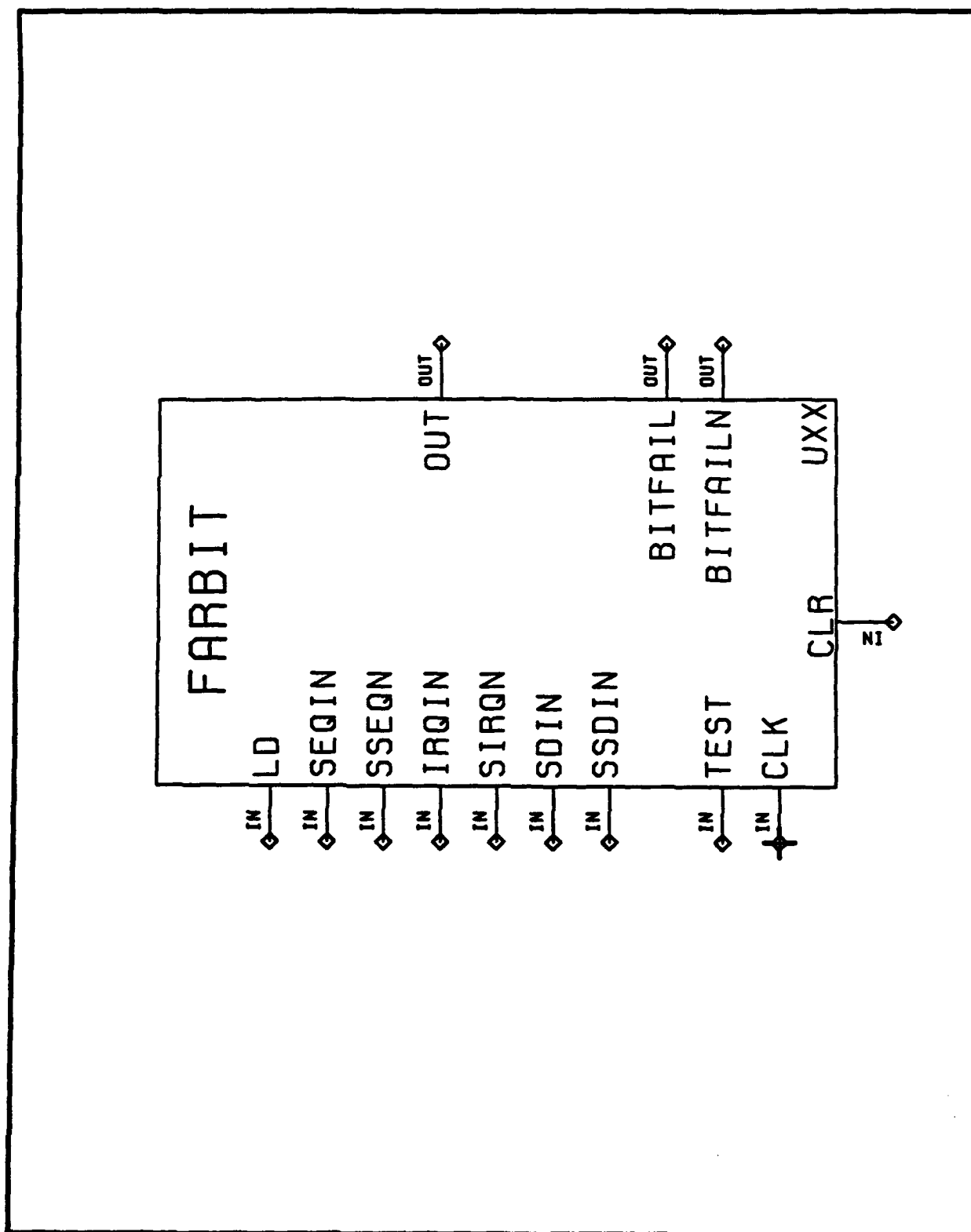
Version 0.8

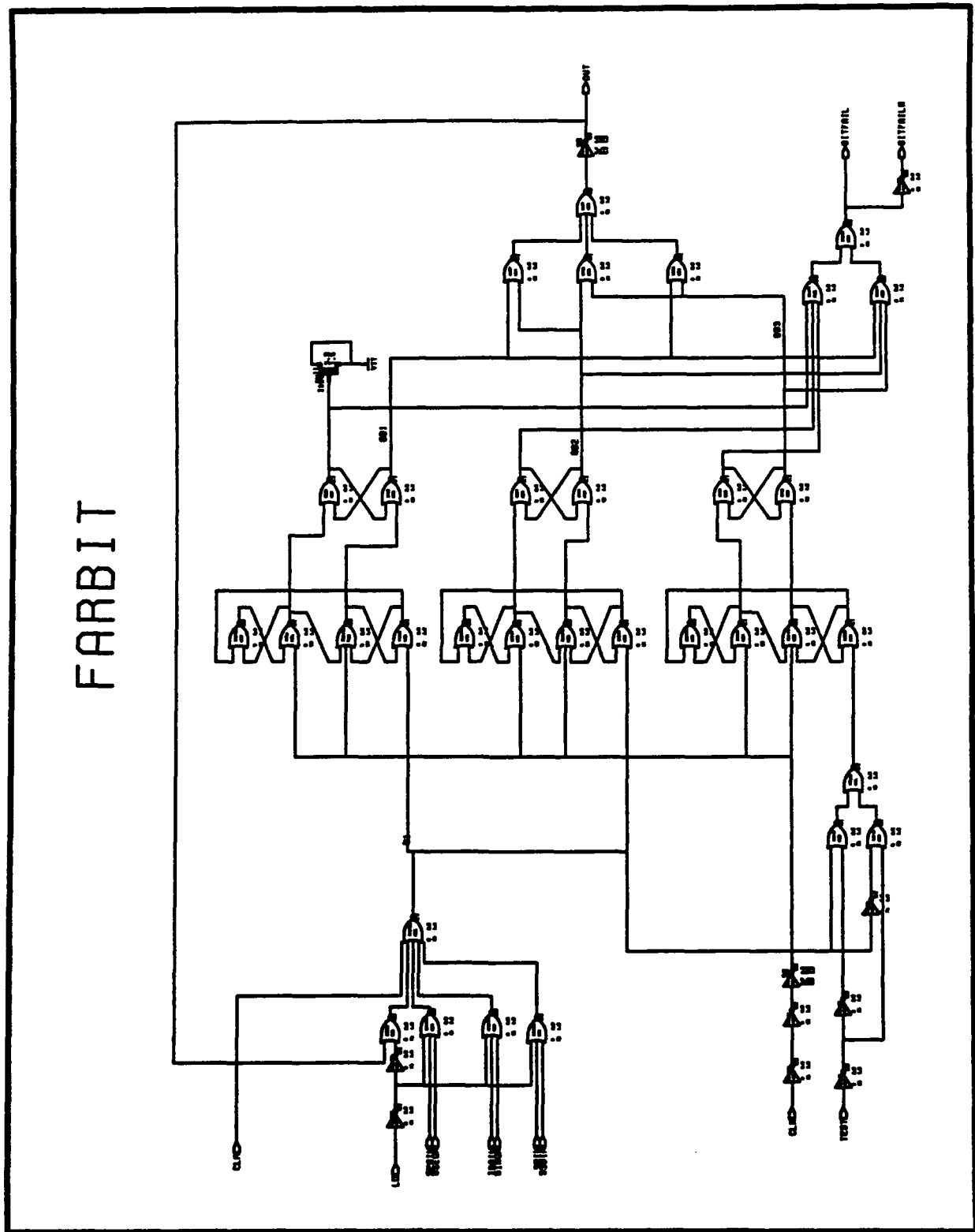
NAME: ECLOUT  
DESCRIPTION: ECL OUTPUT DRVR FOR DMC

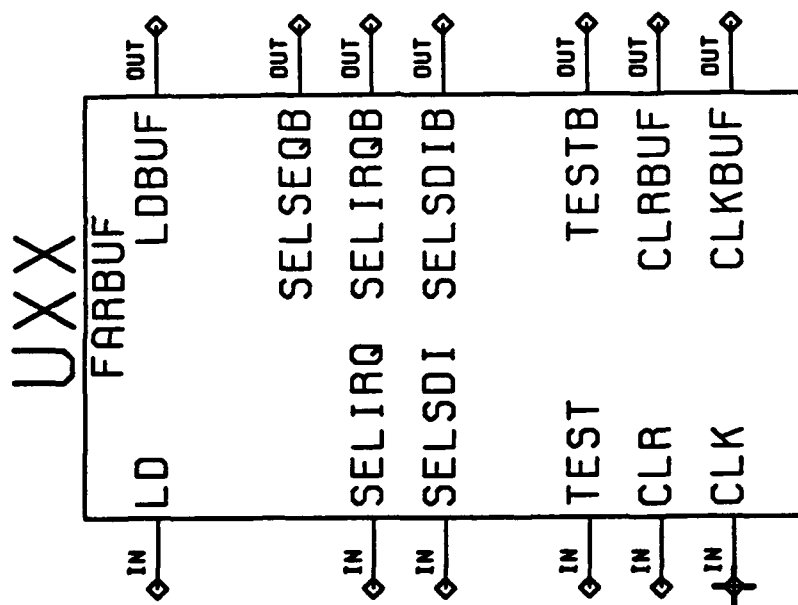


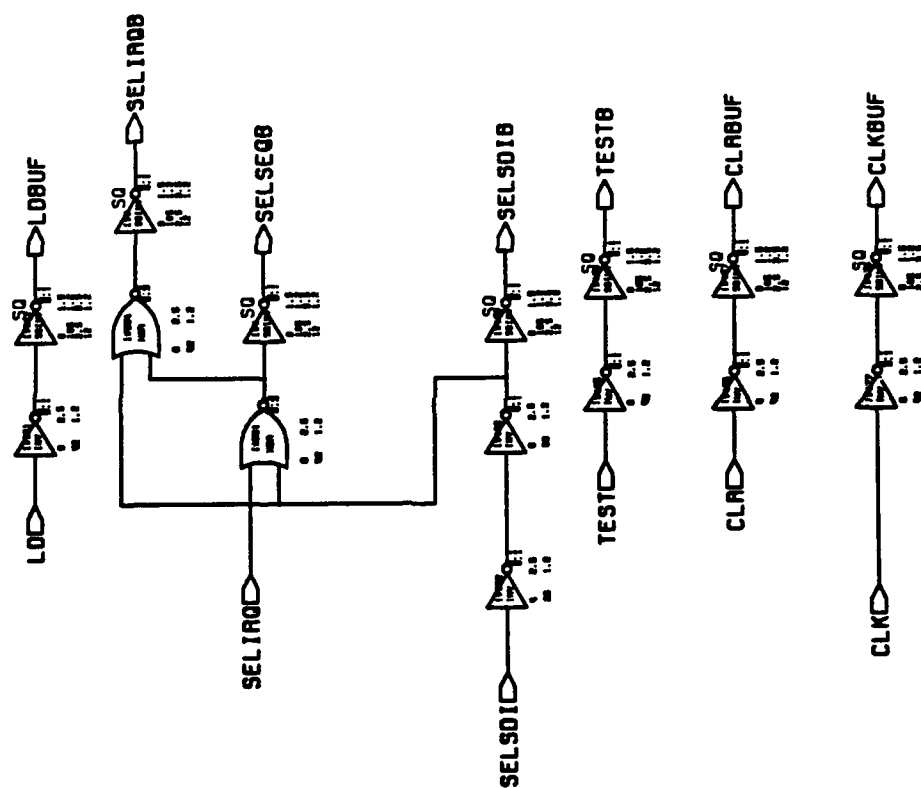


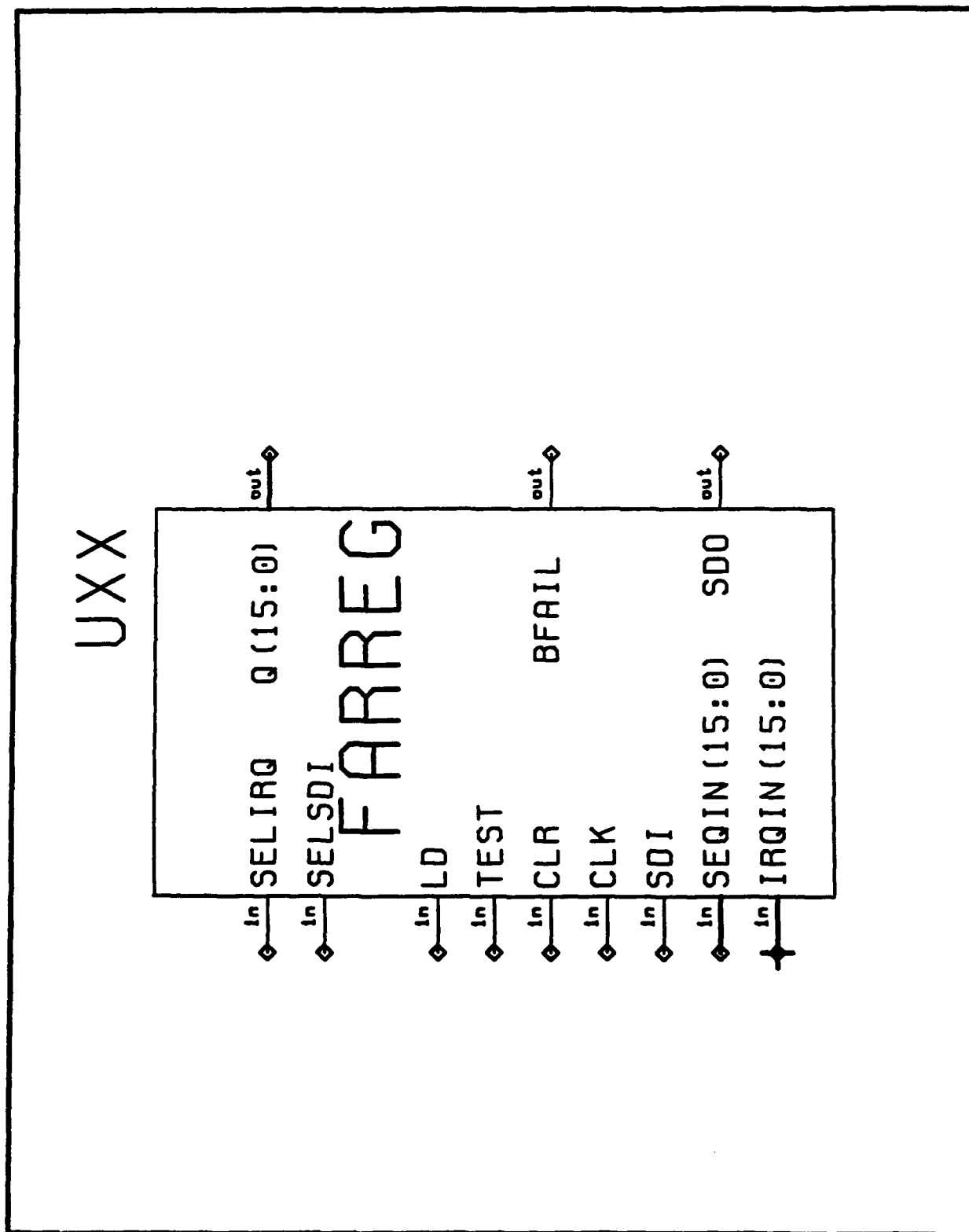




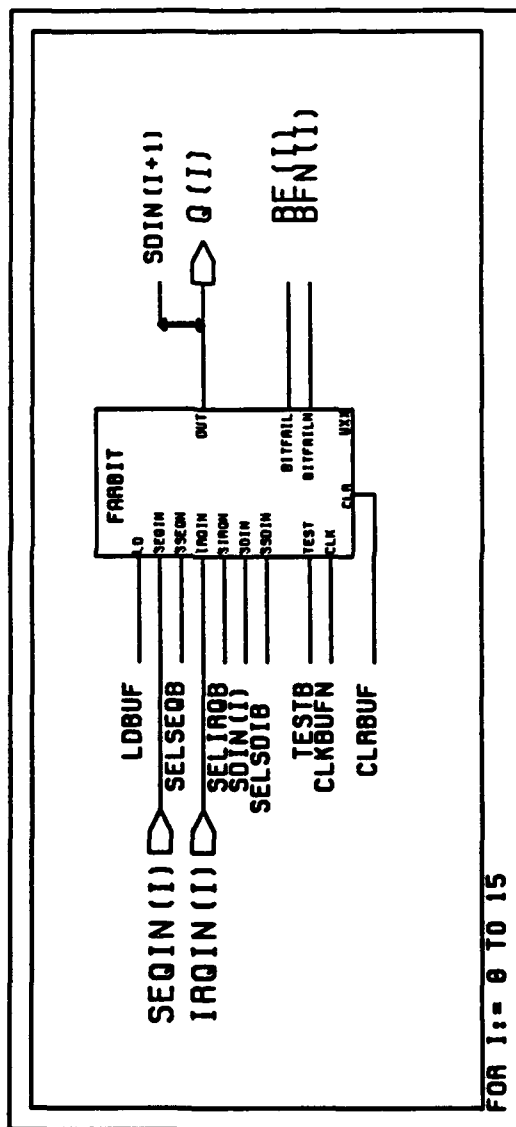
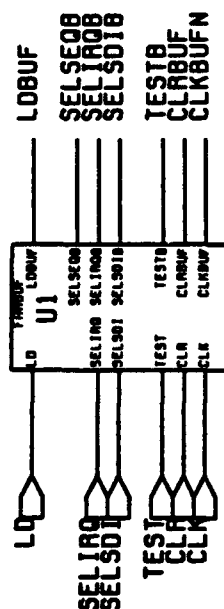




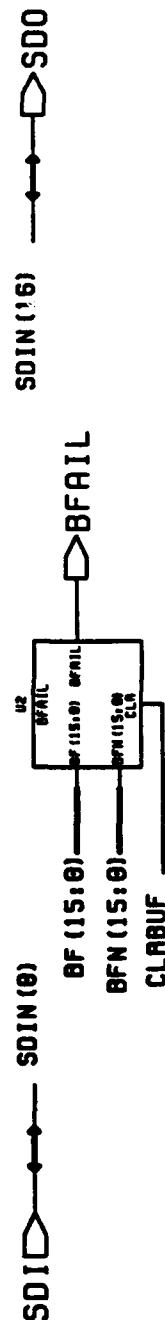


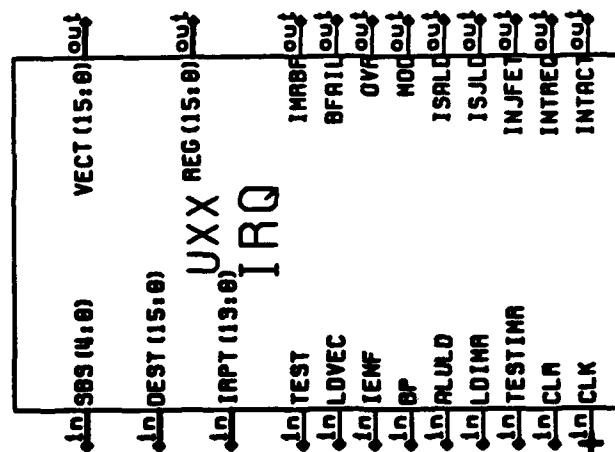


# FARREG

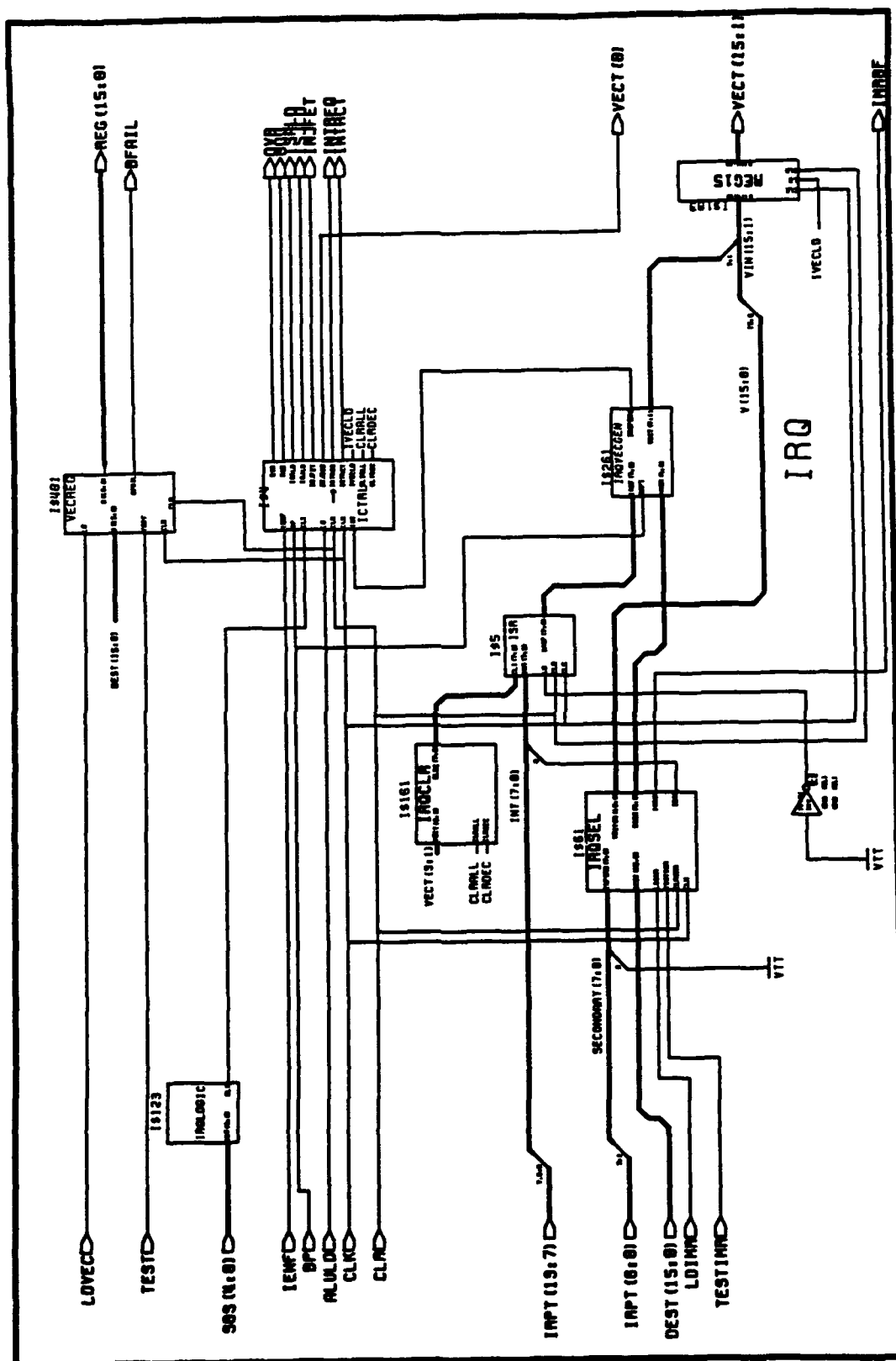


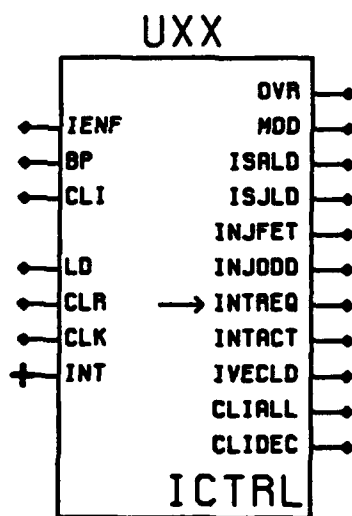
FOR I := 0 TO 15

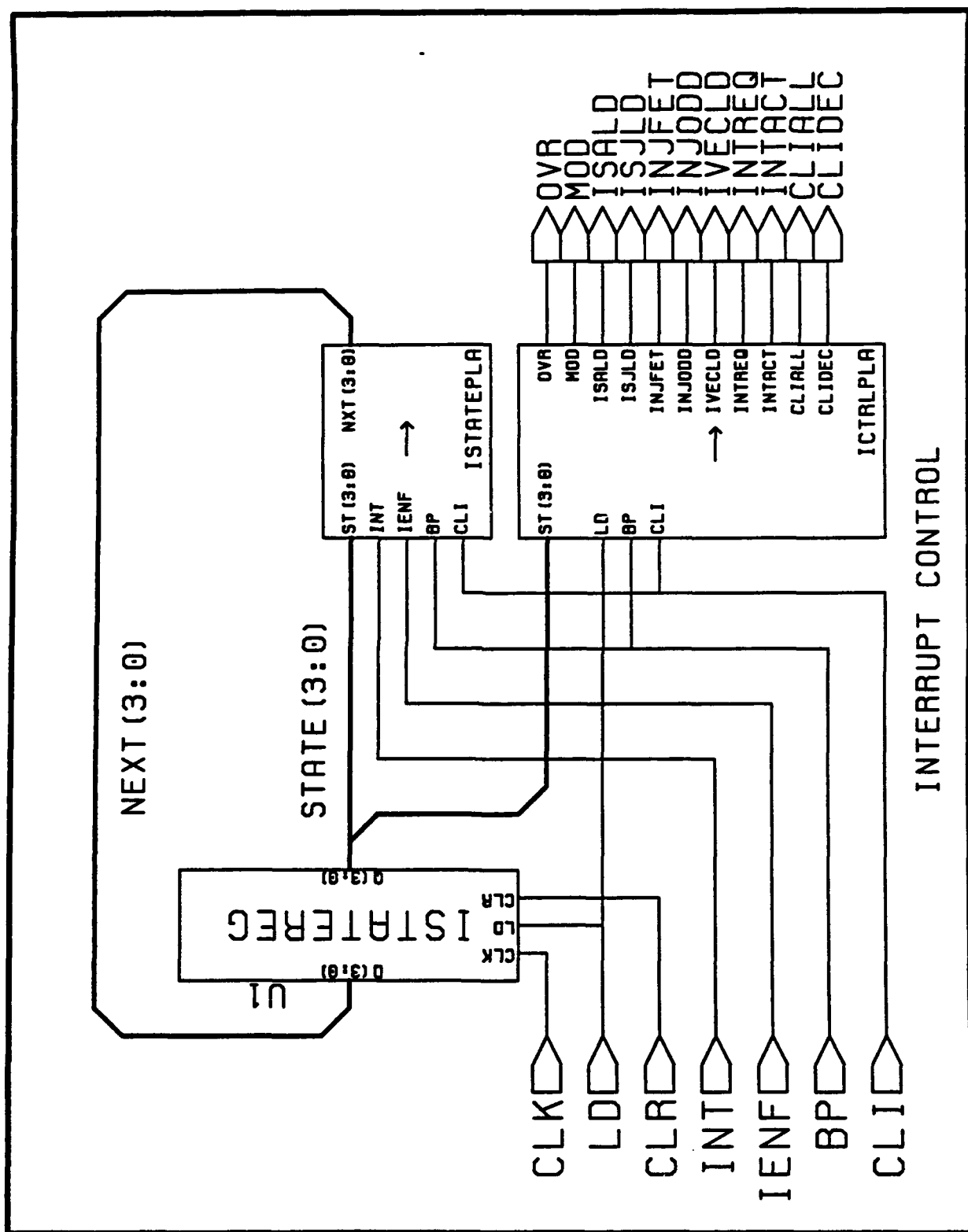


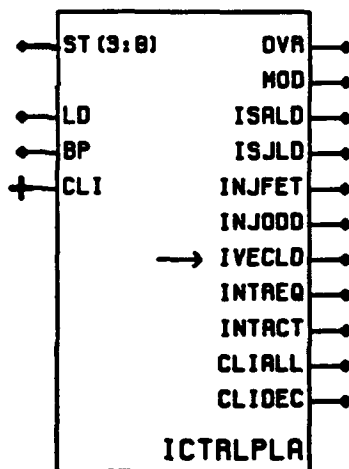


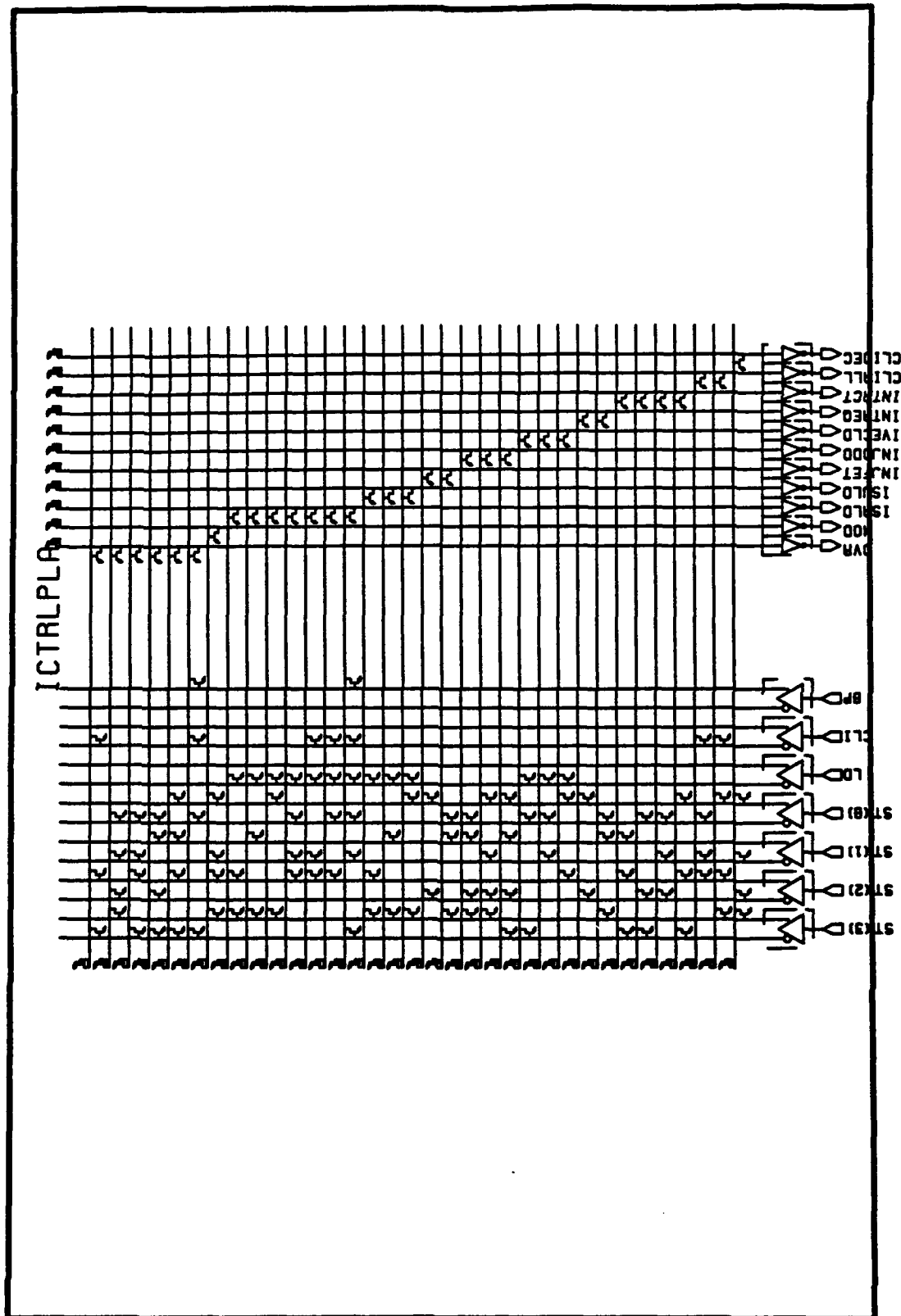


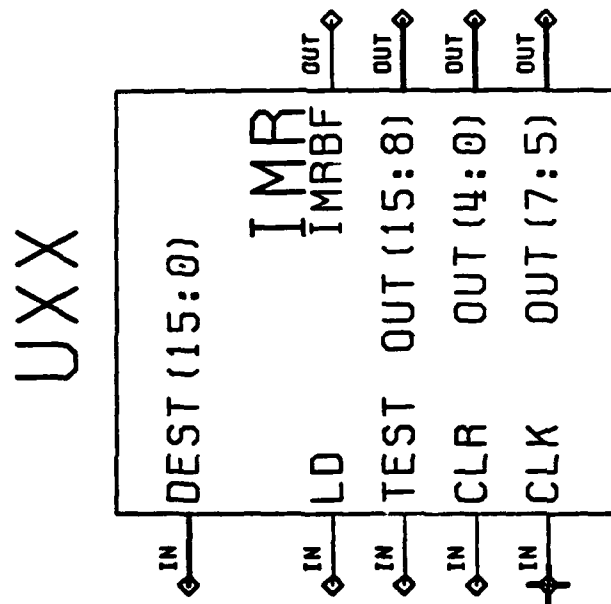


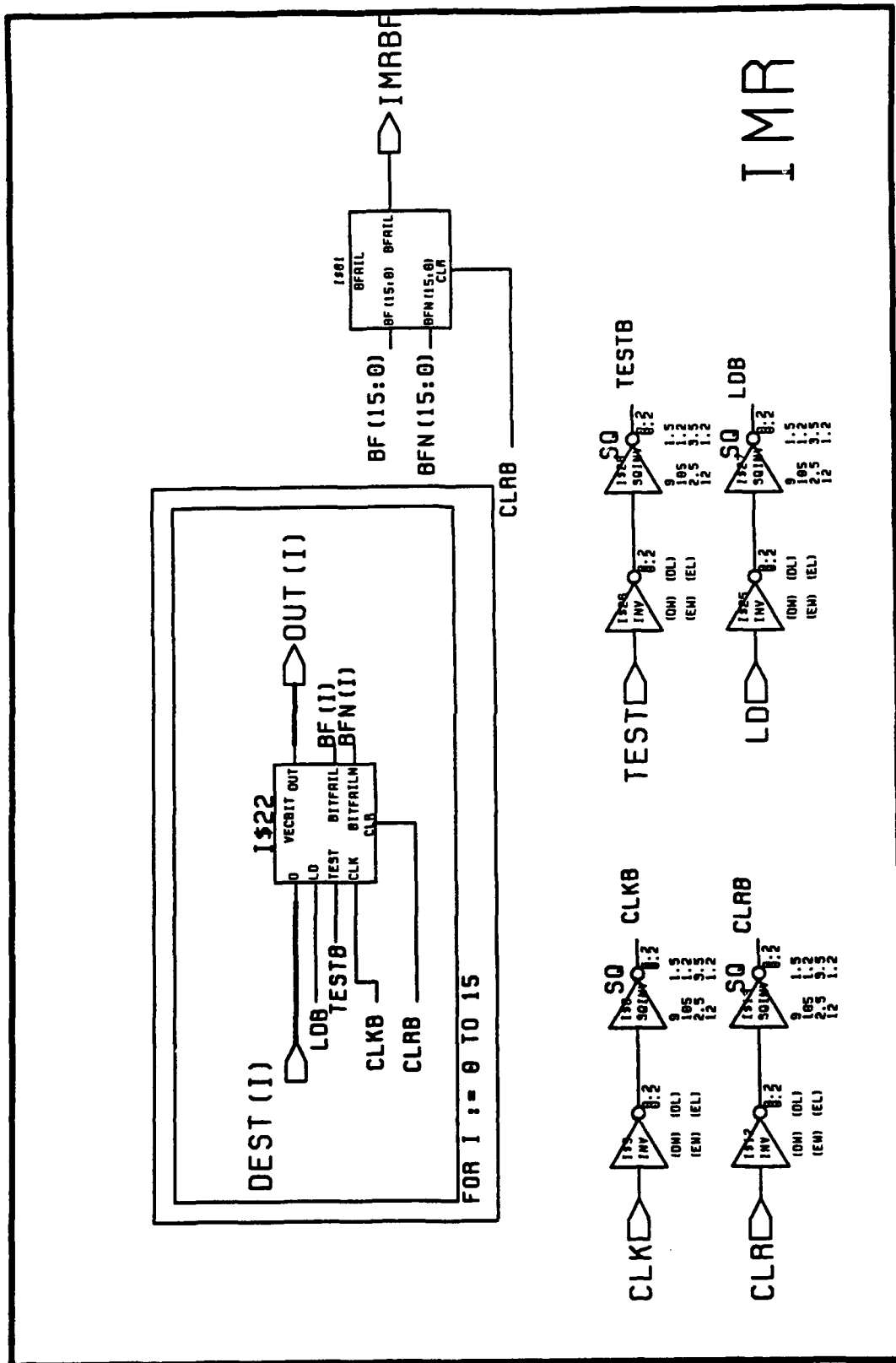


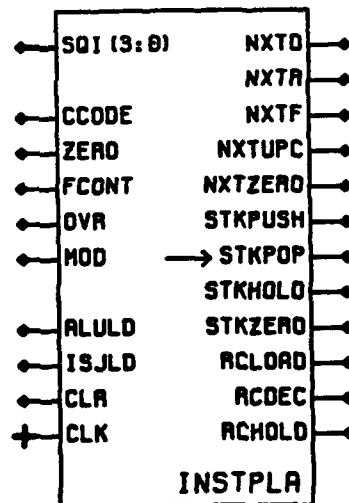




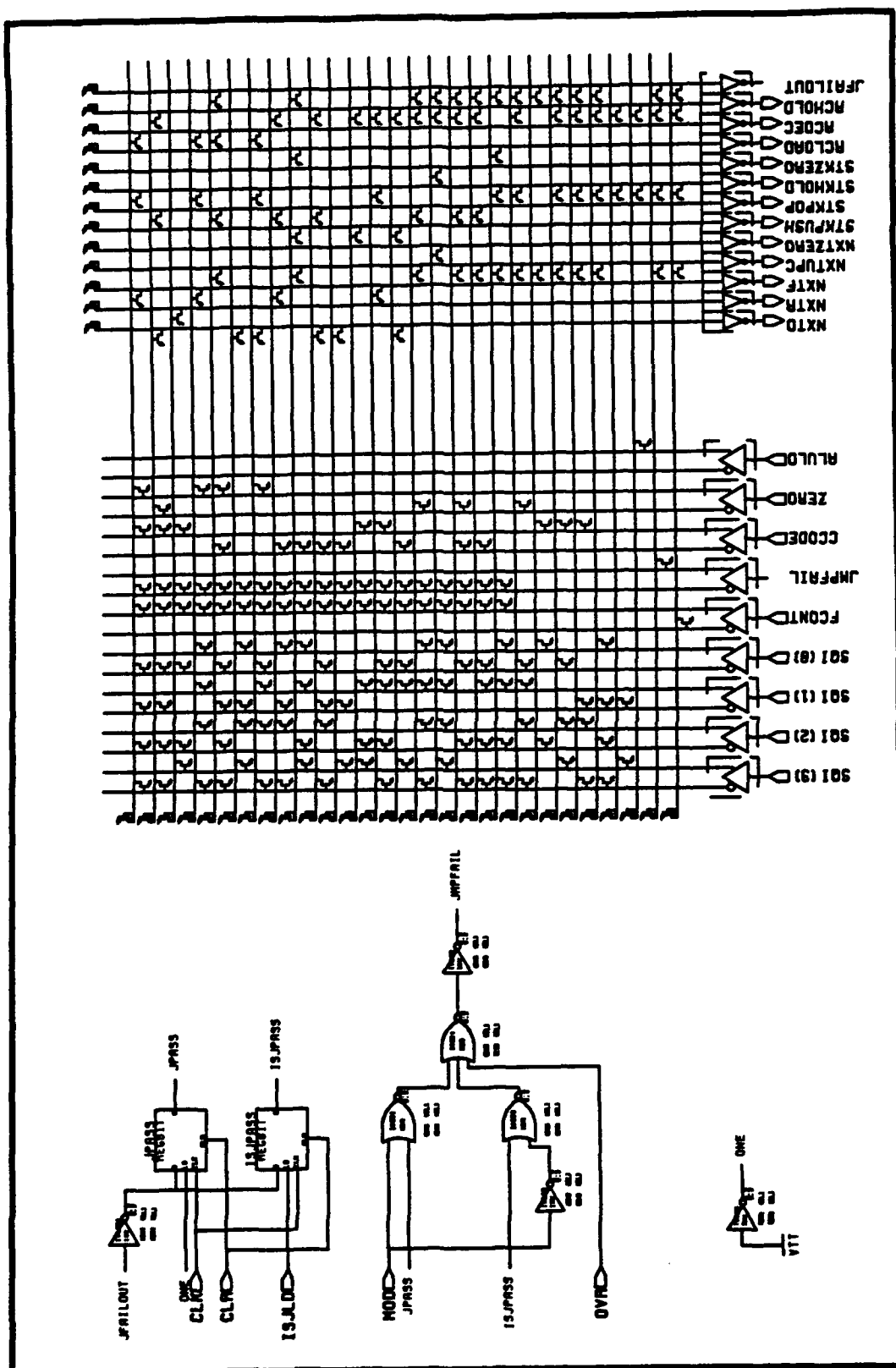


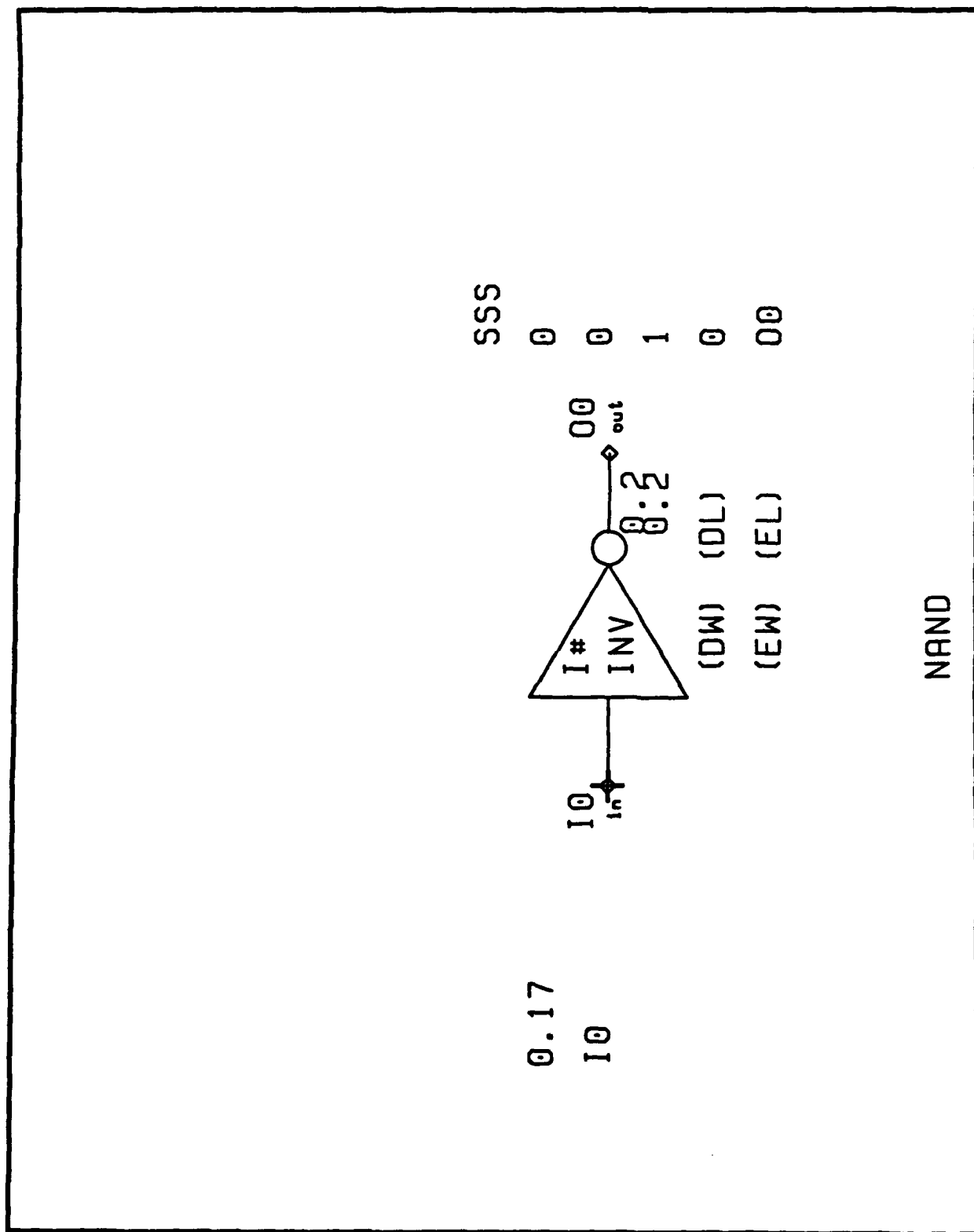


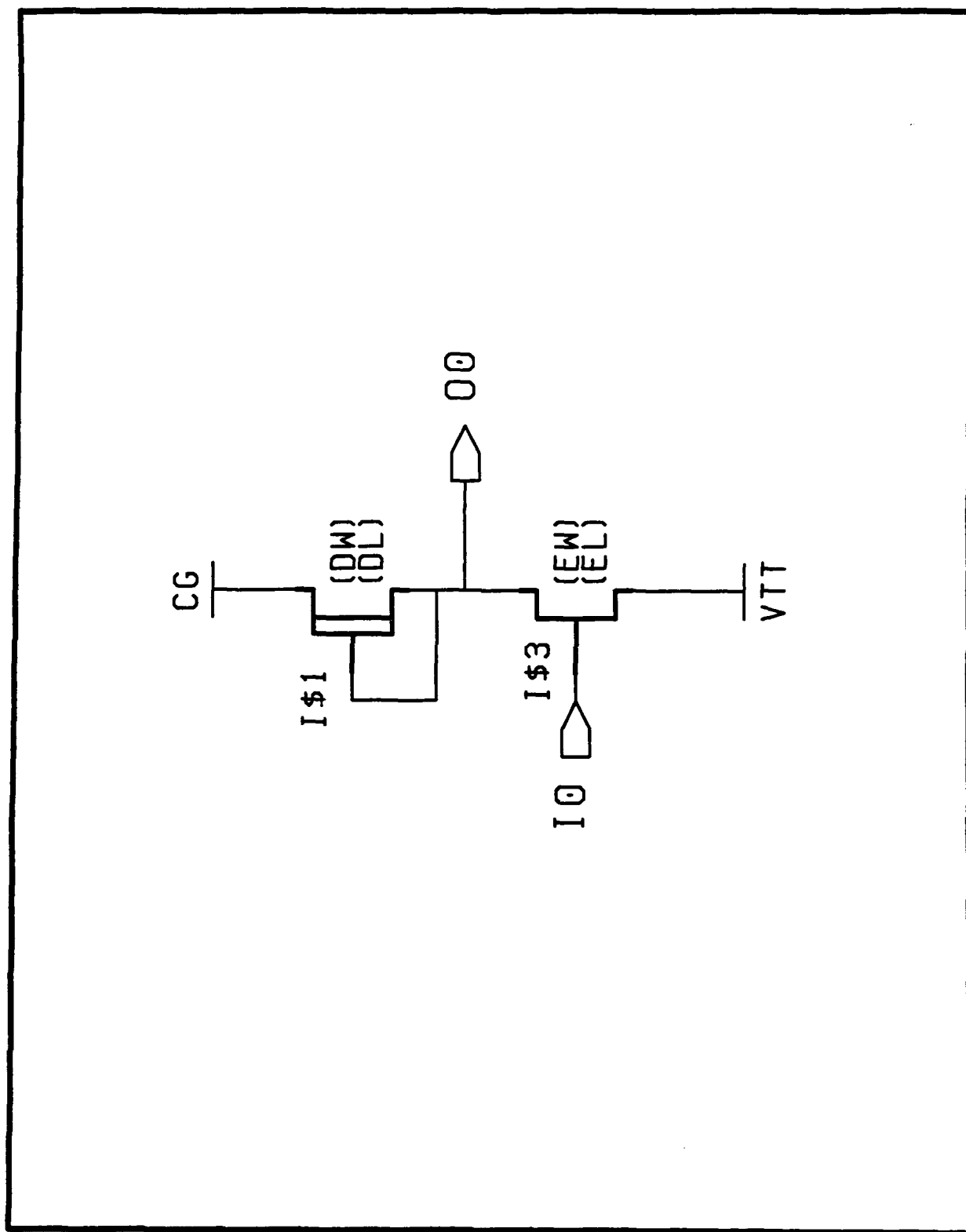


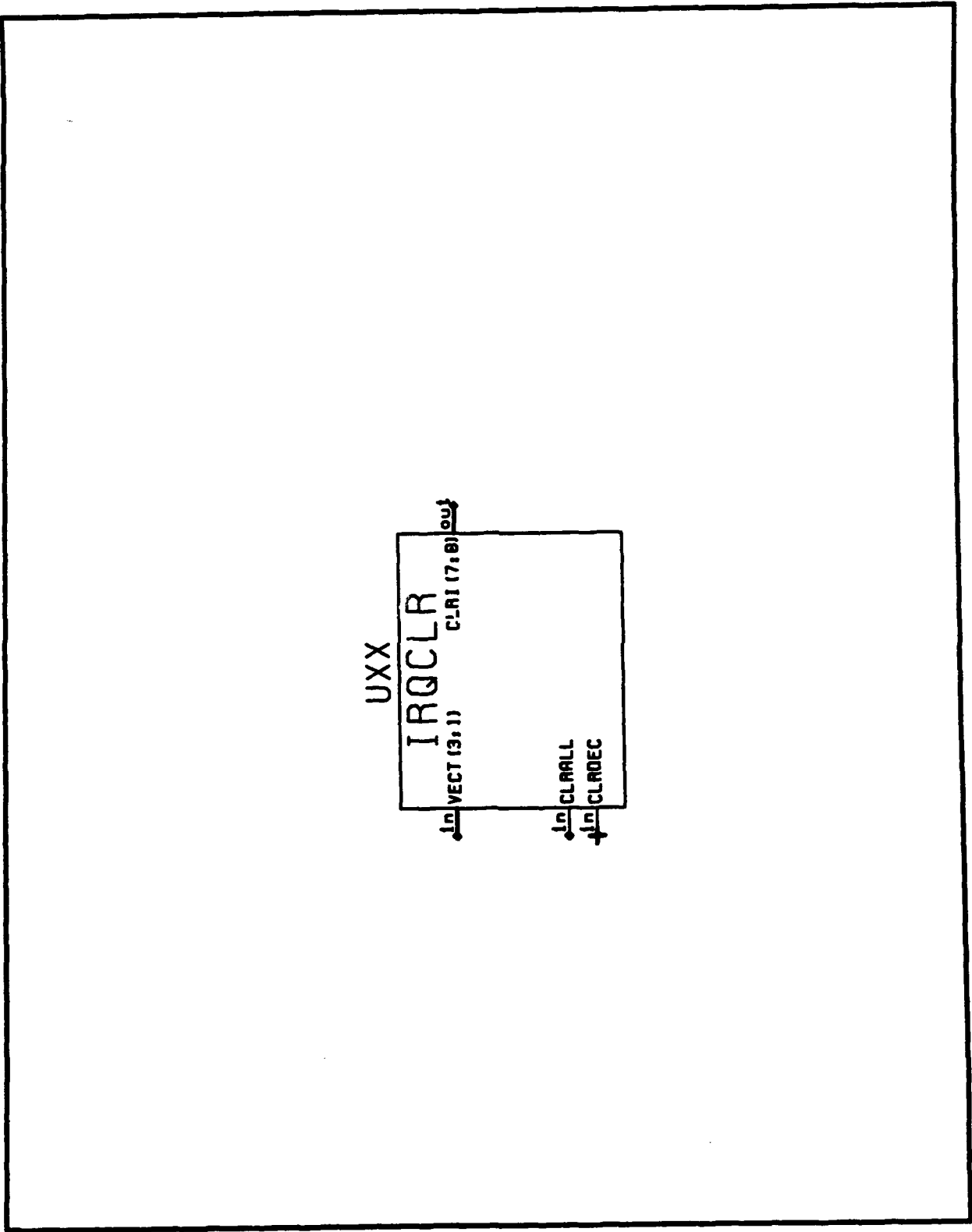




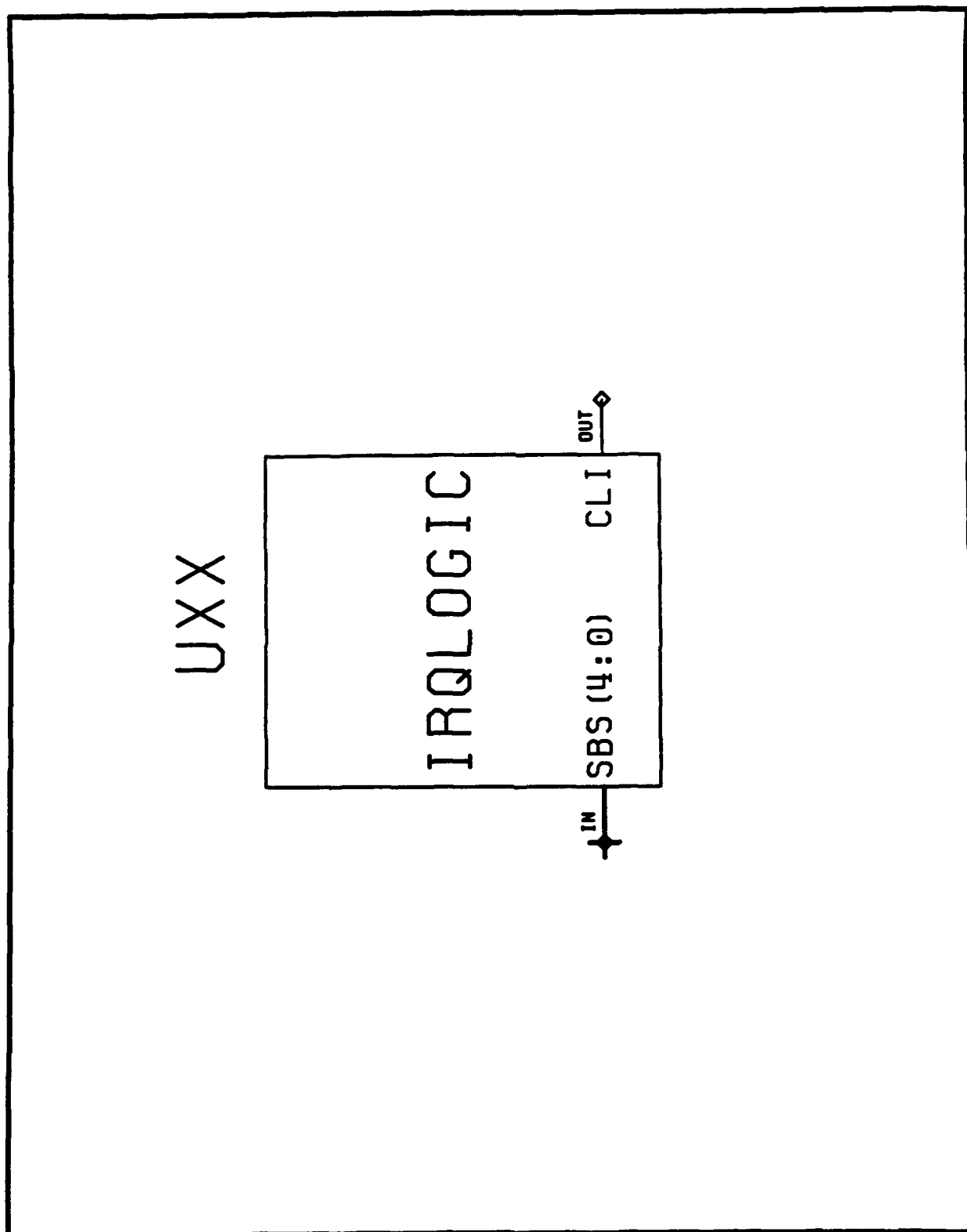


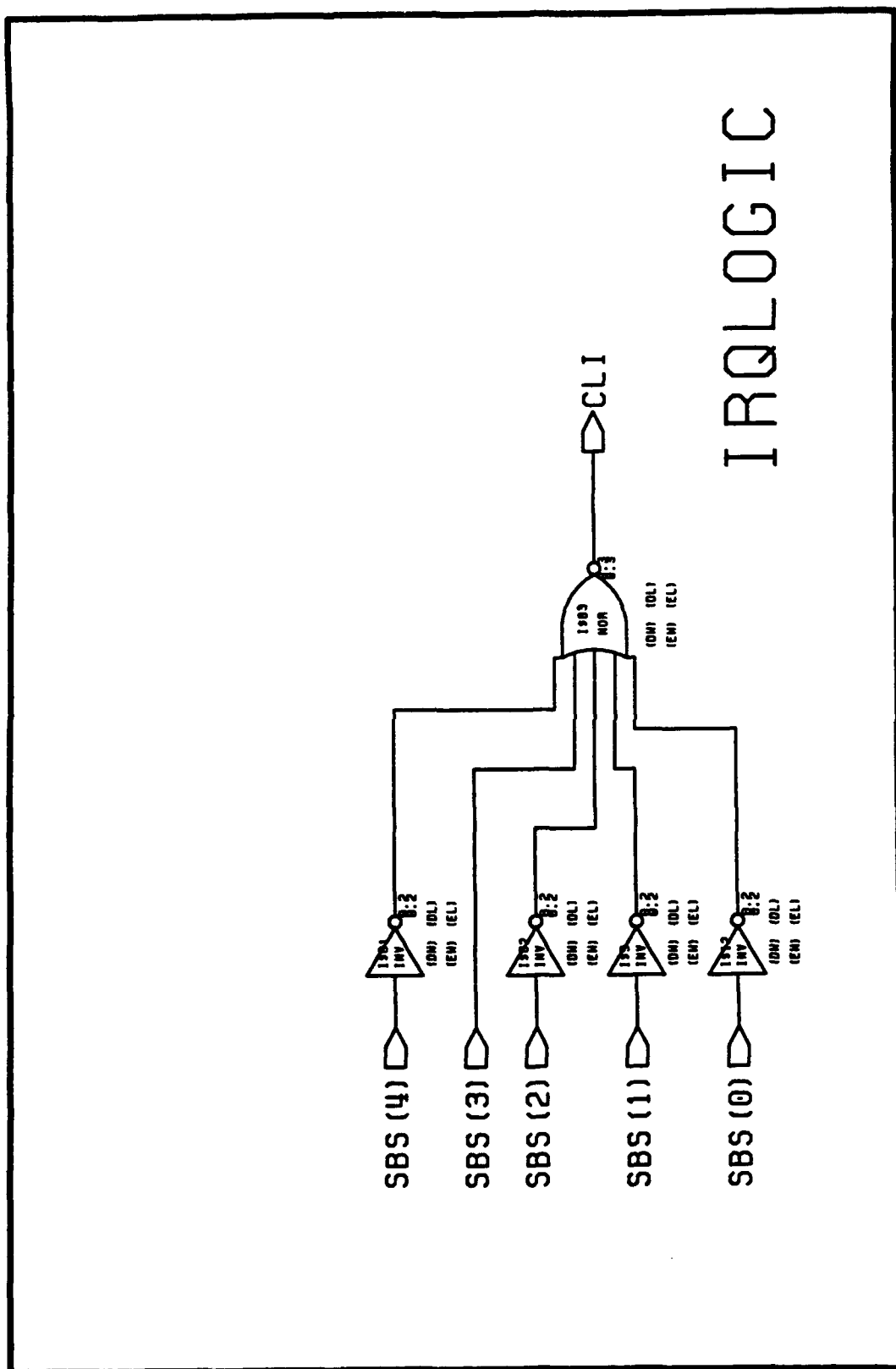


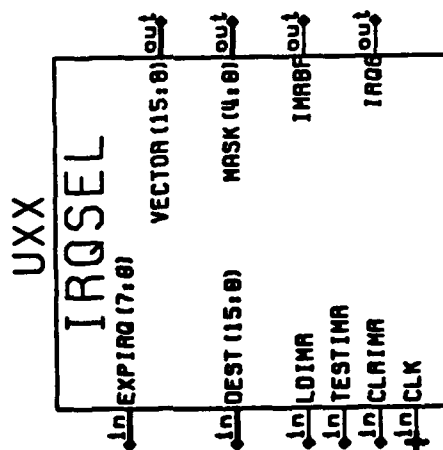




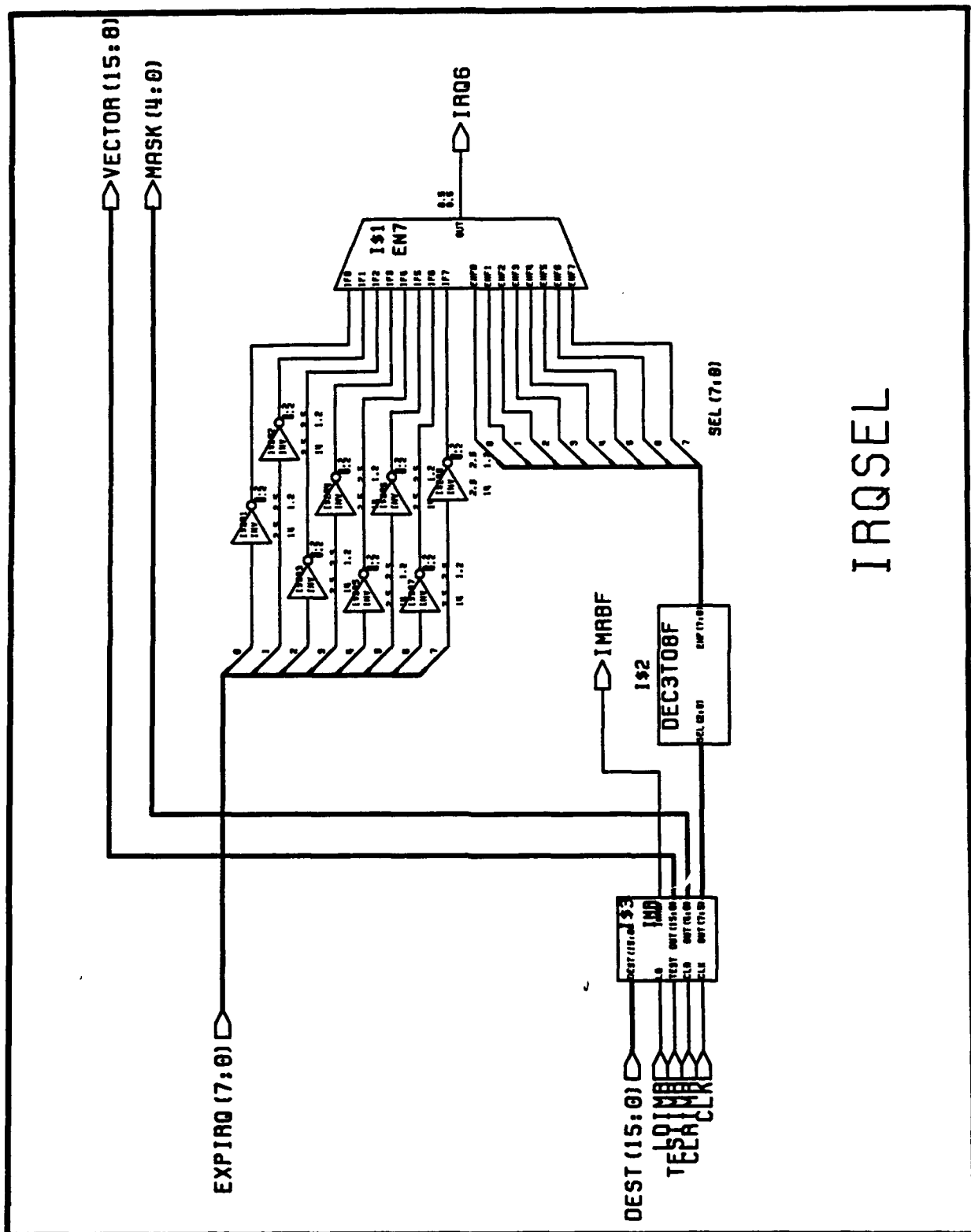




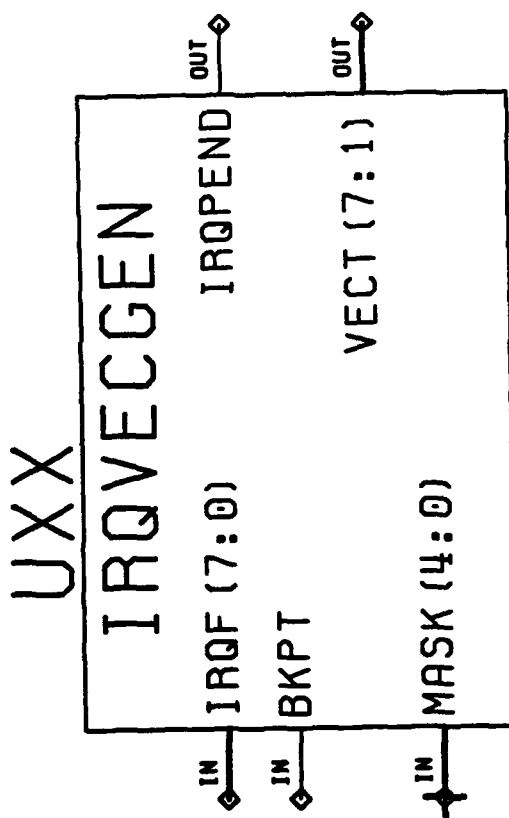


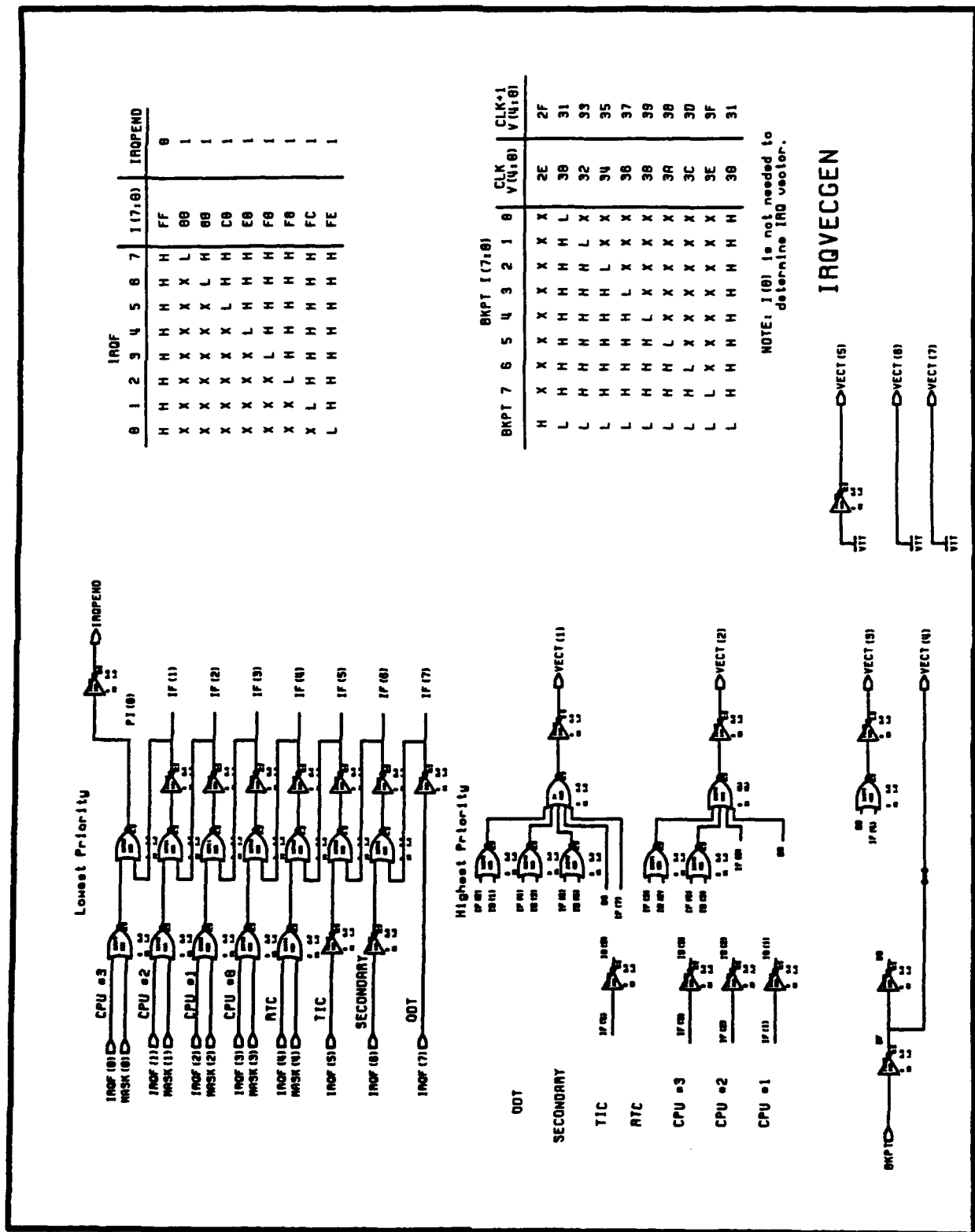


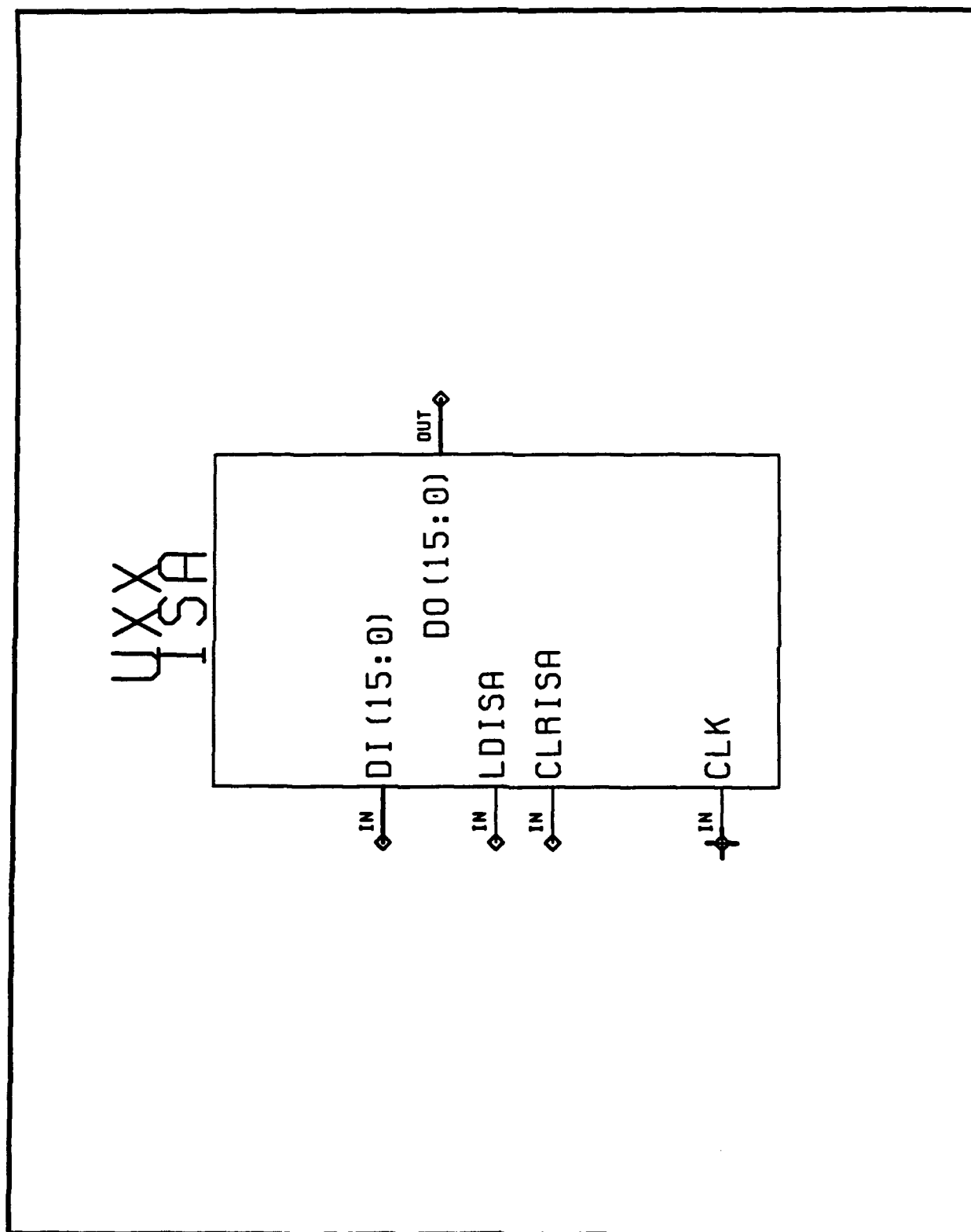


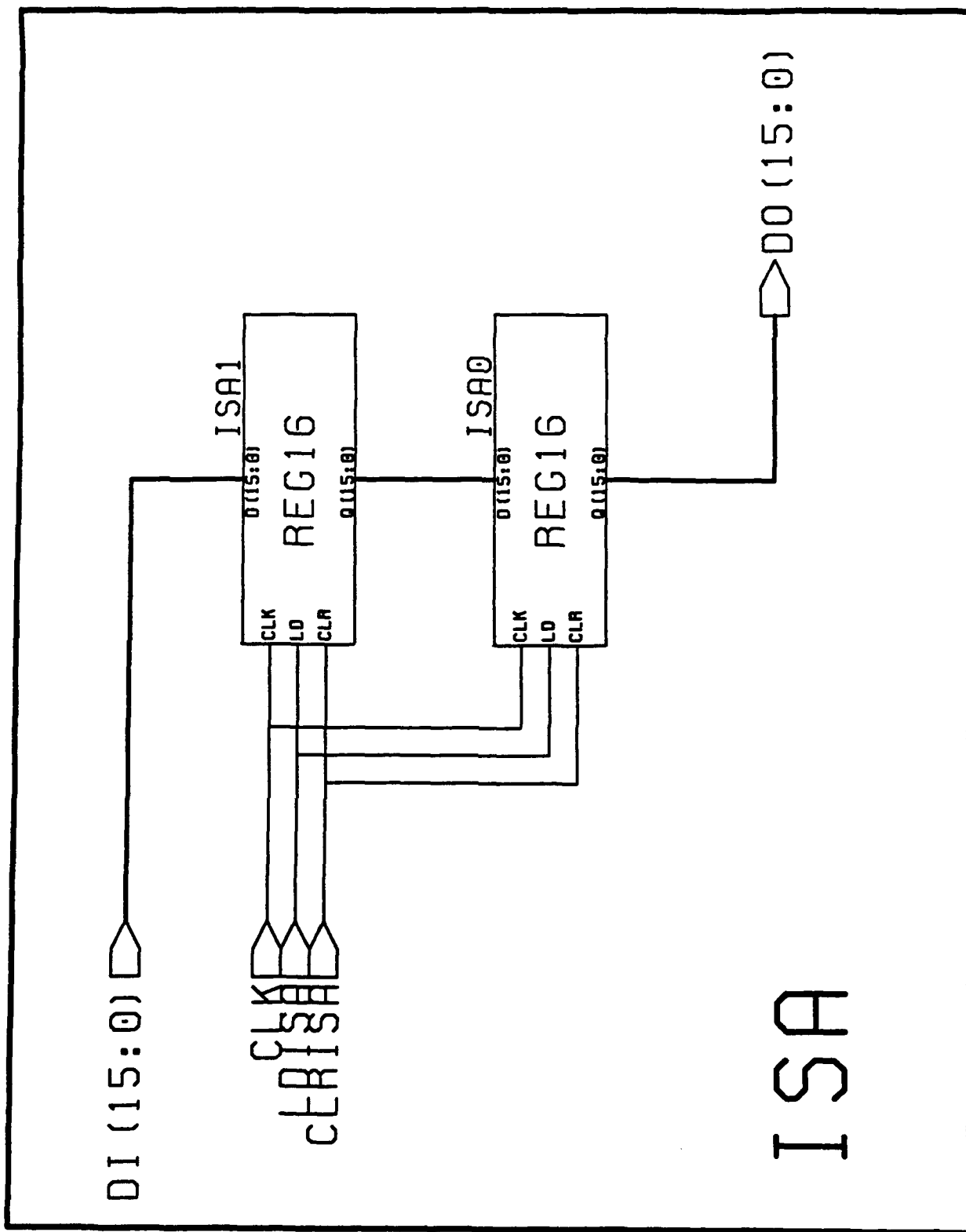


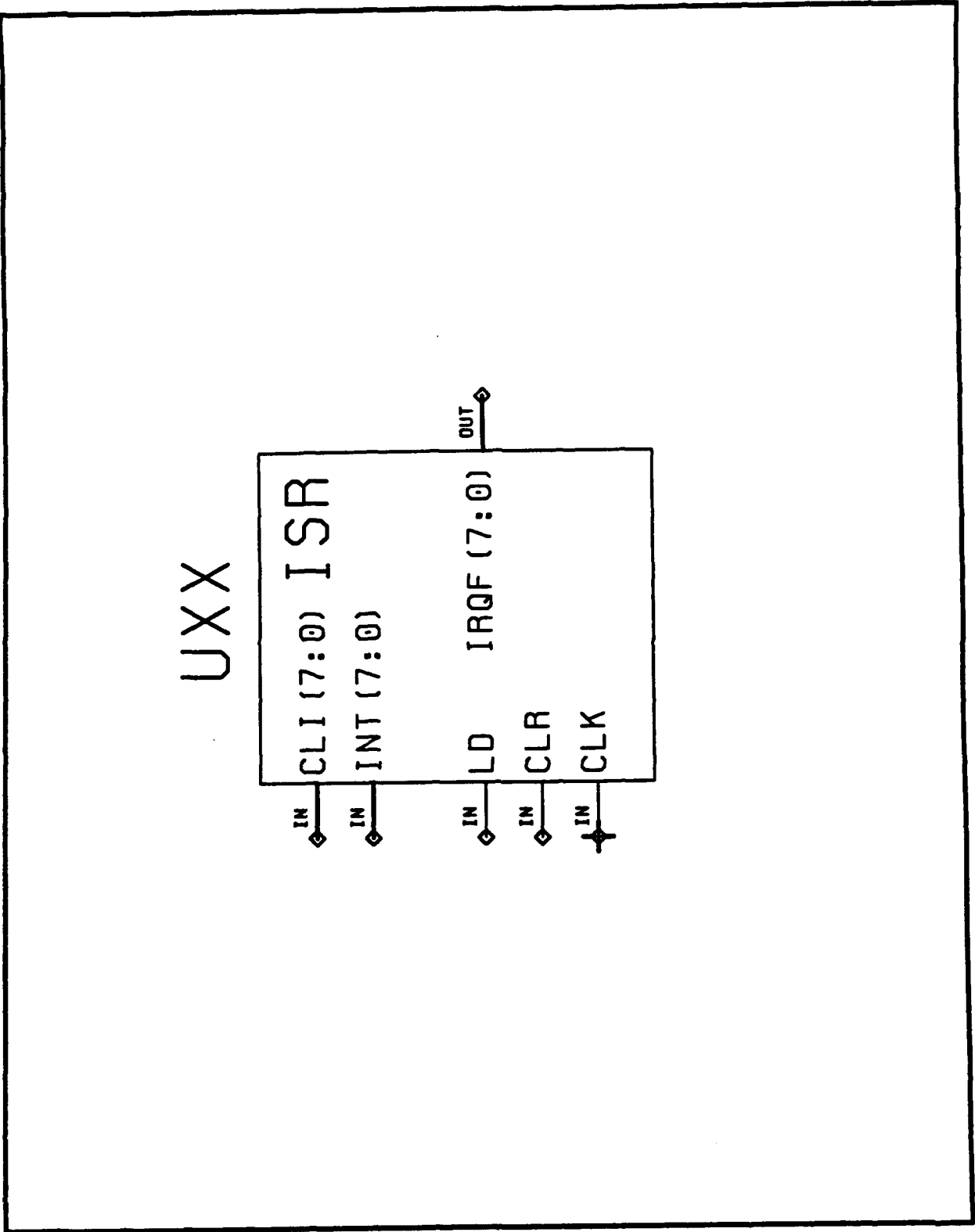
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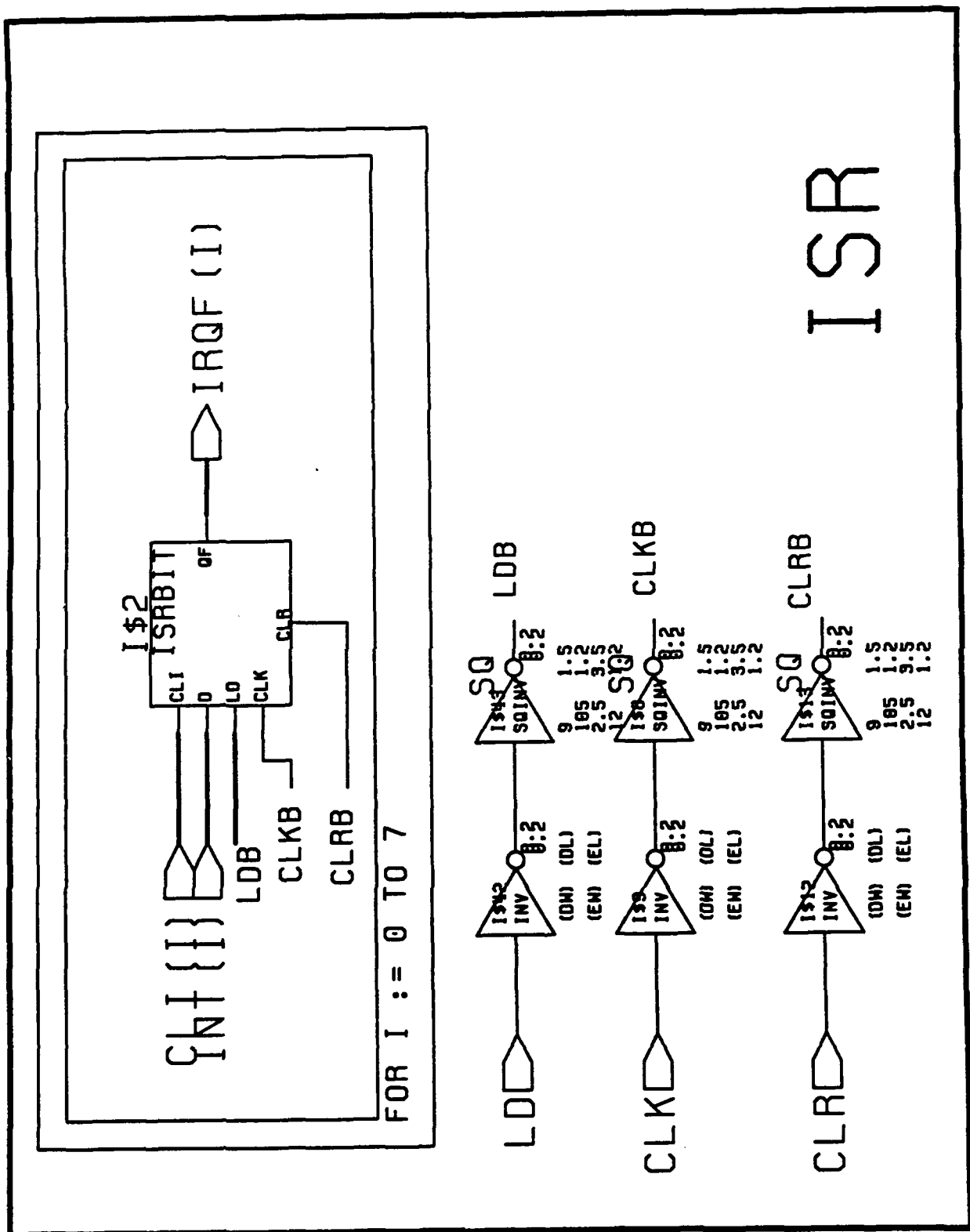


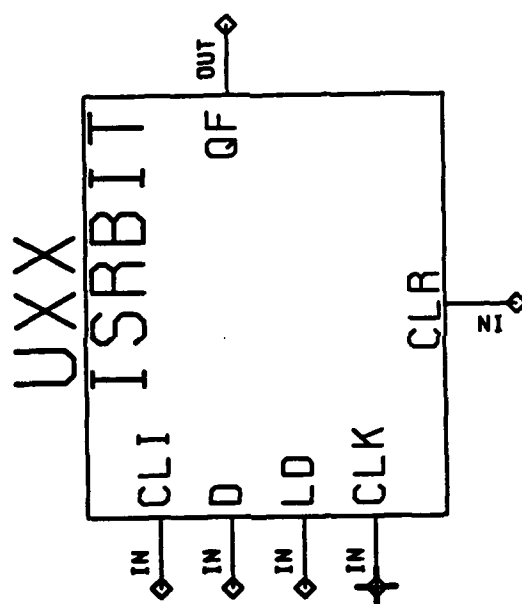




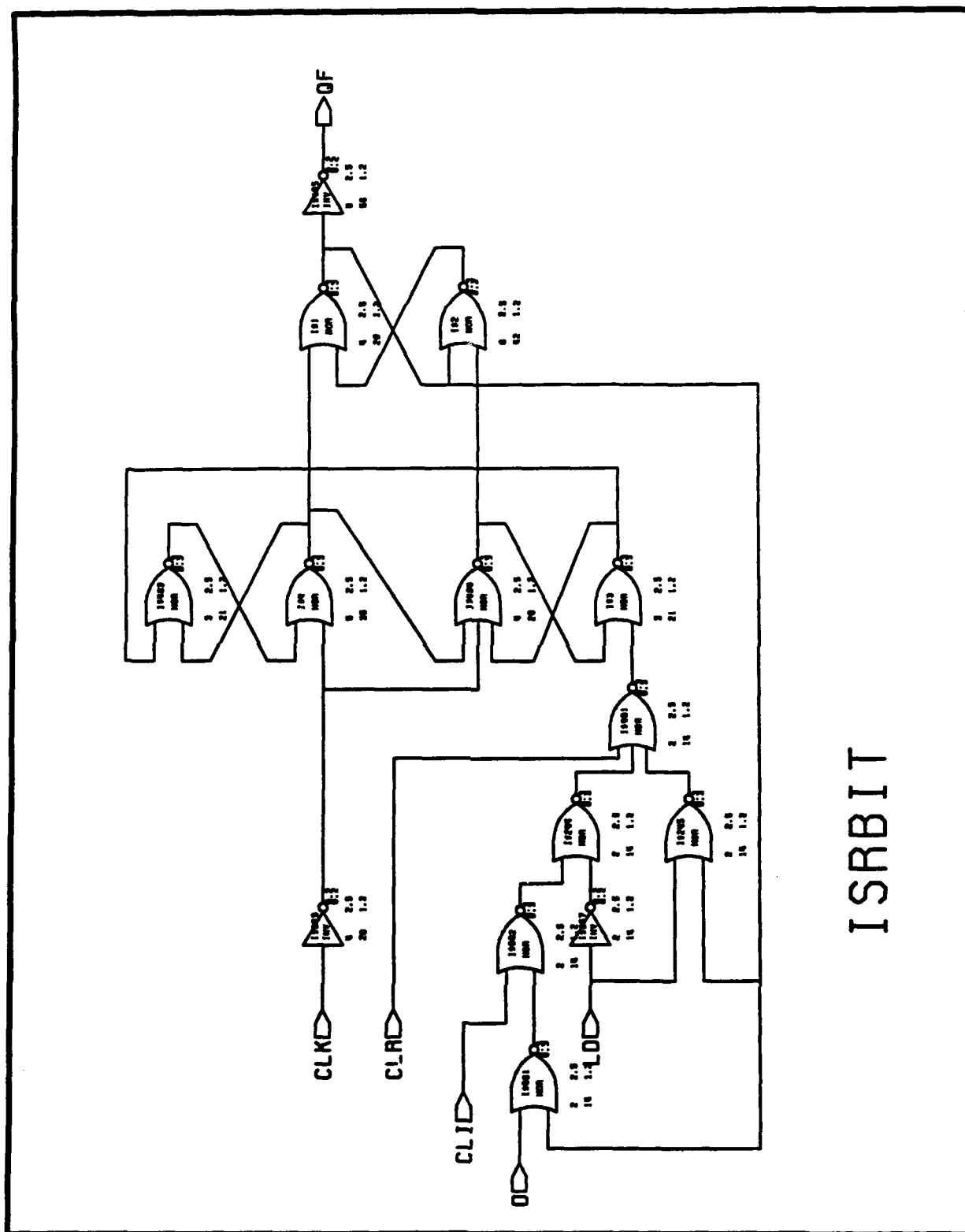


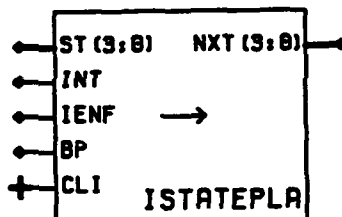


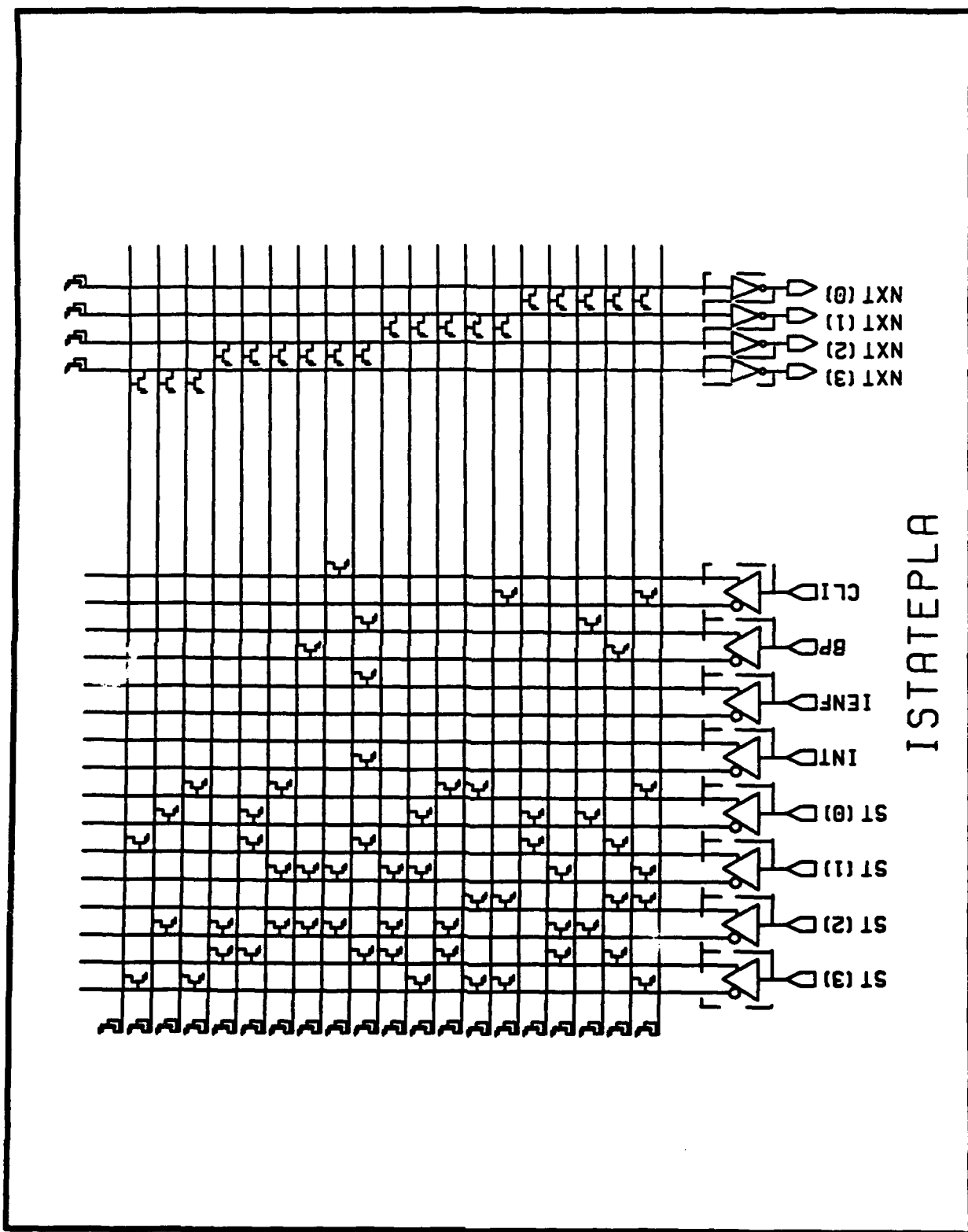


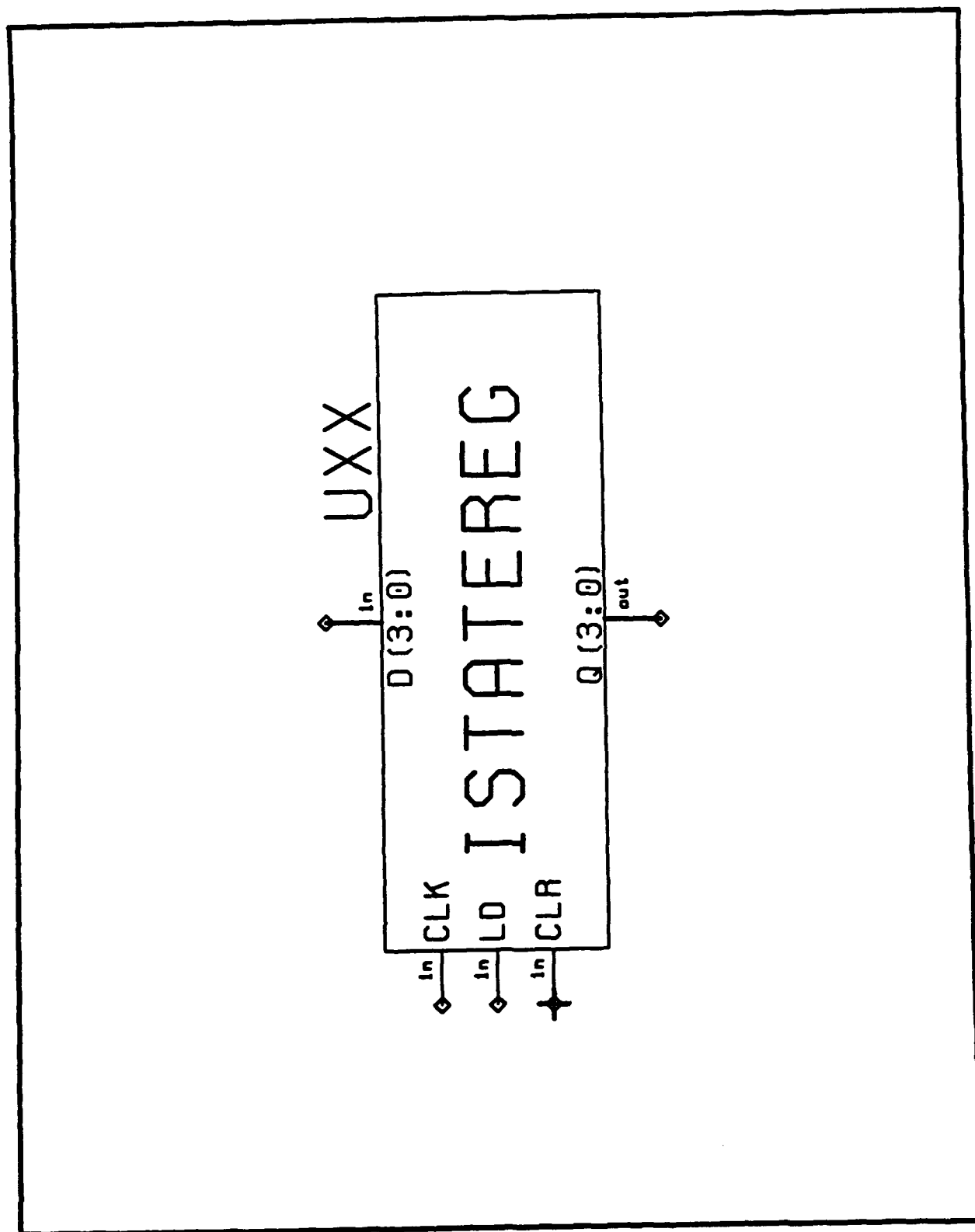


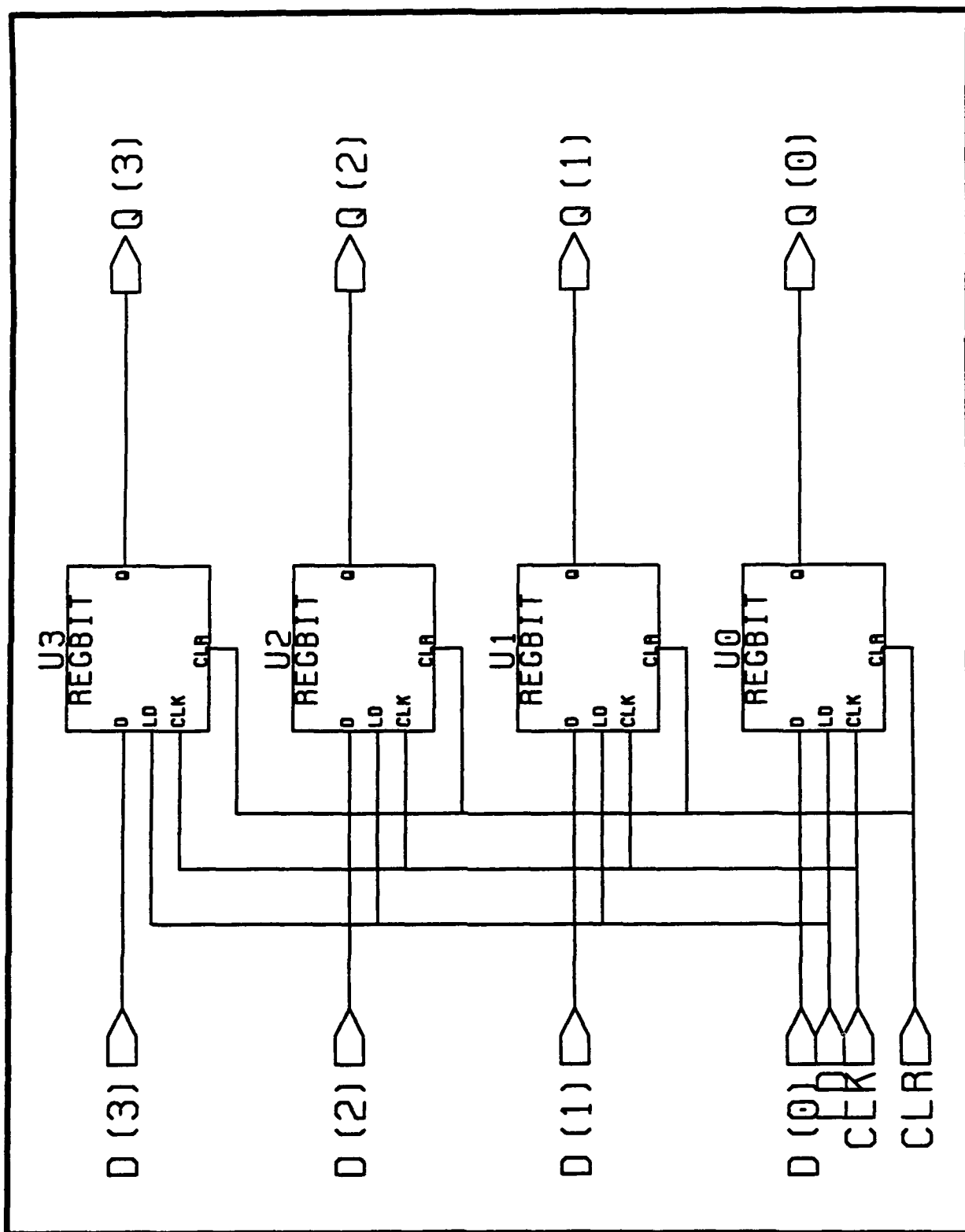


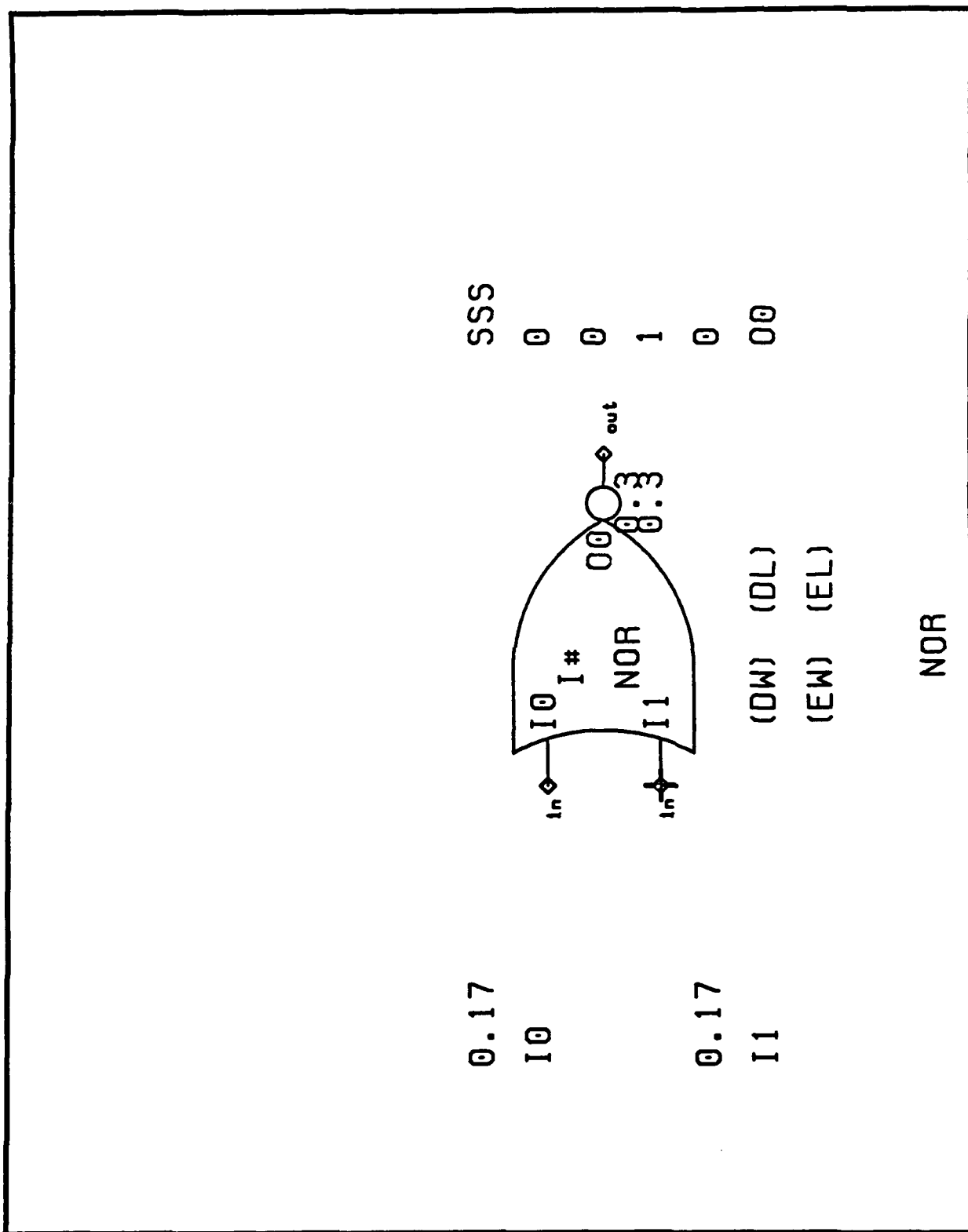


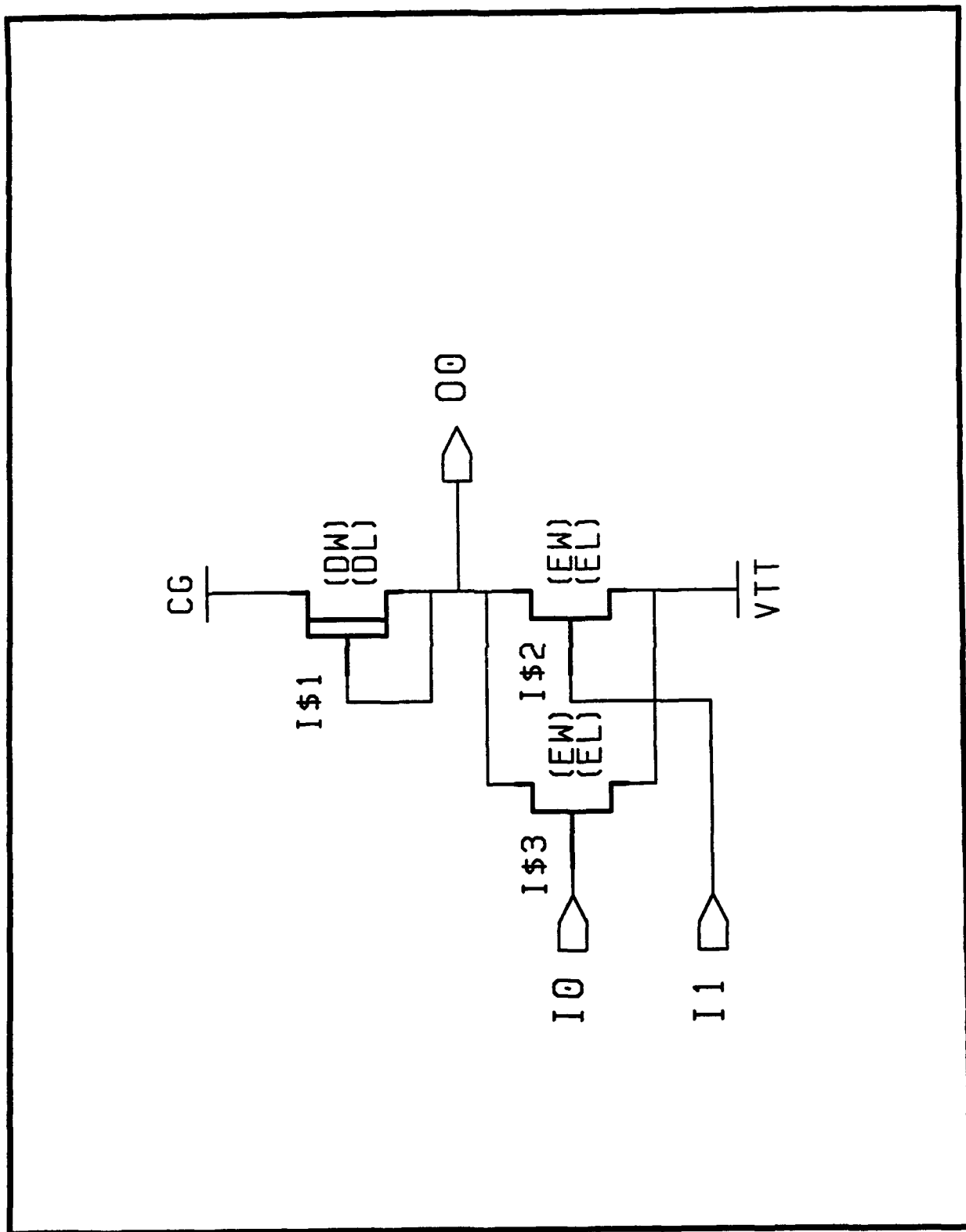


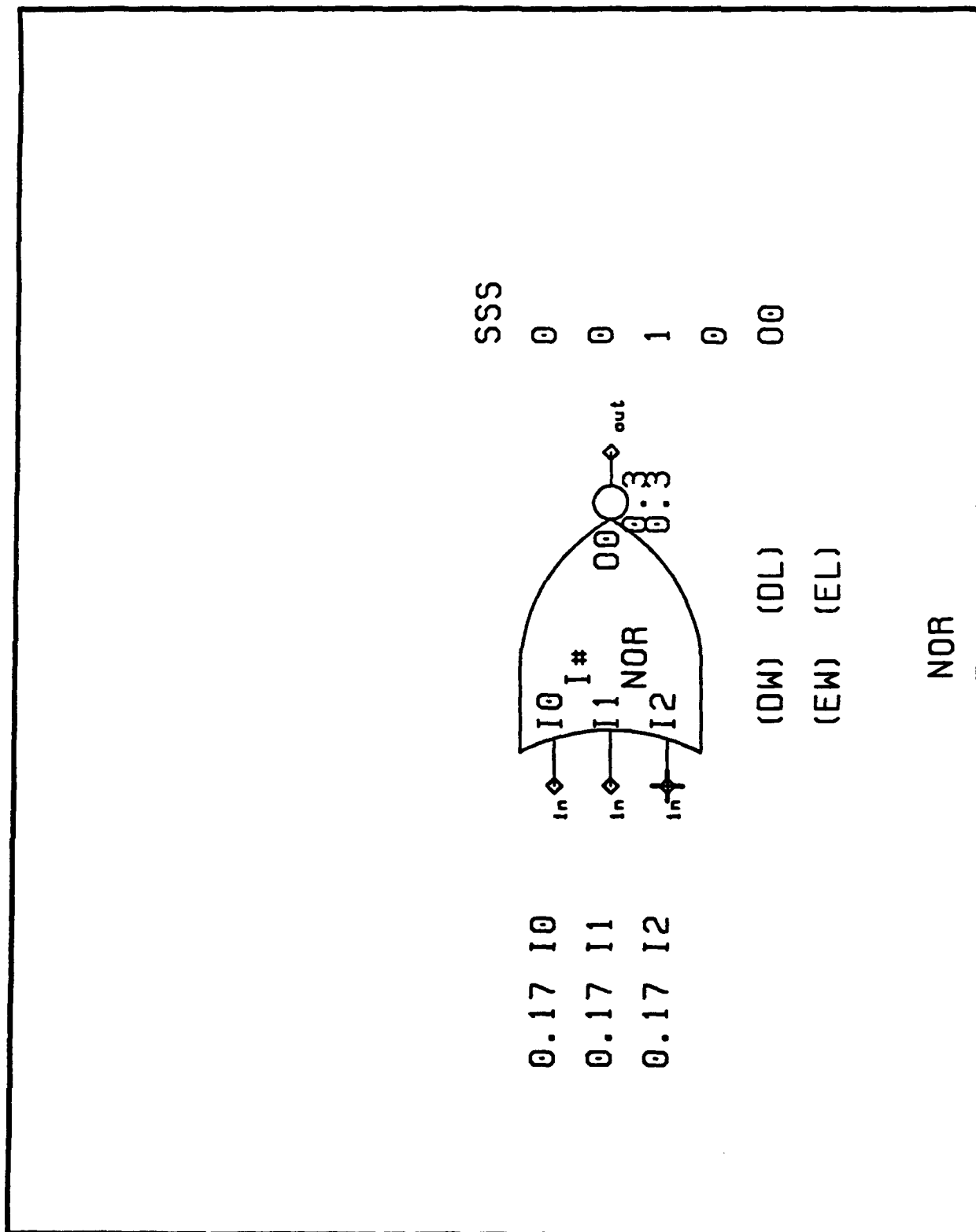




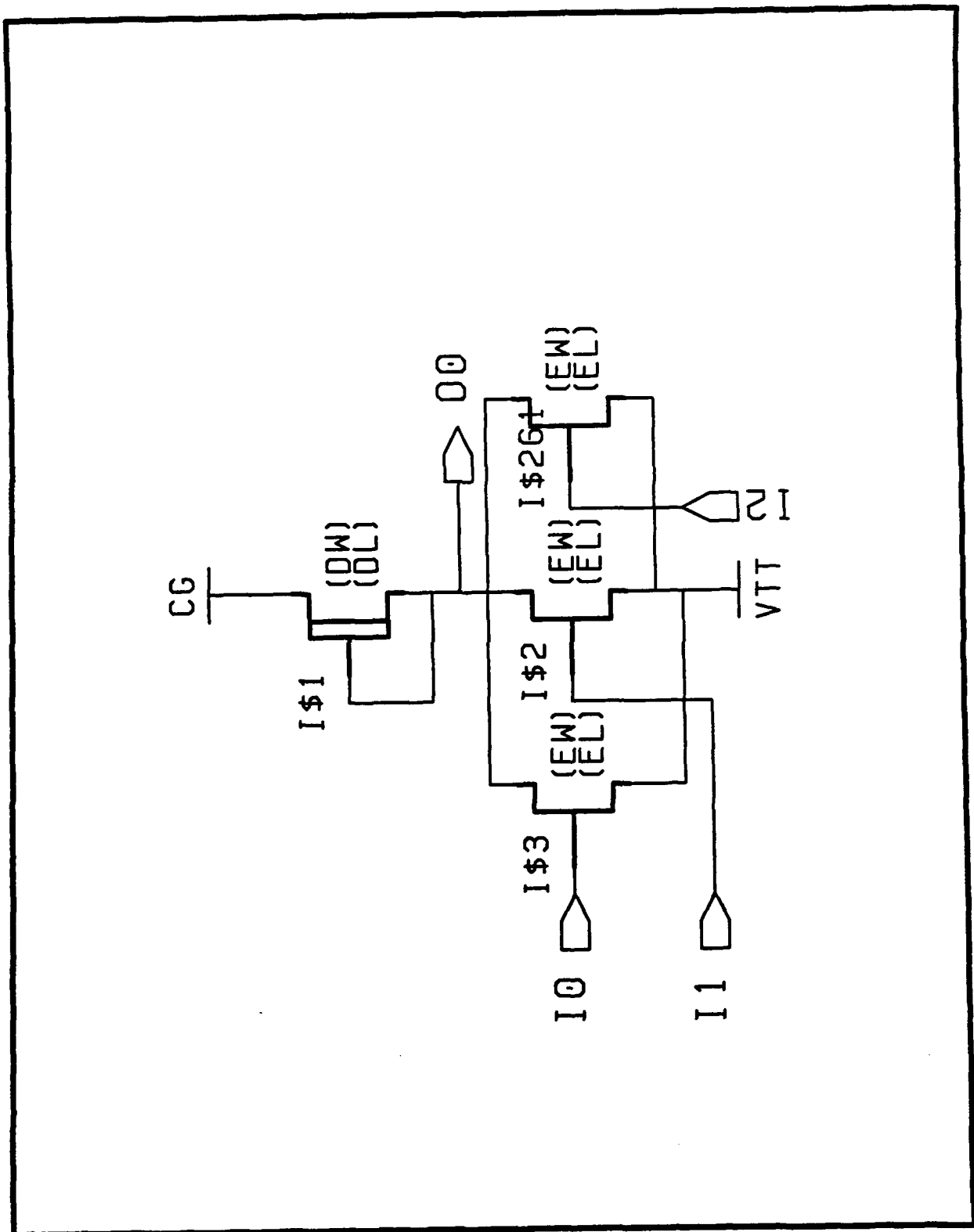


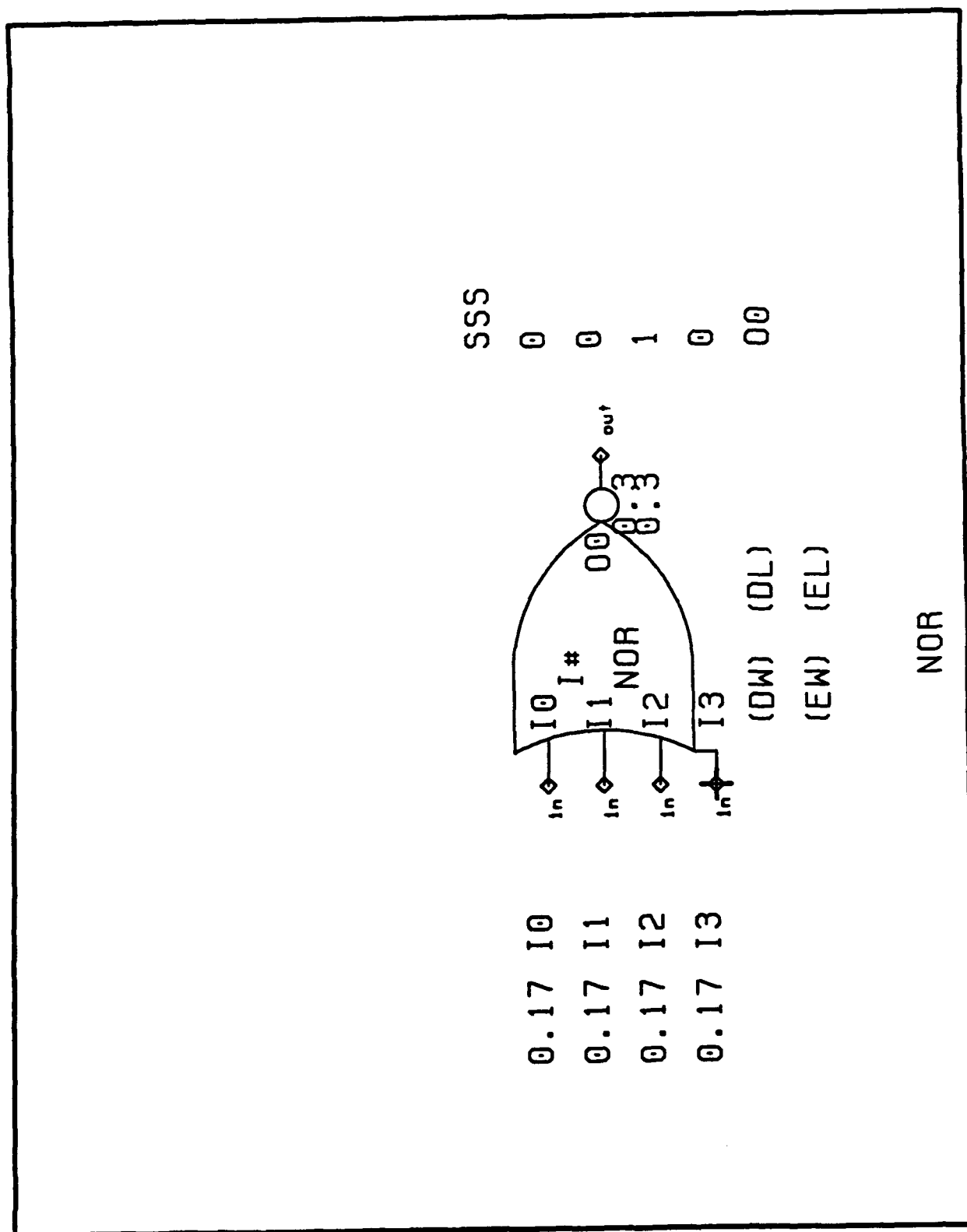


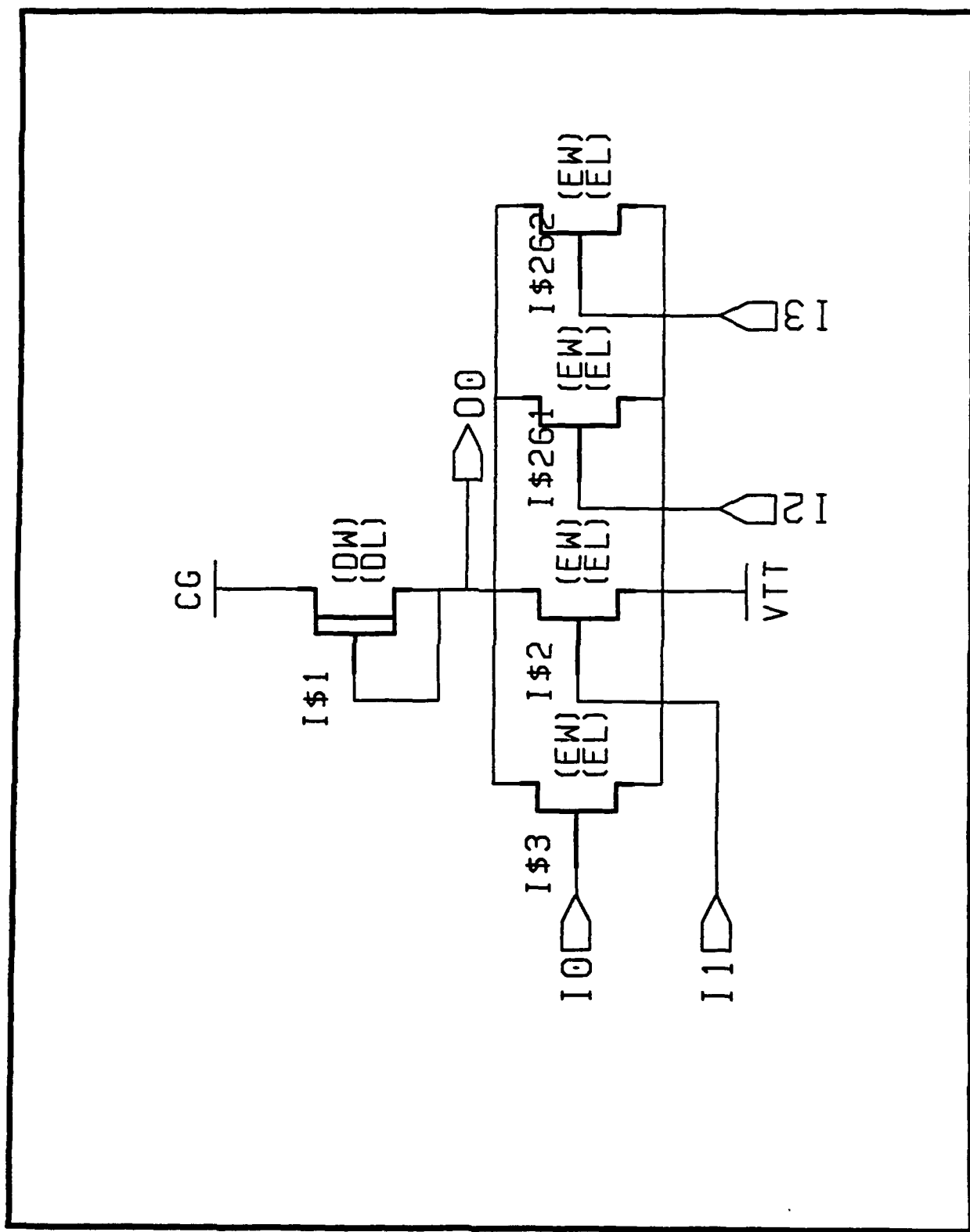


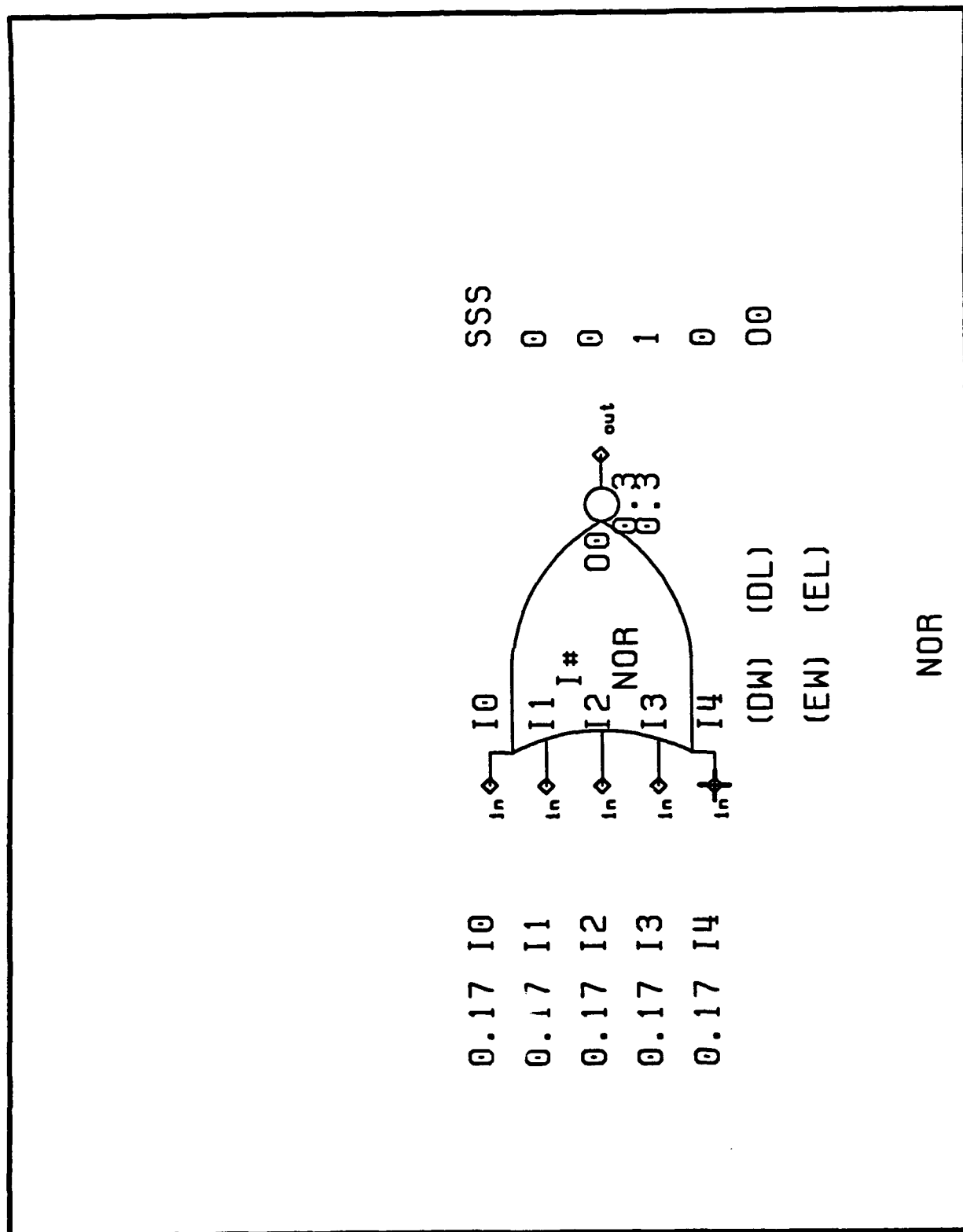


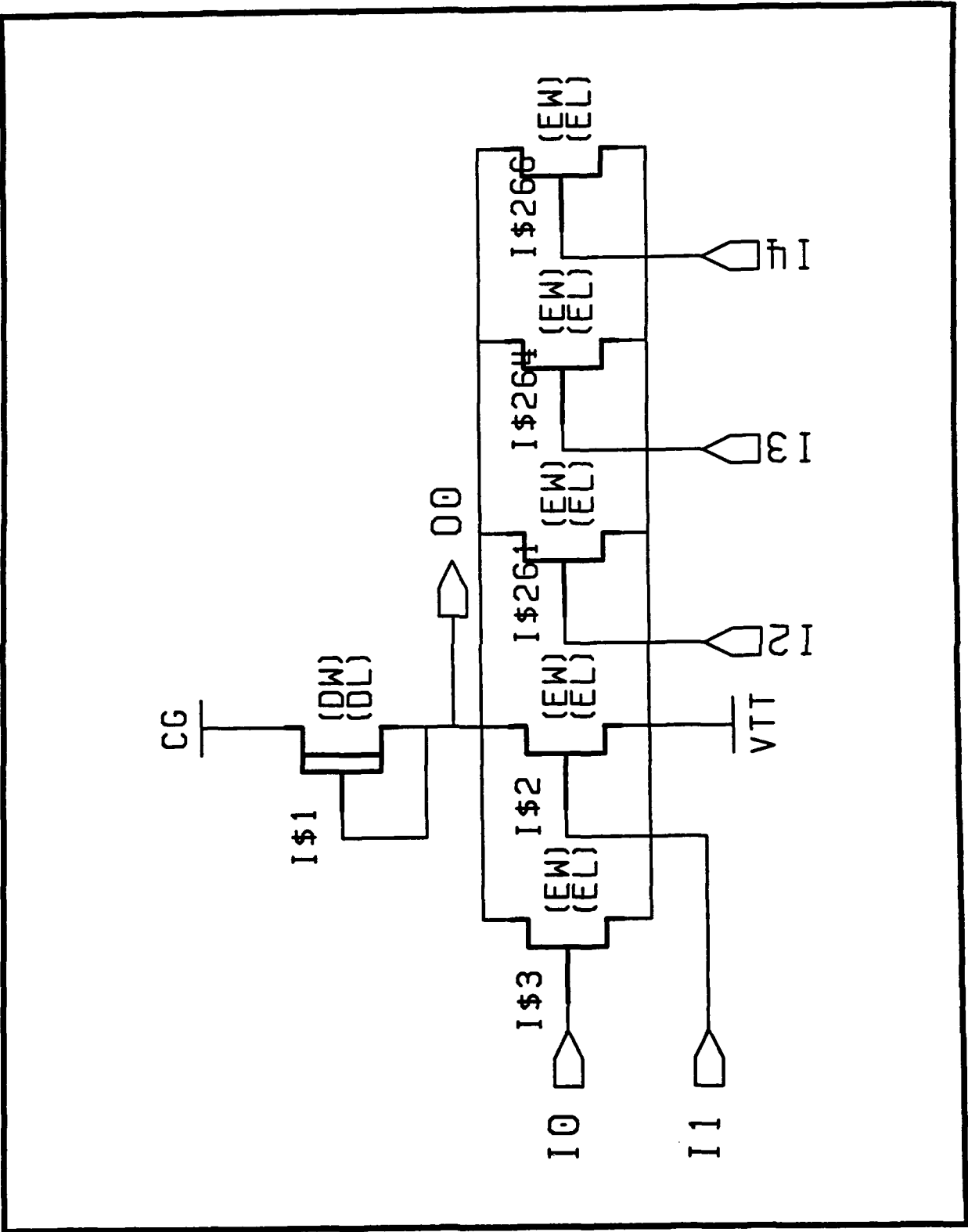


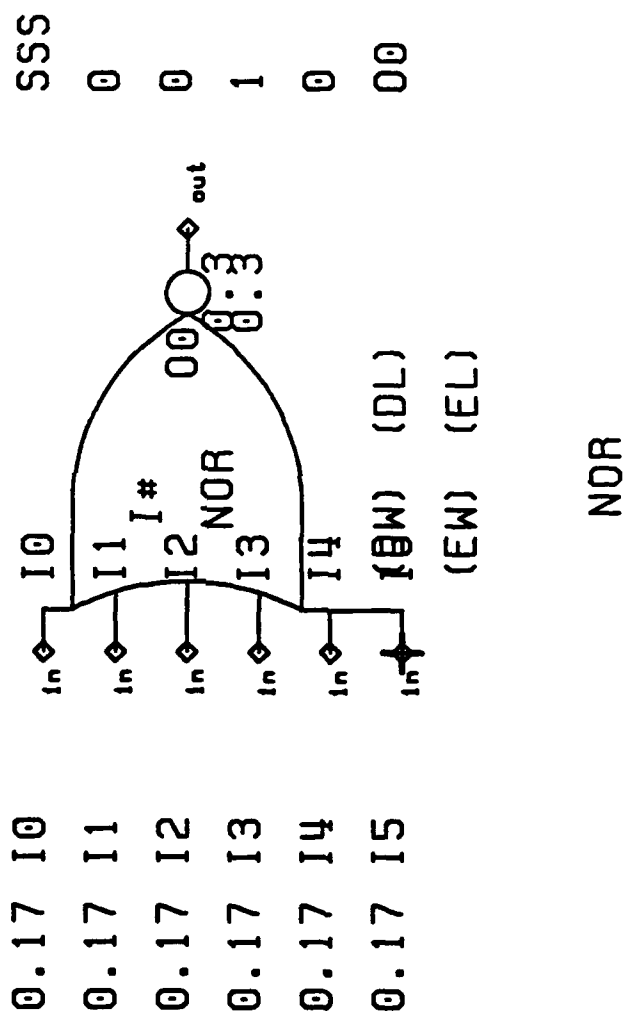


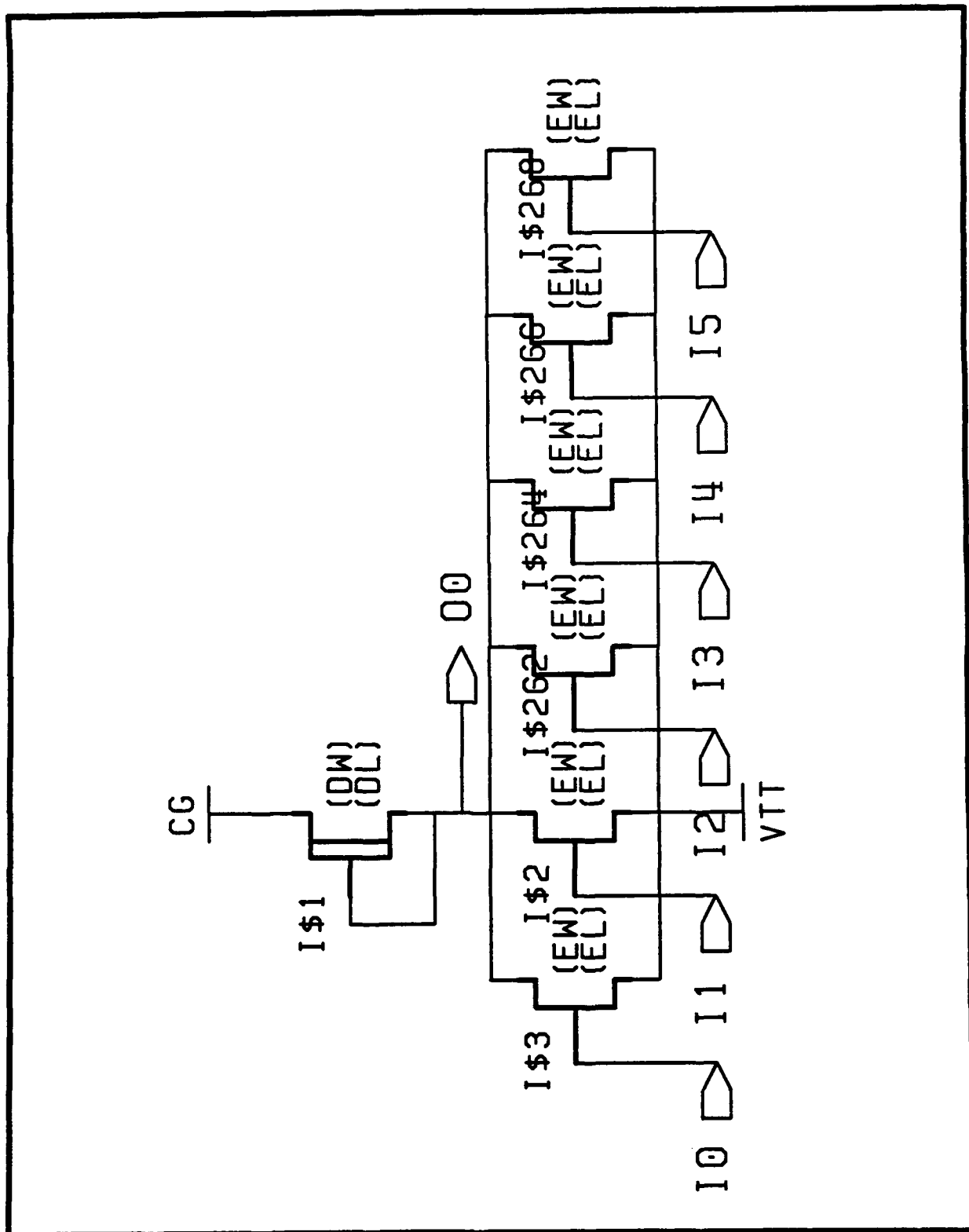


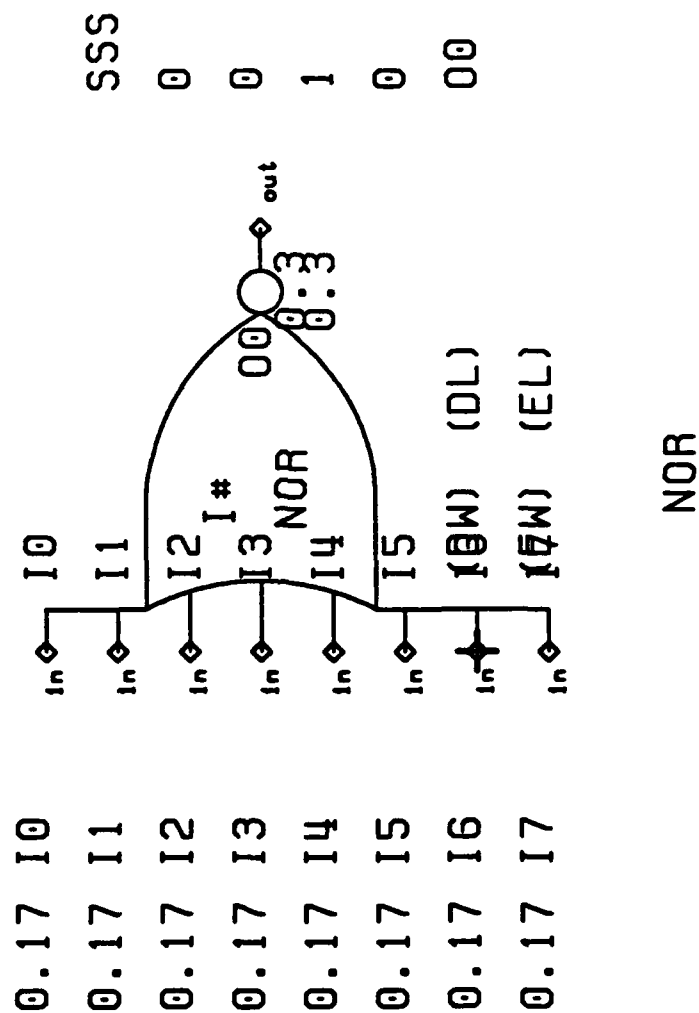




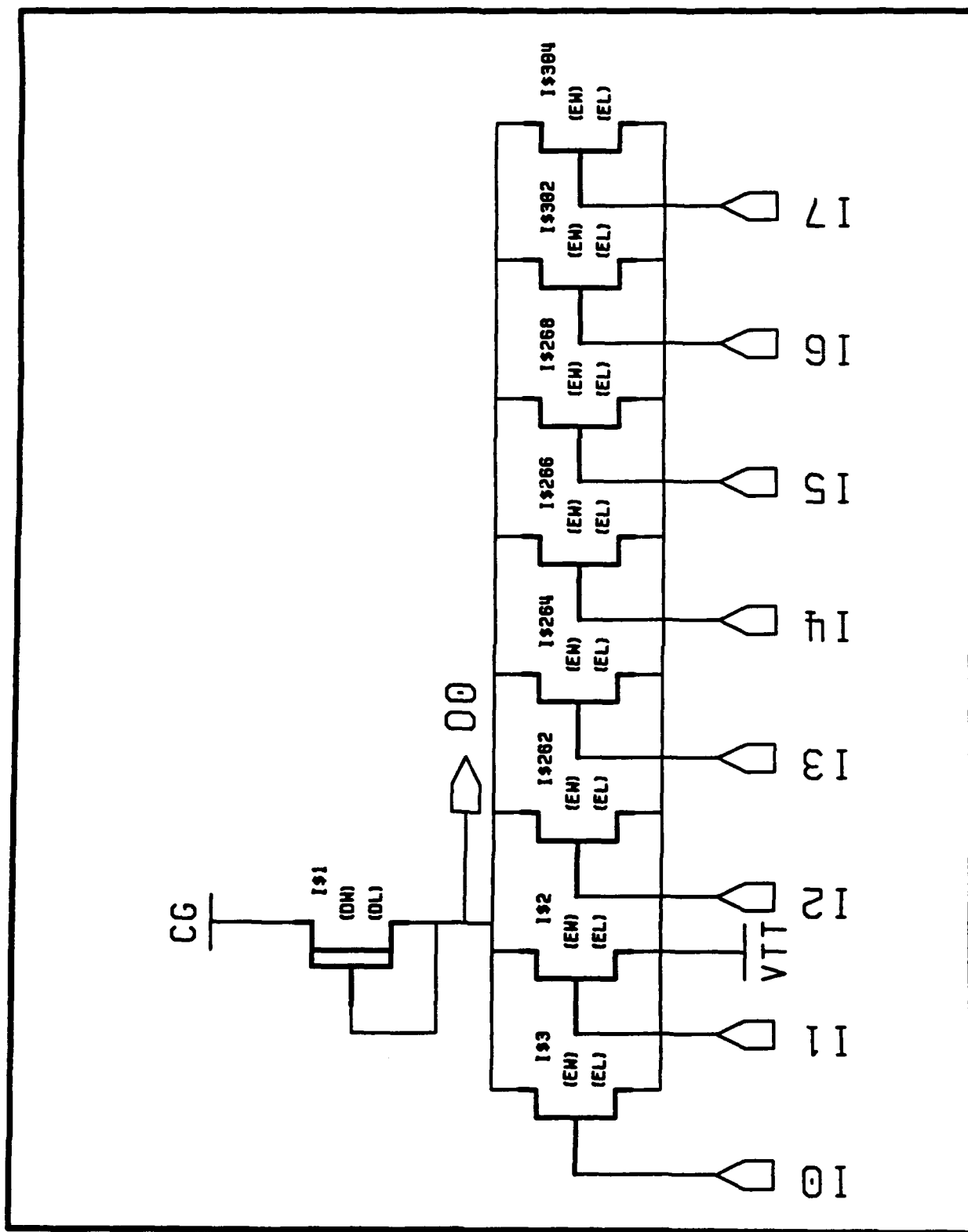


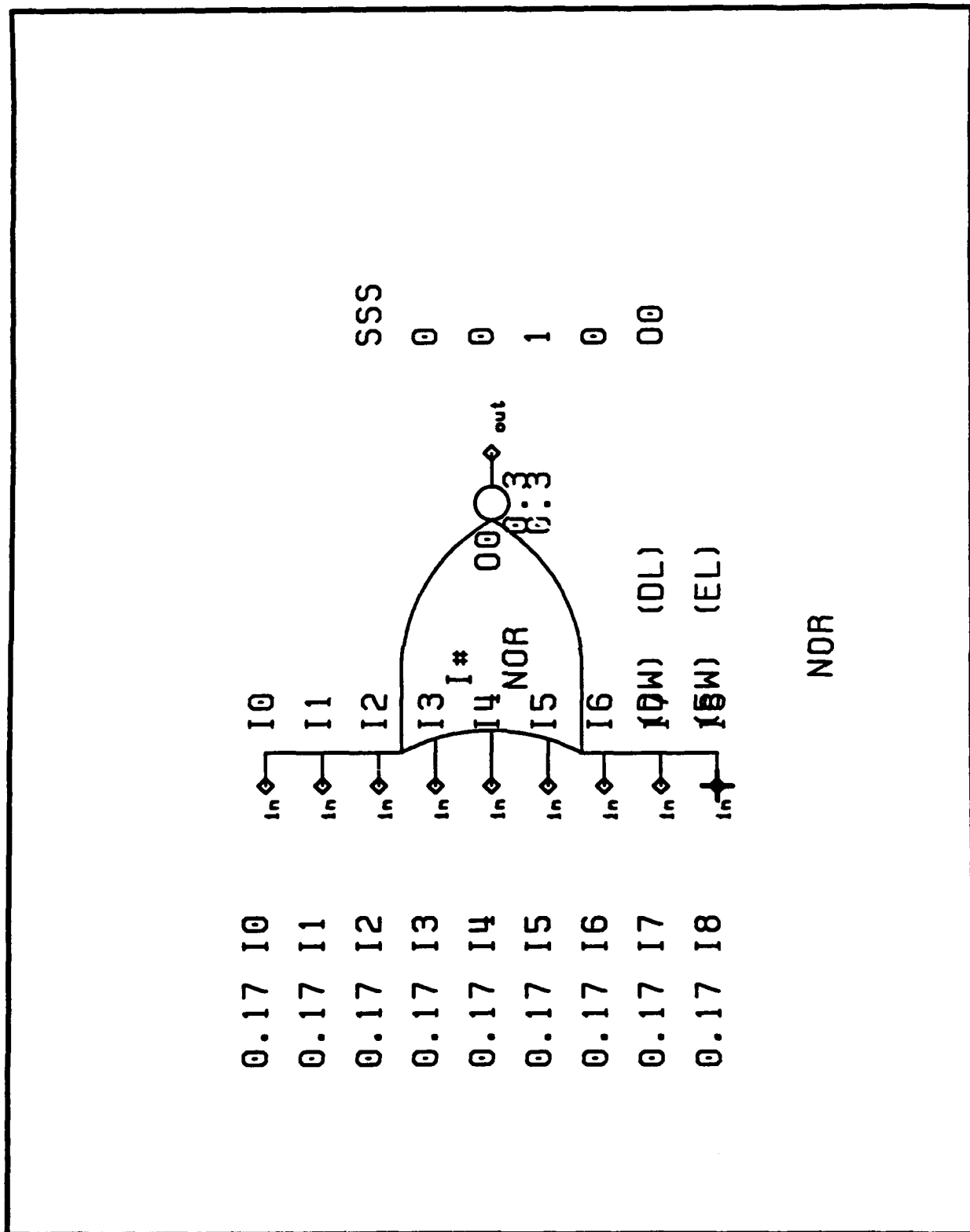


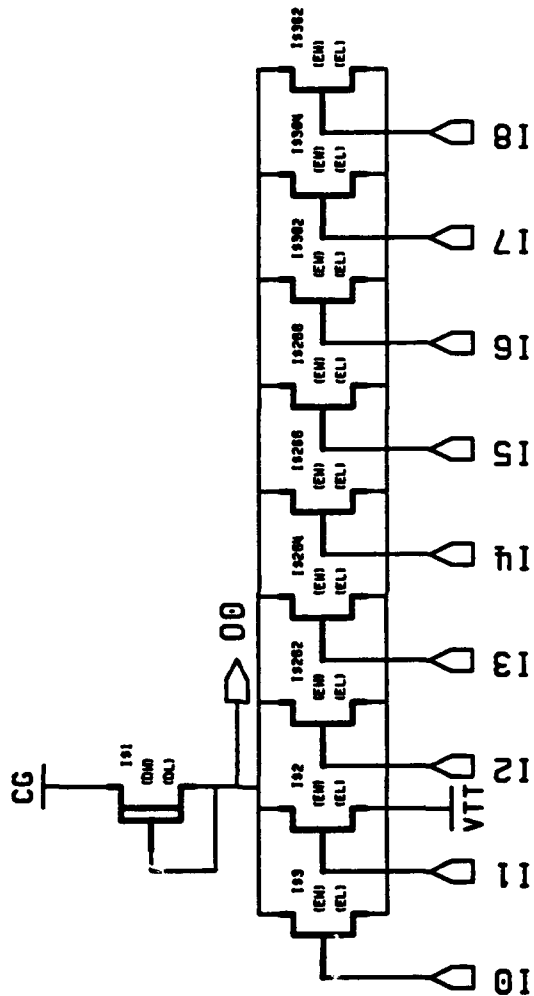


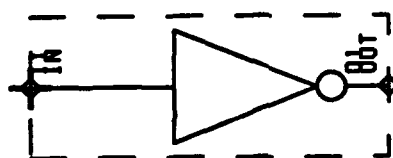


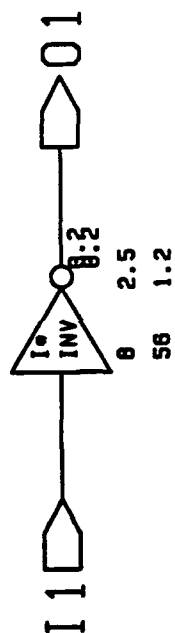


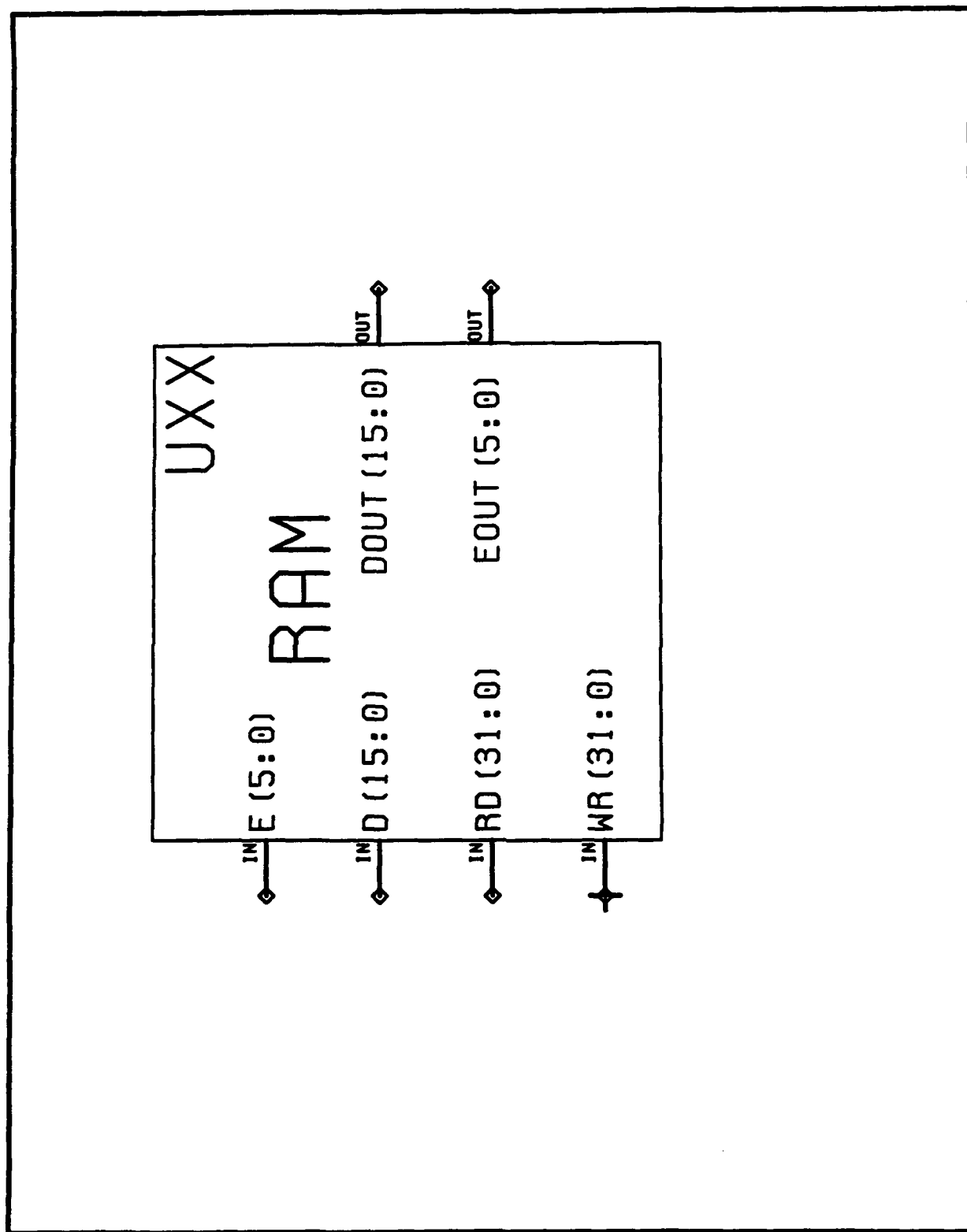


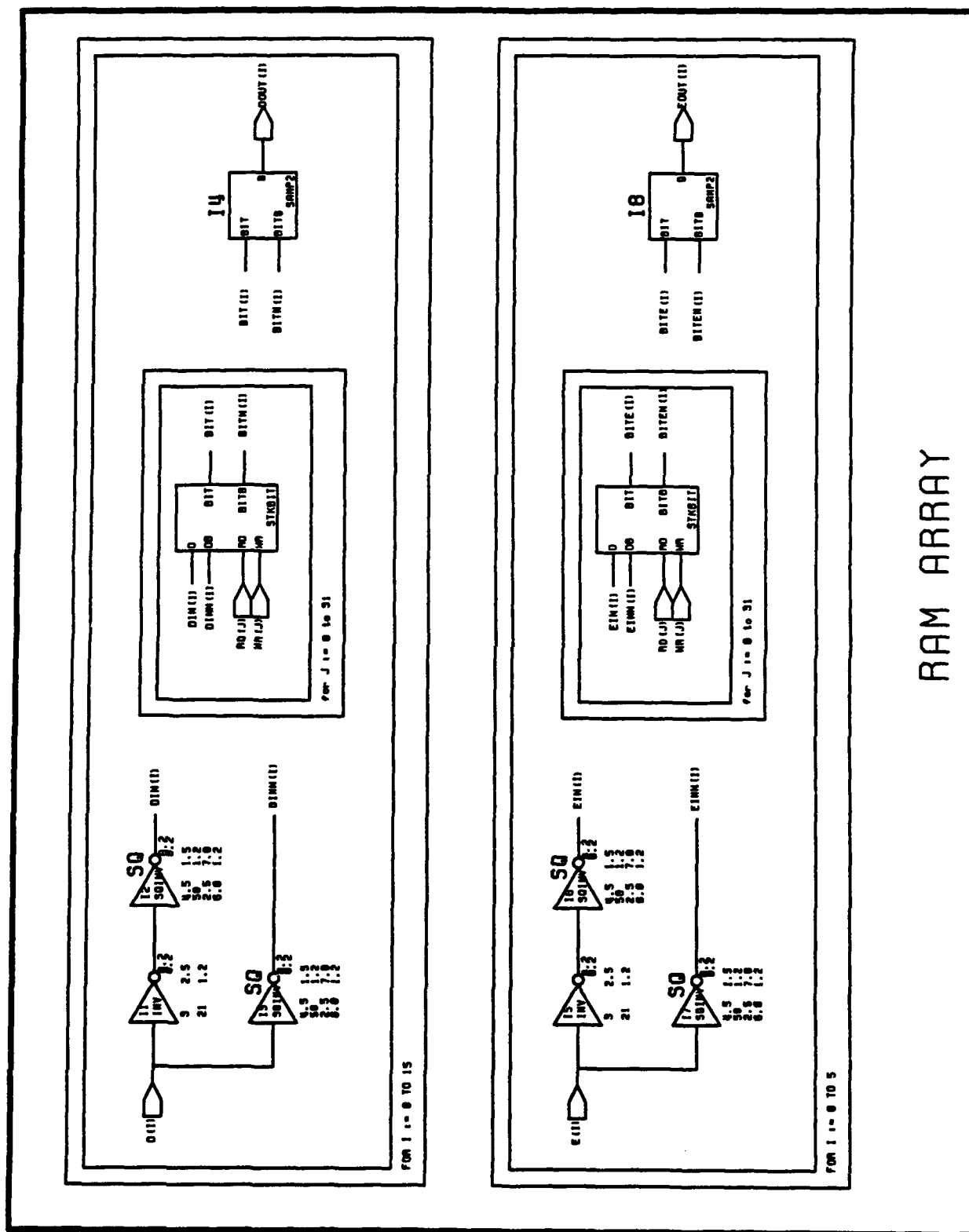


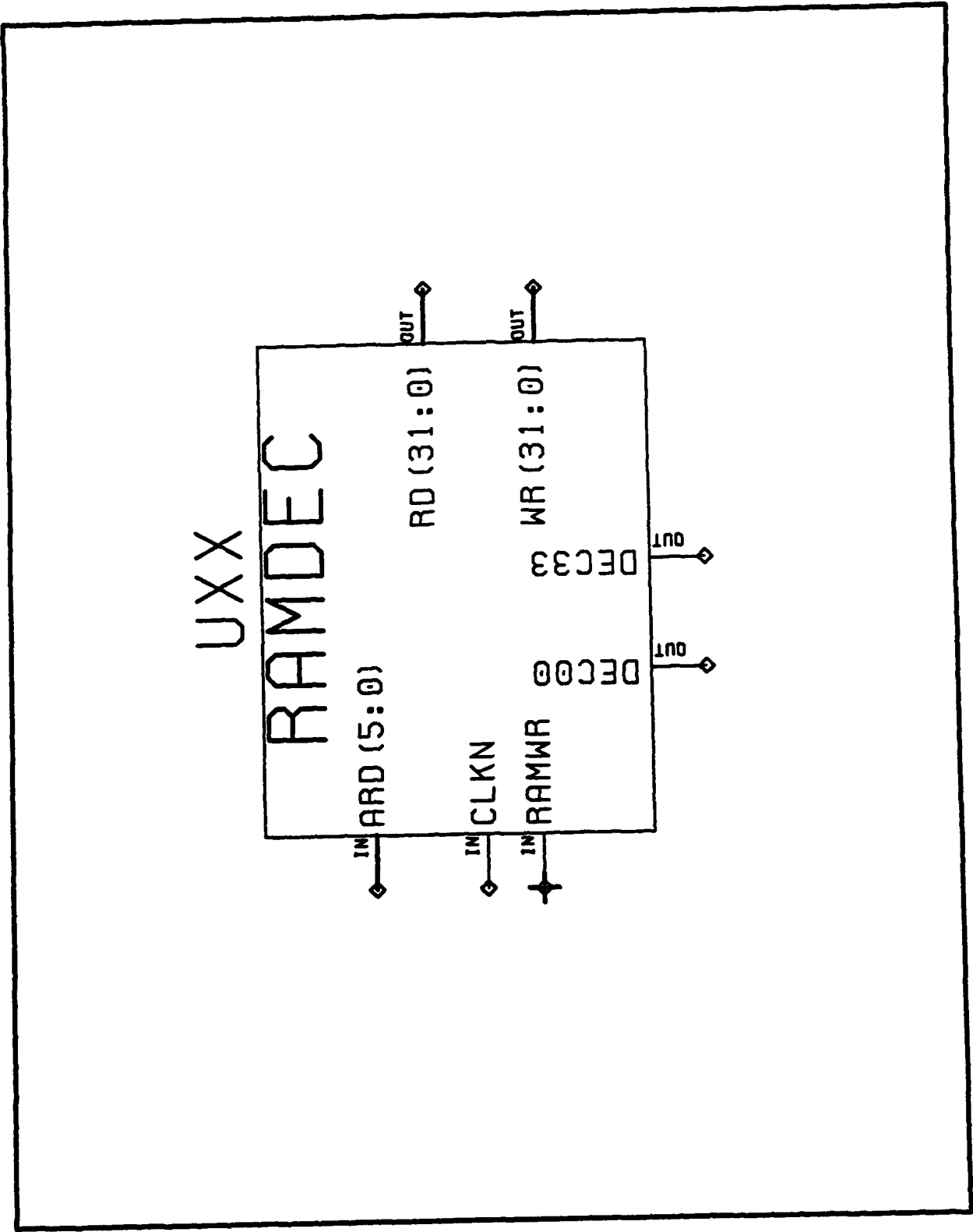




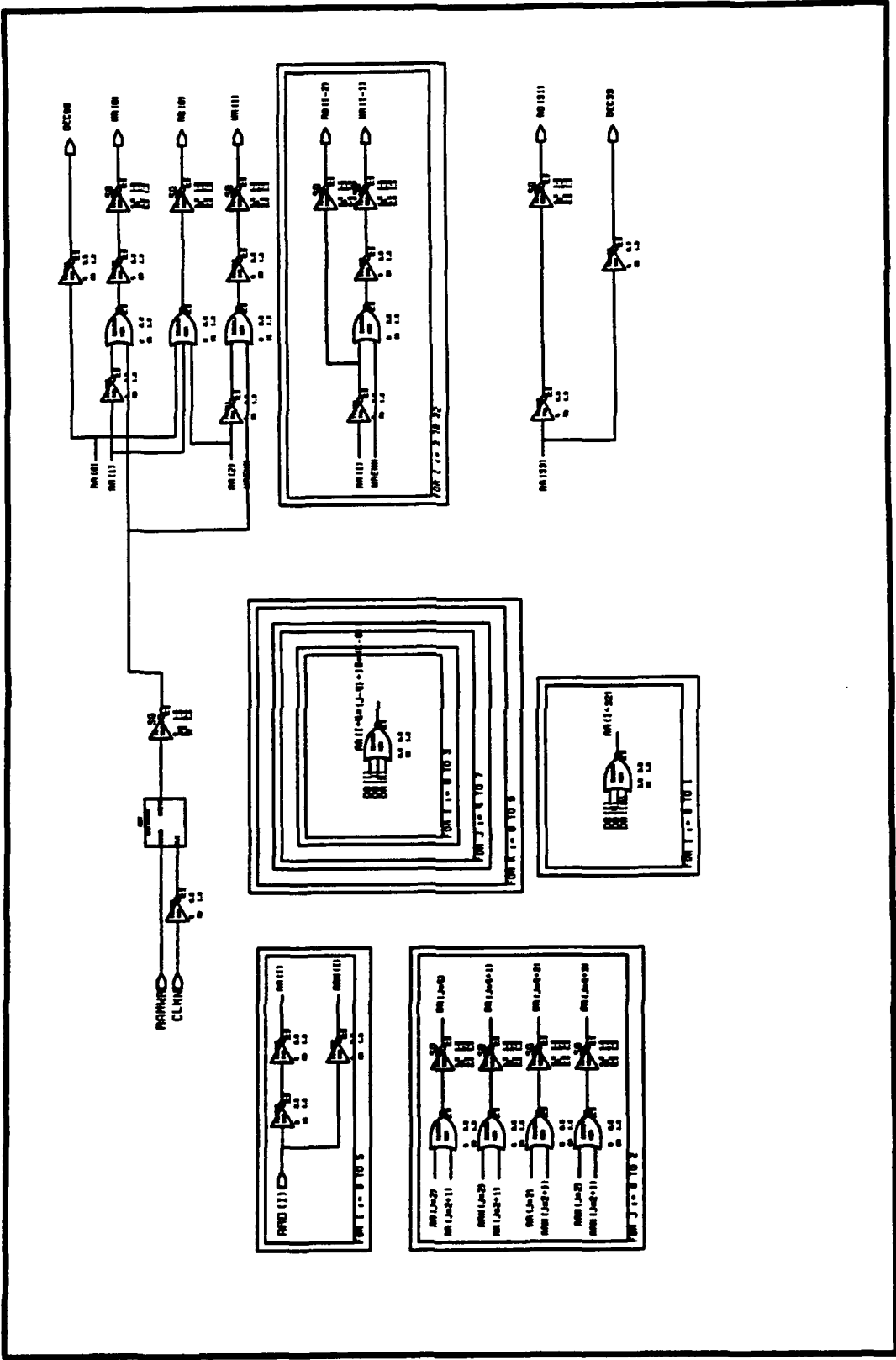


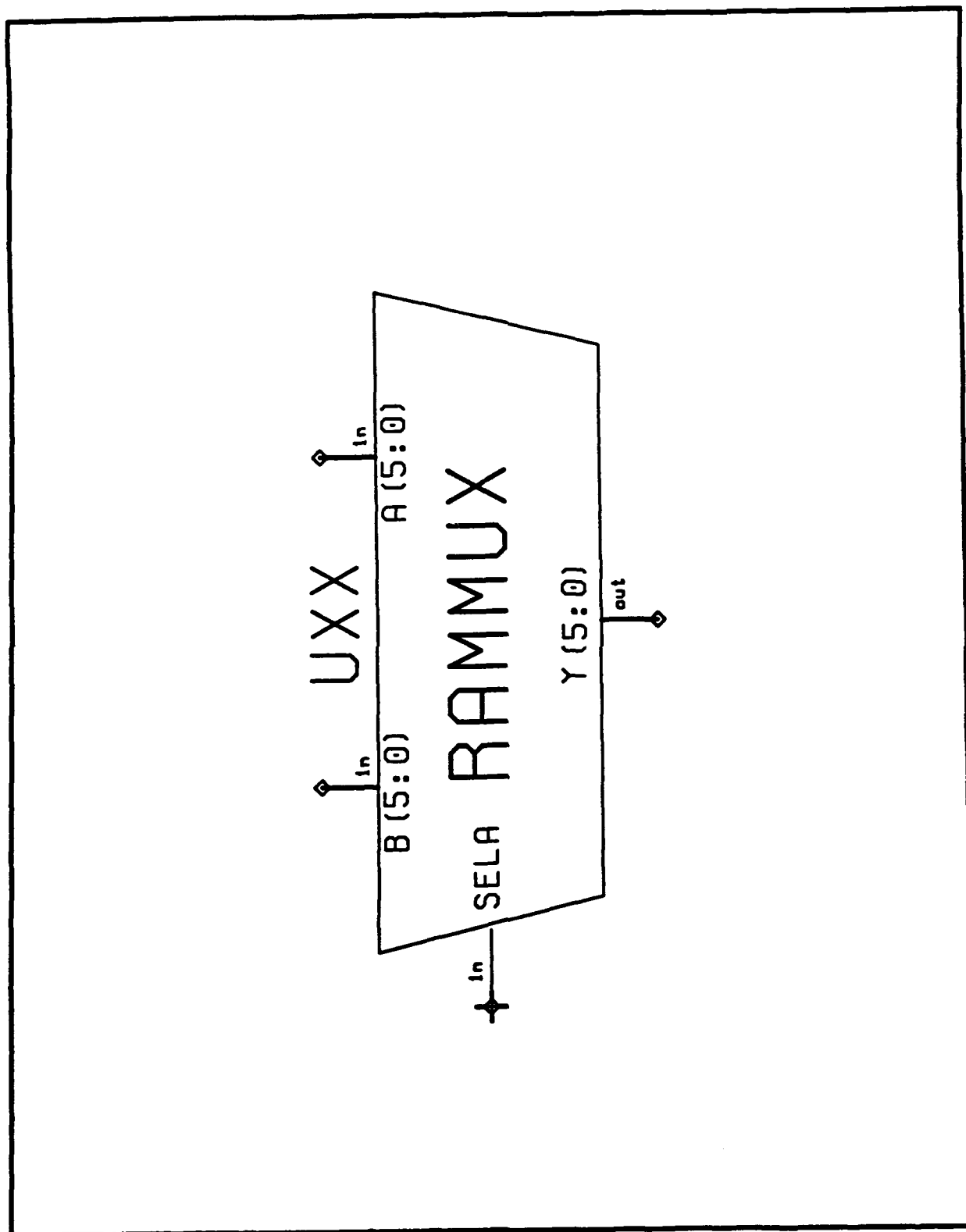














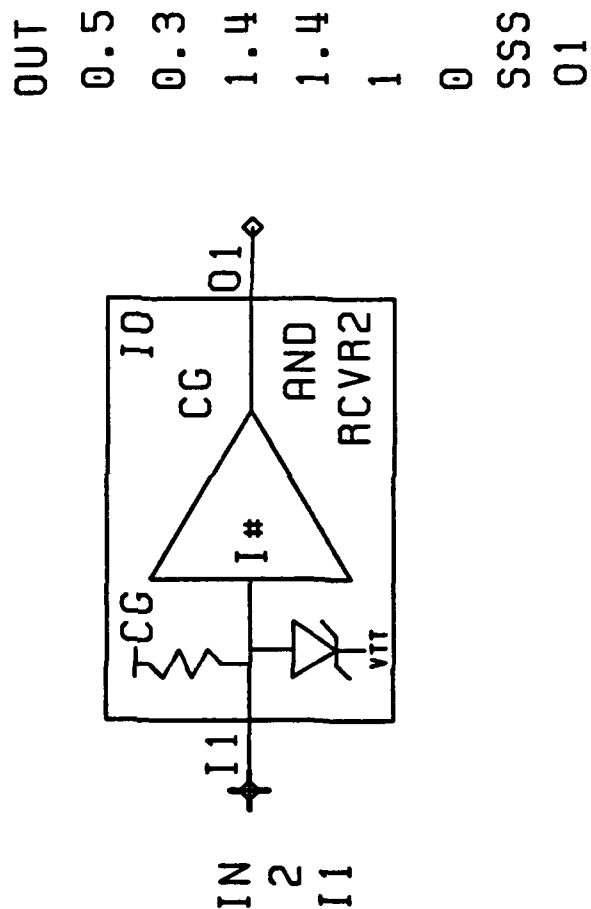
VITESSE GAAS CELL LIBRARY  
Version 0.8

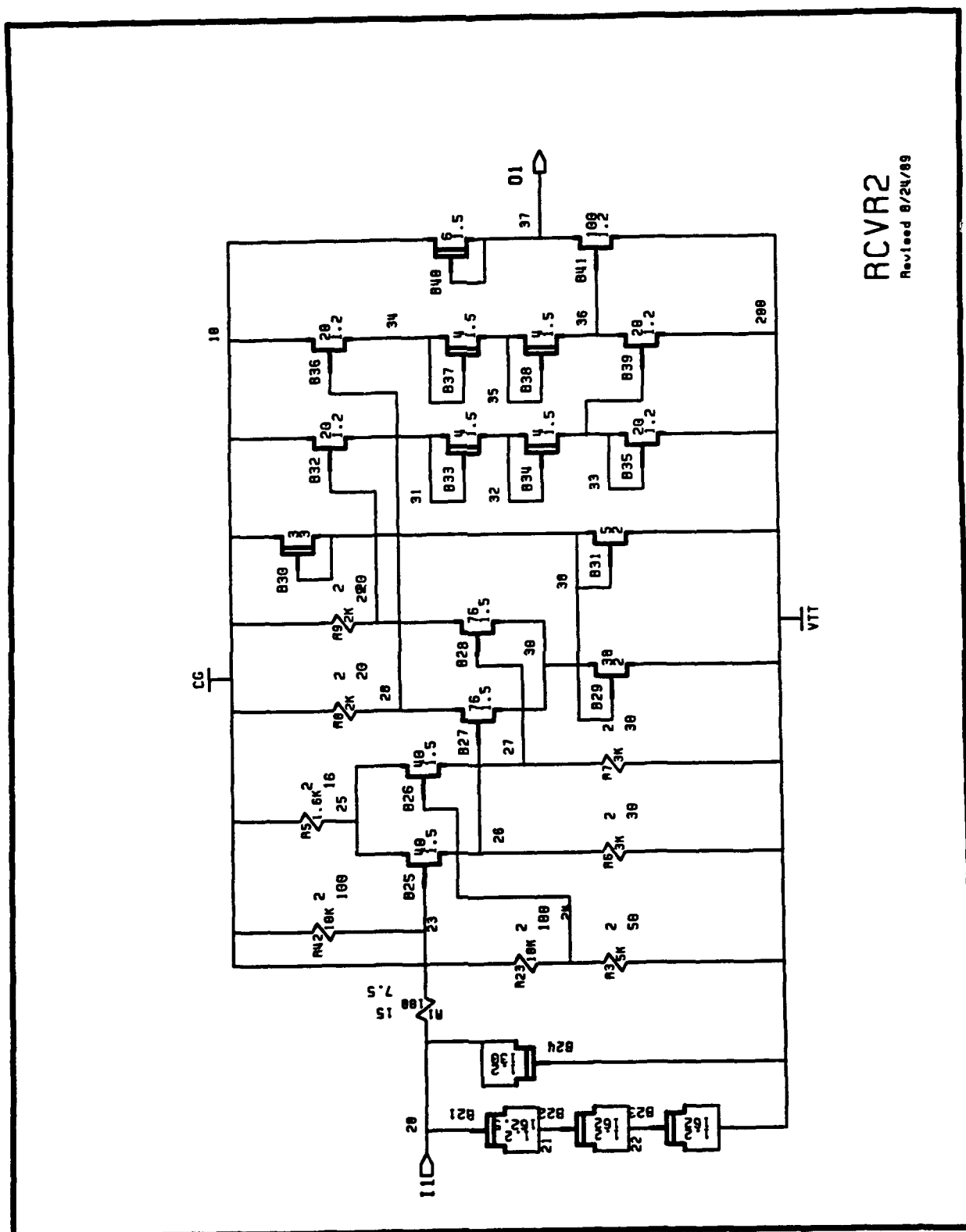
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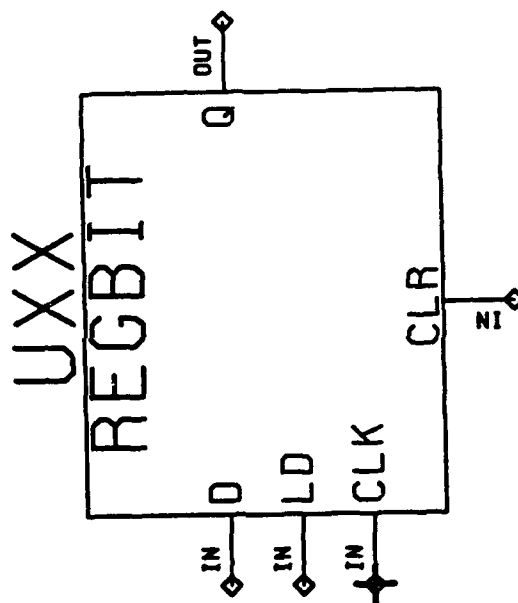
RCVR2

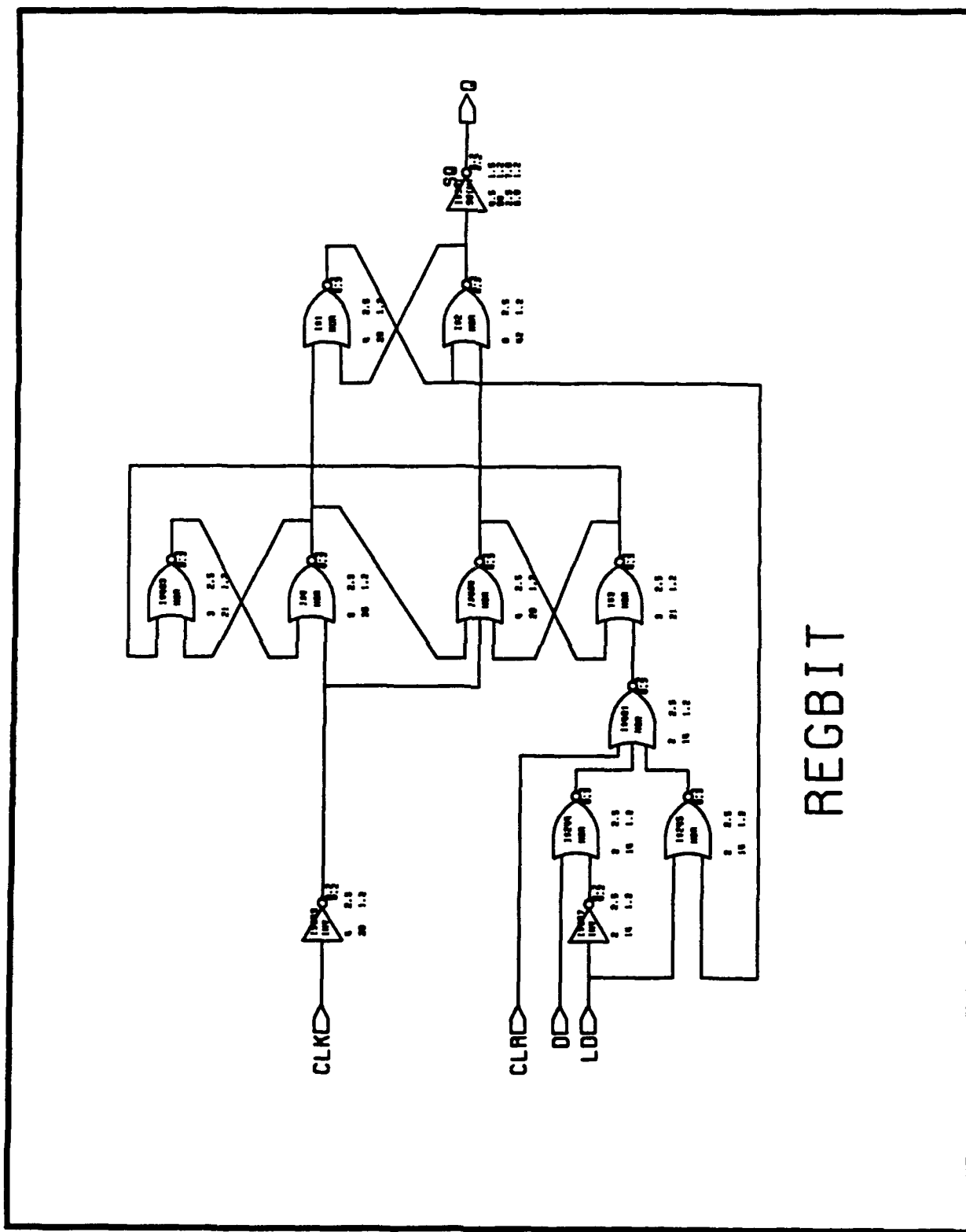
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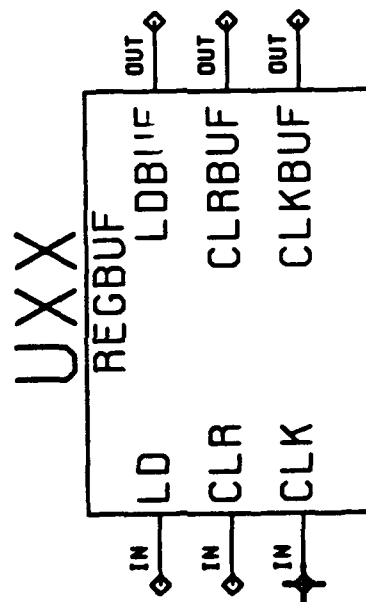
LOW POWER 2 VOLT RECEIVER WITH PAD



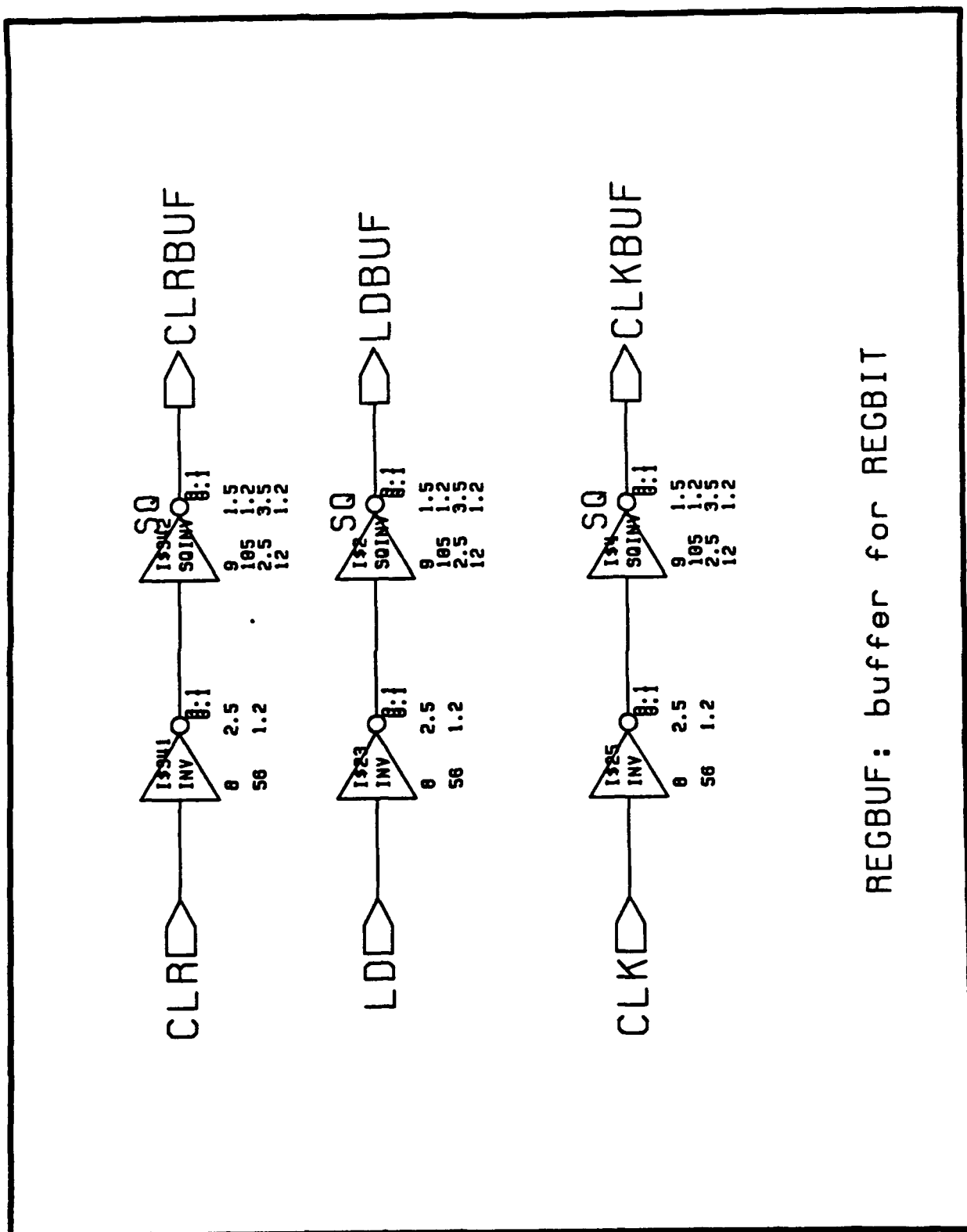


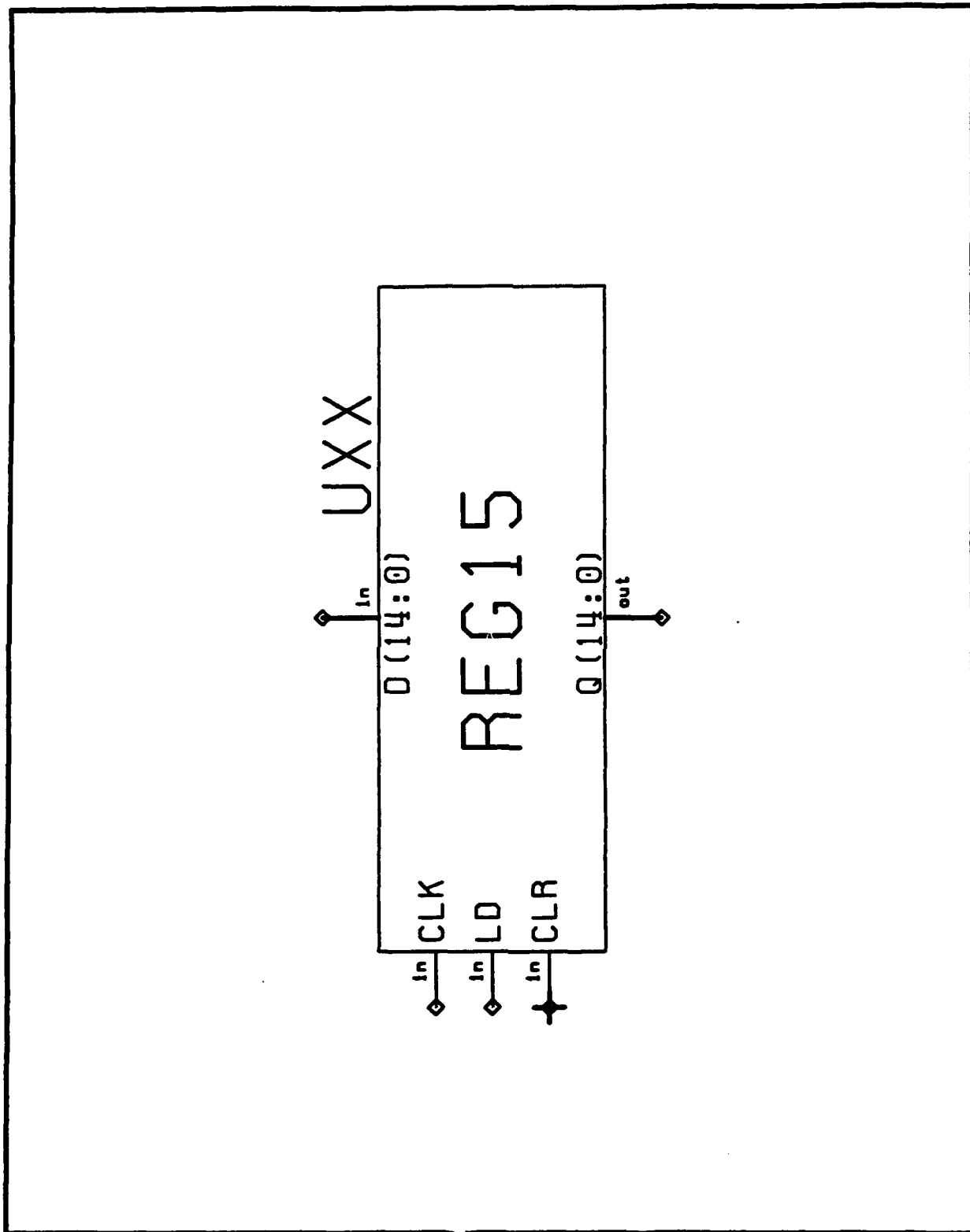


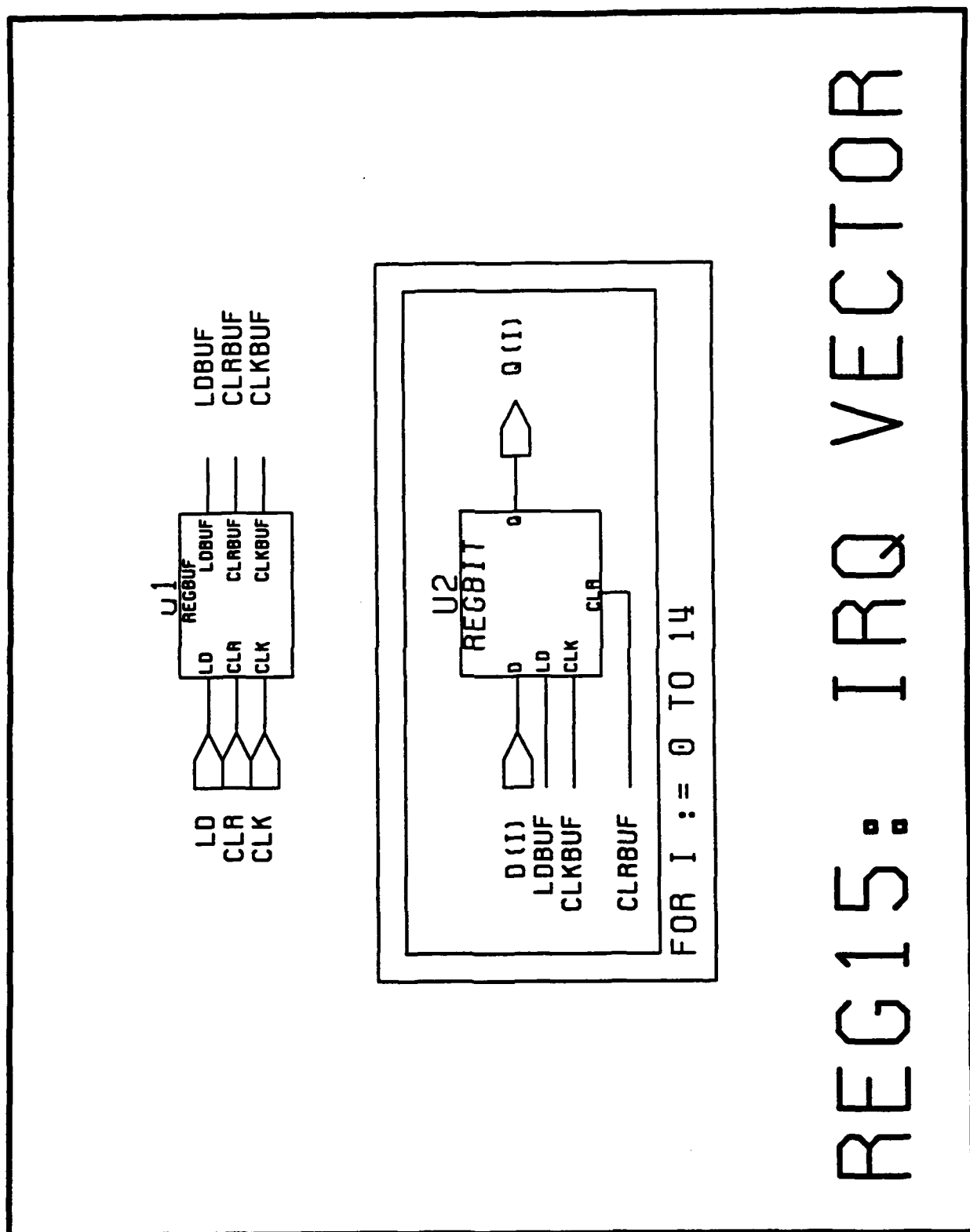


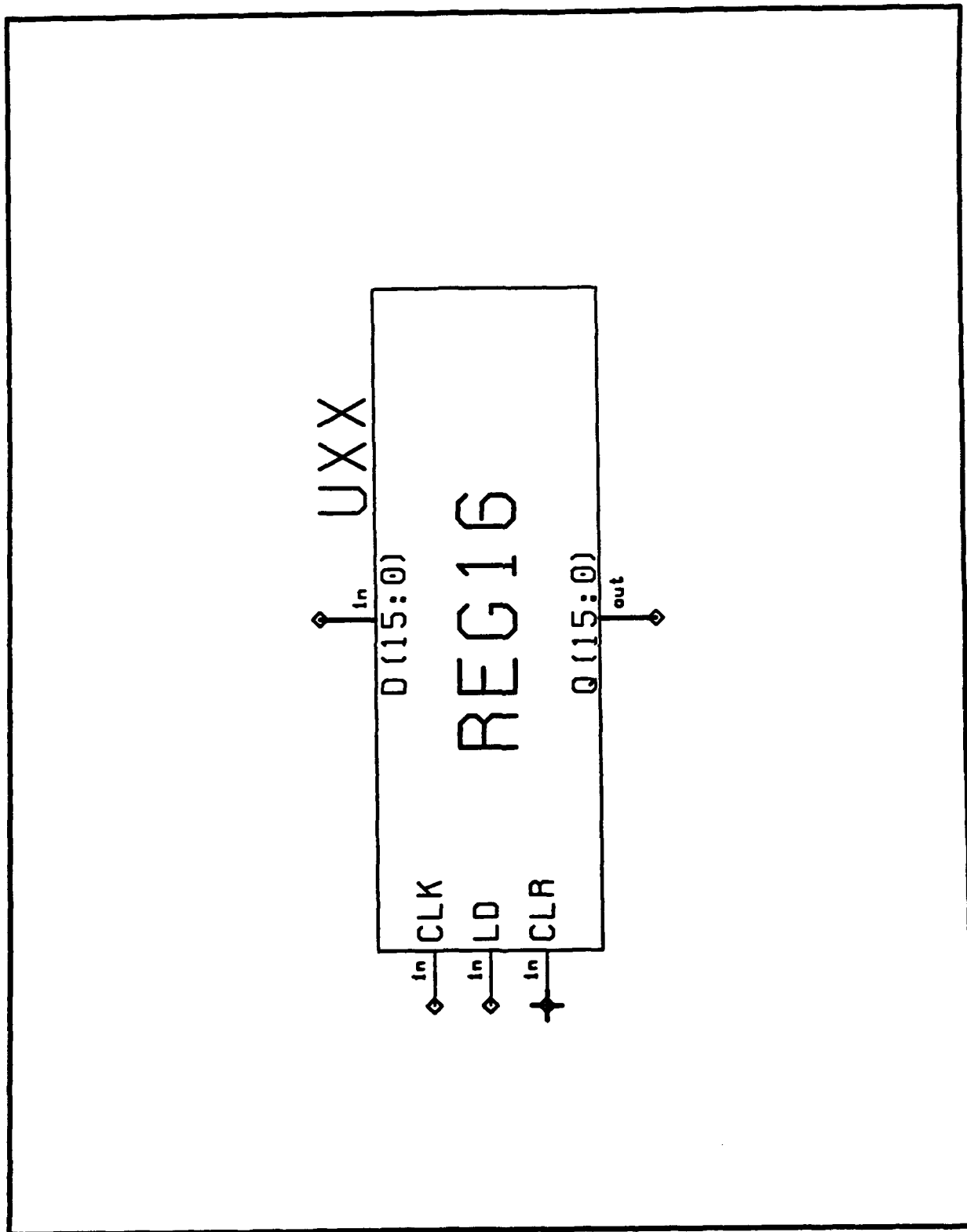


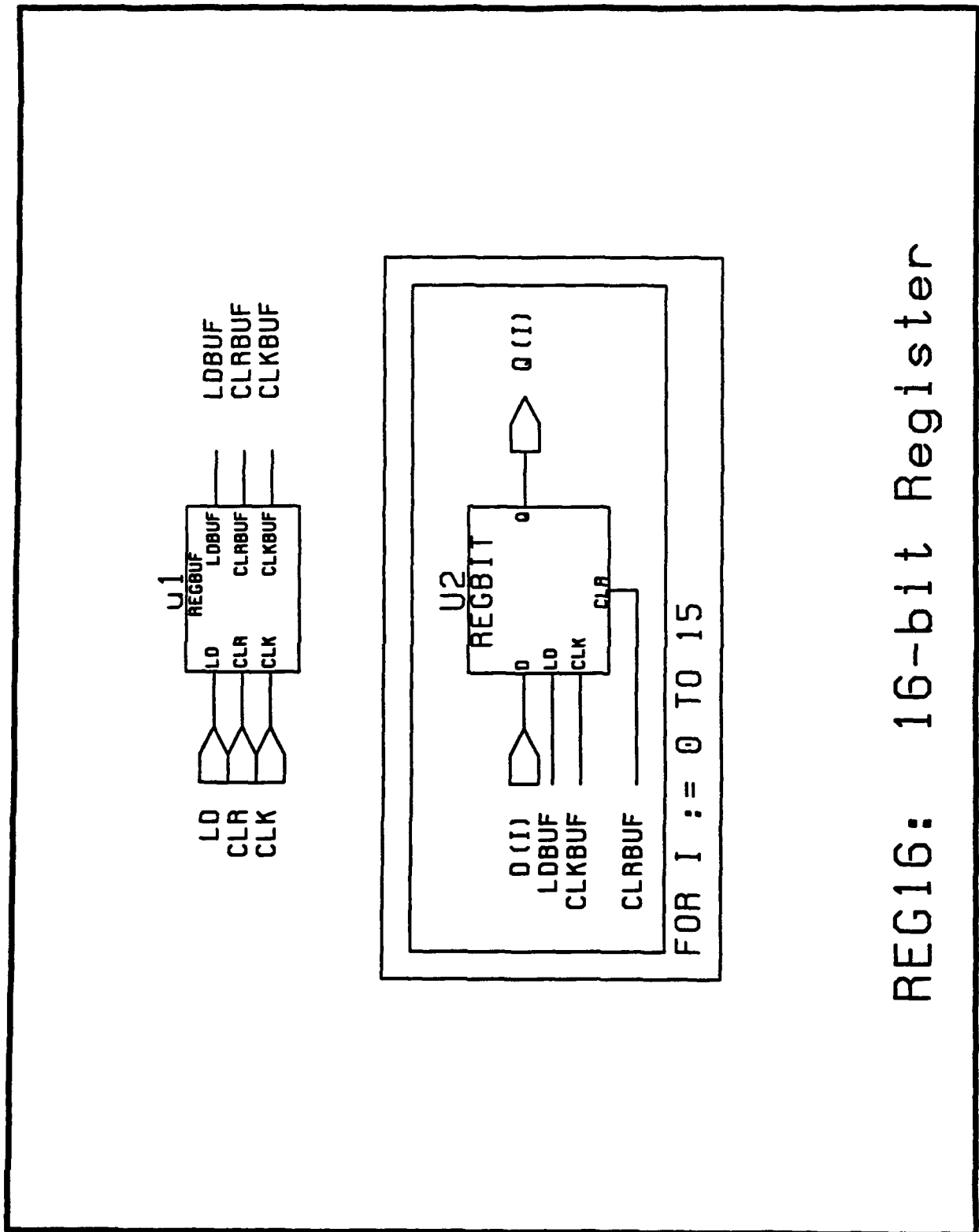




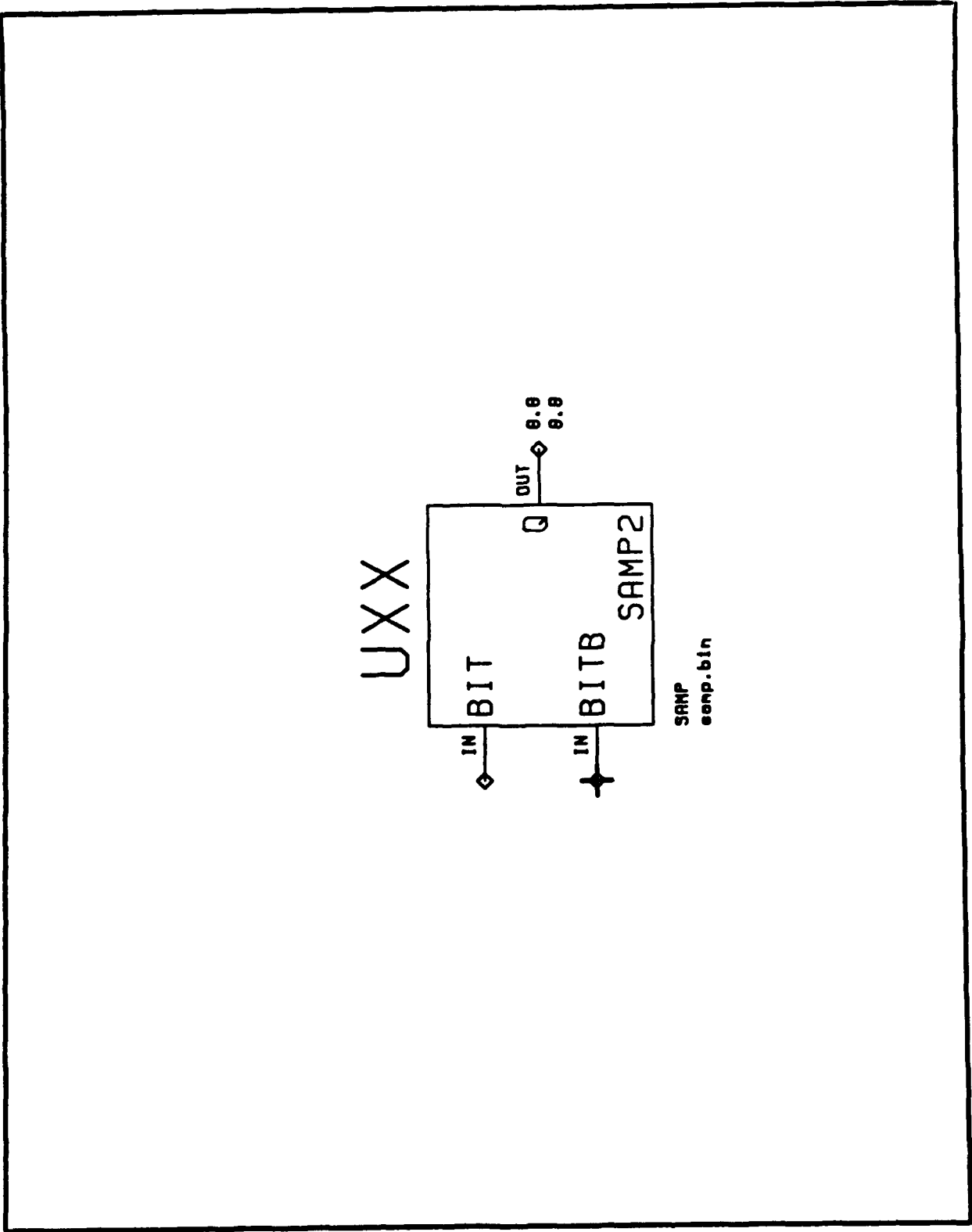


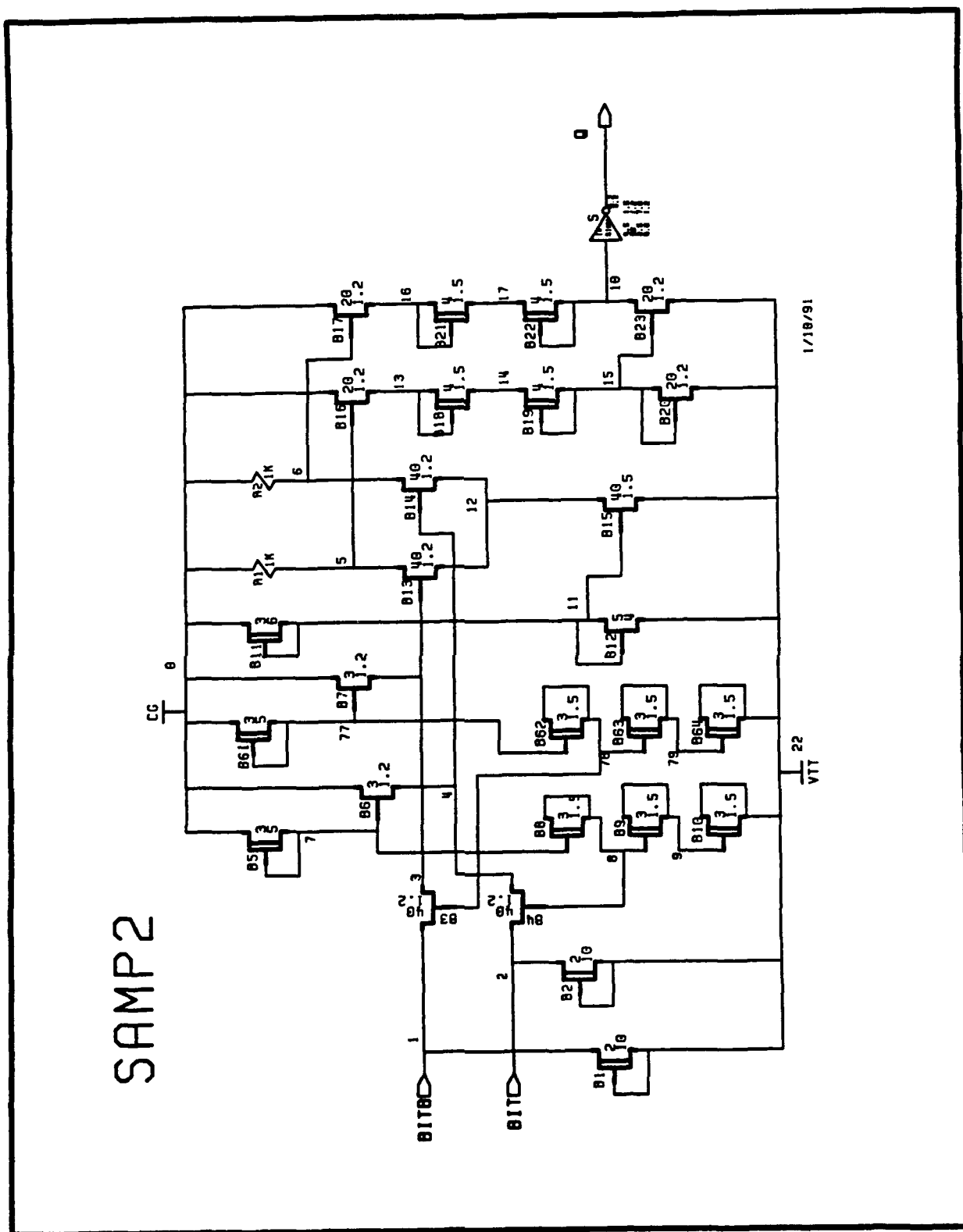


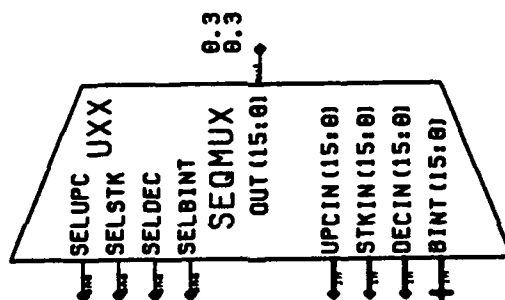




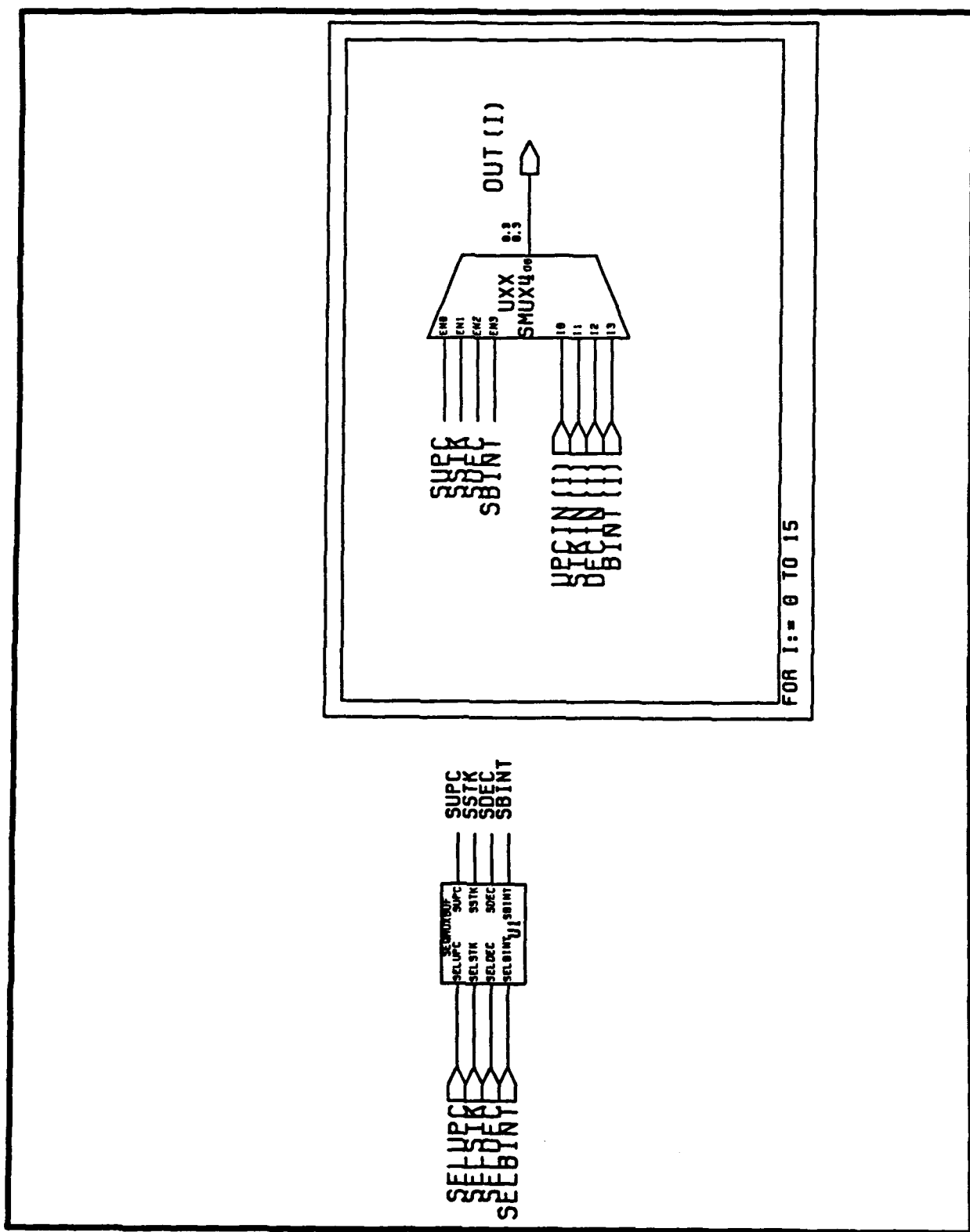
REG16: 16-bit Register

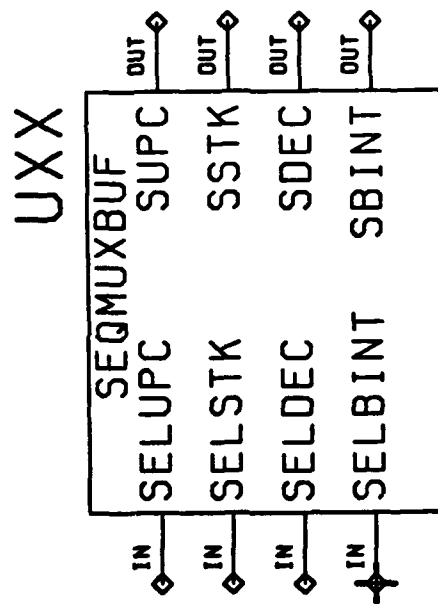


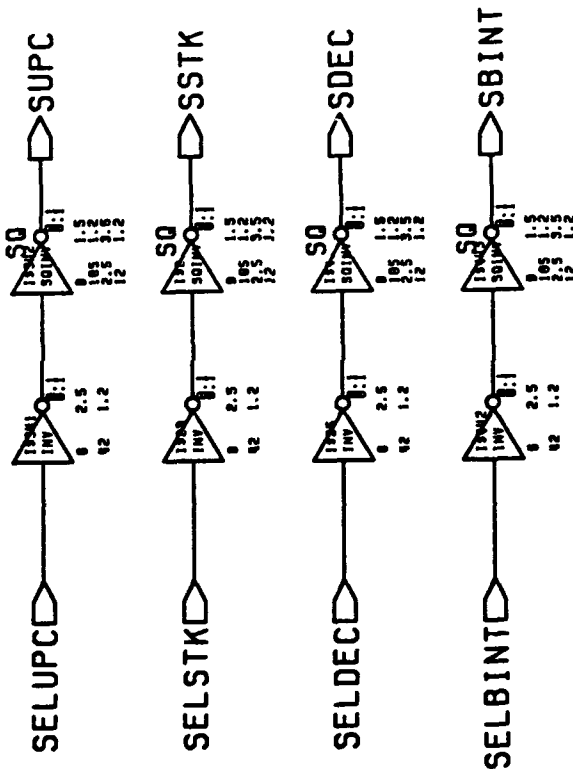


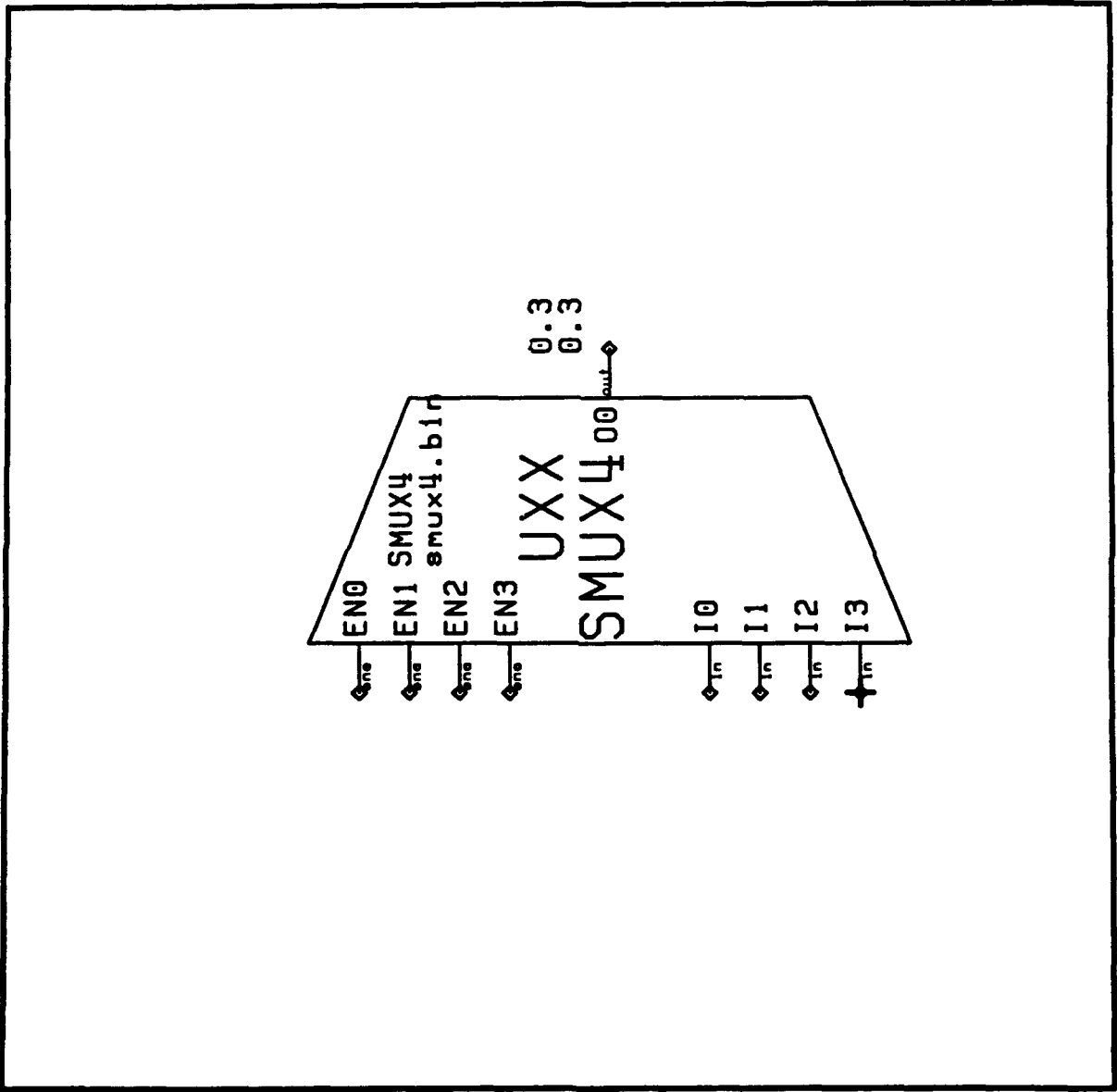


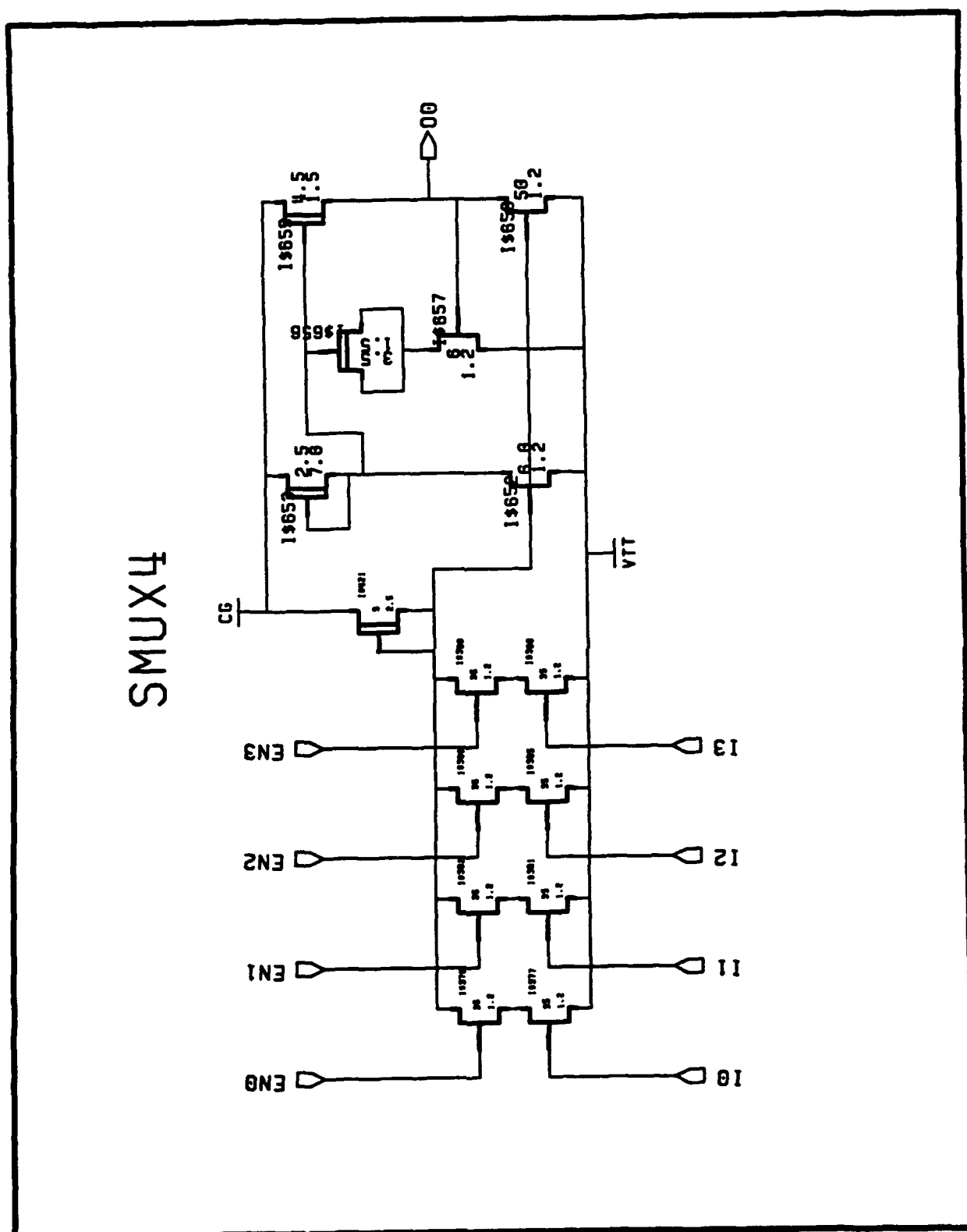


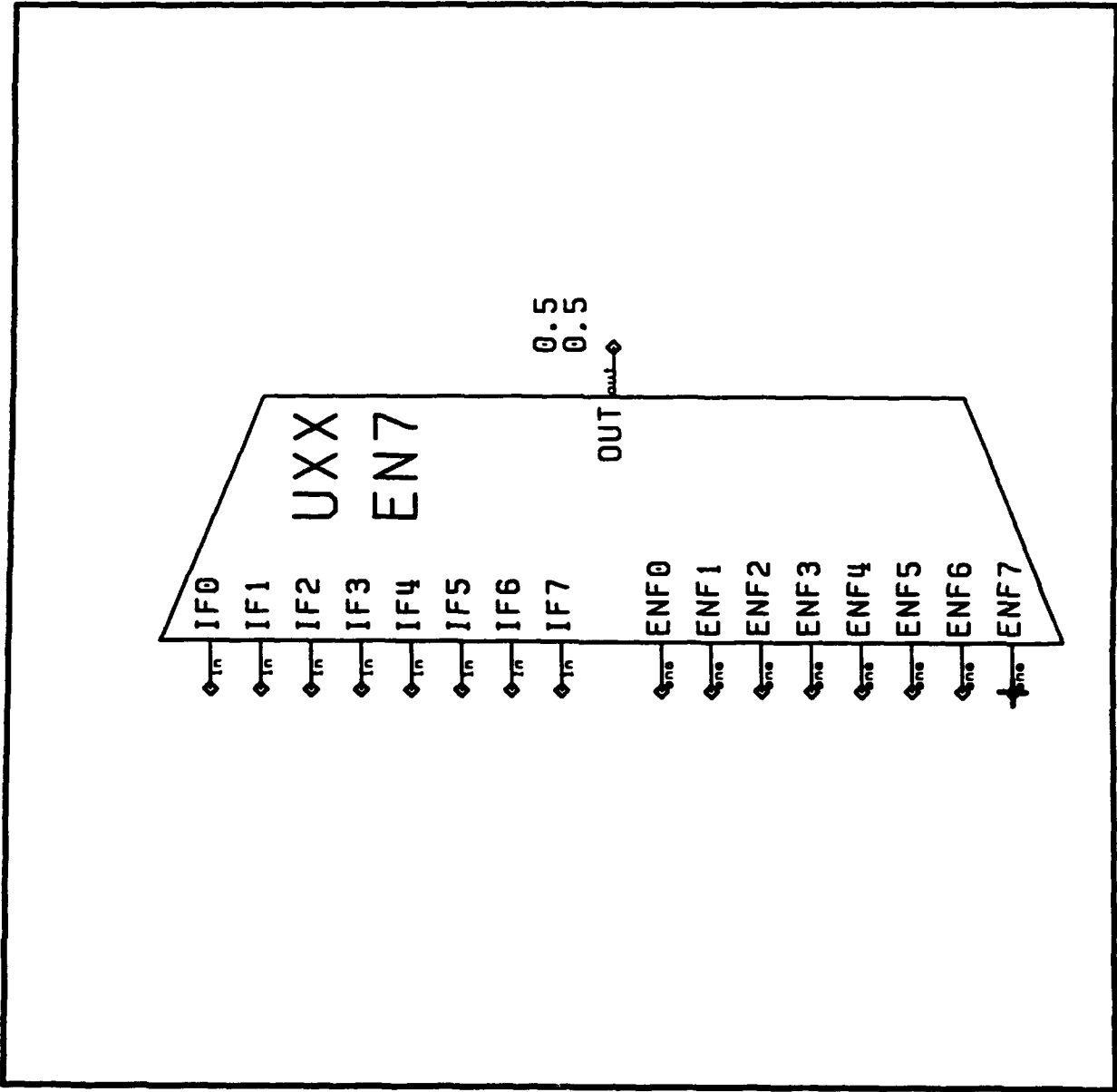


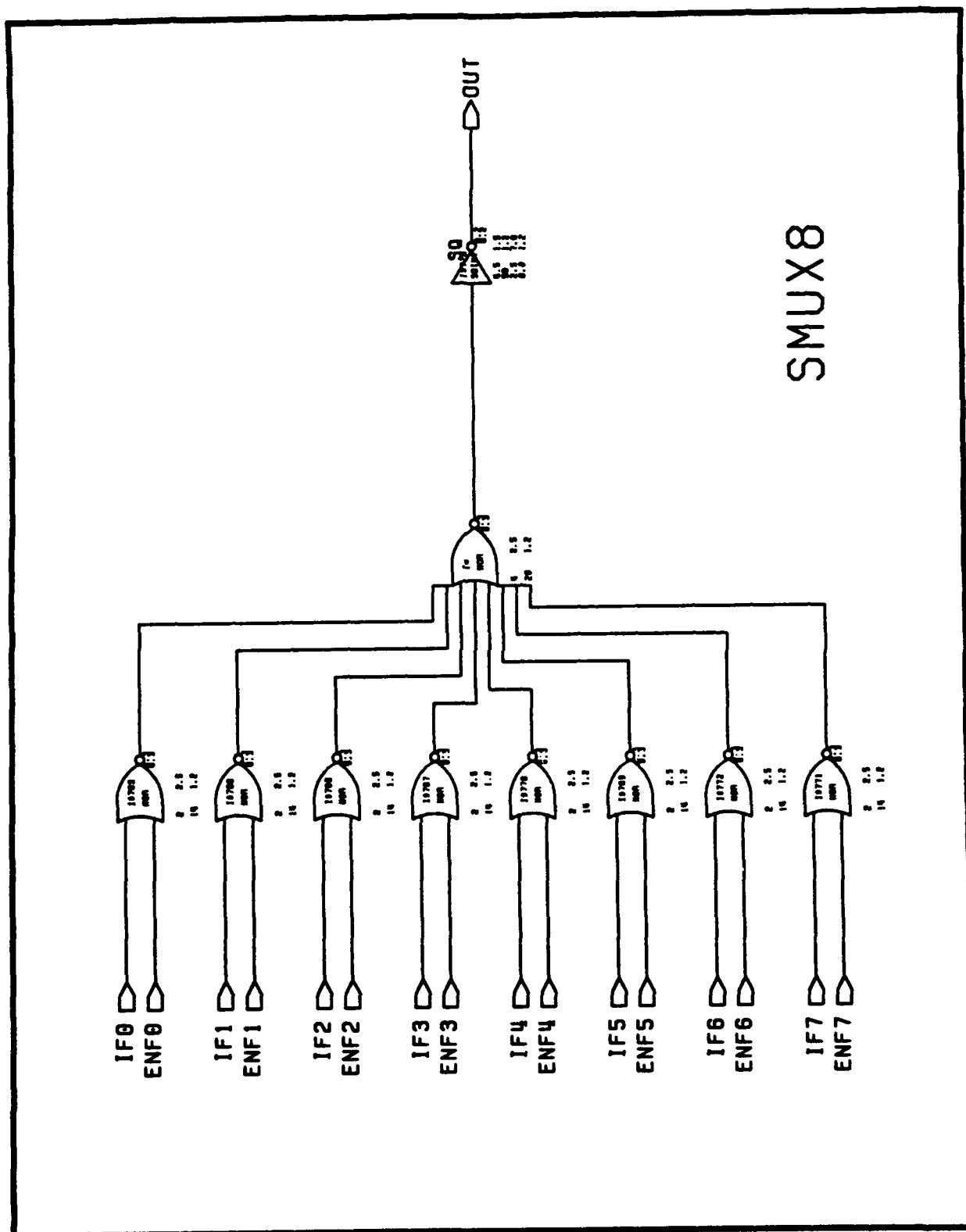


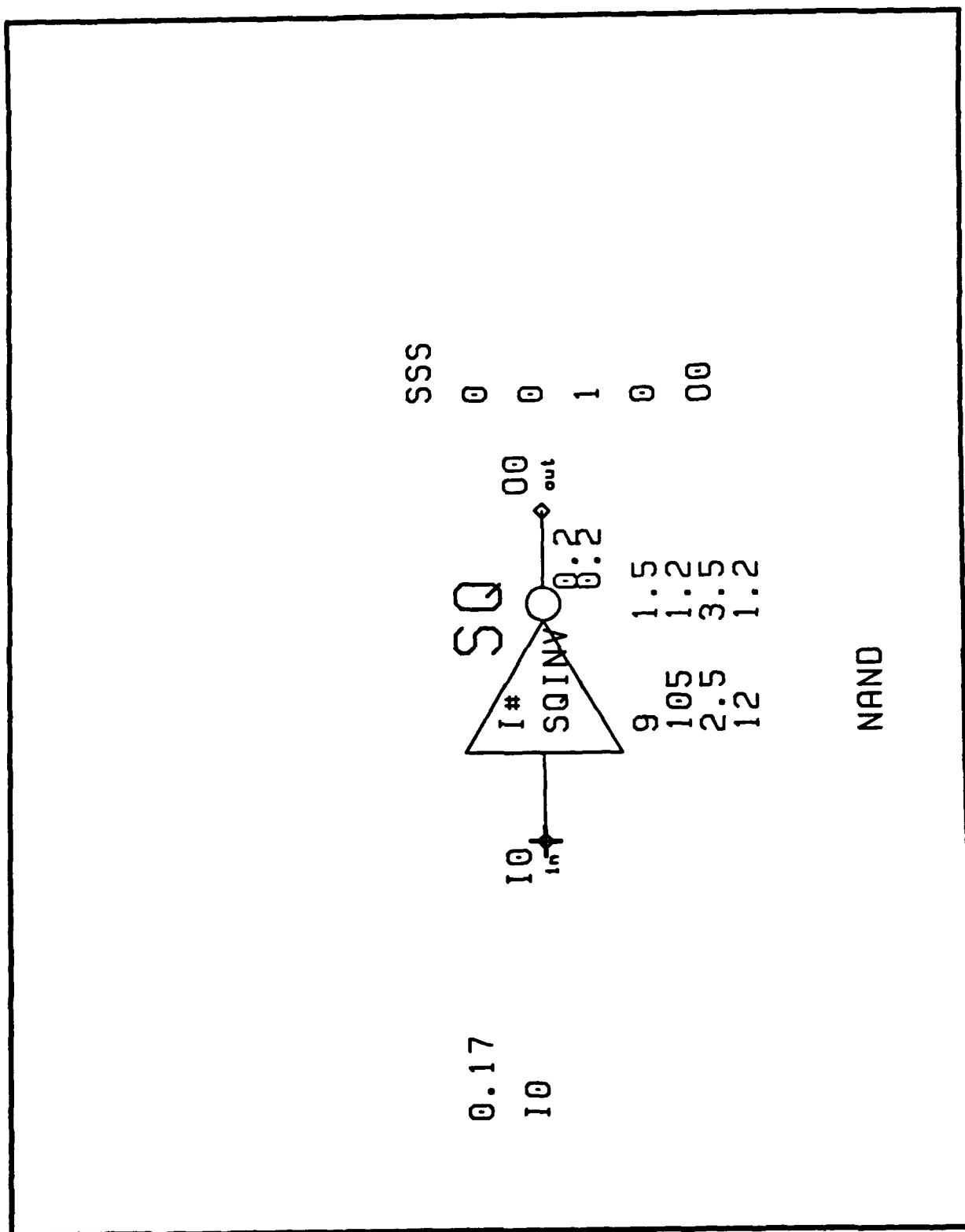




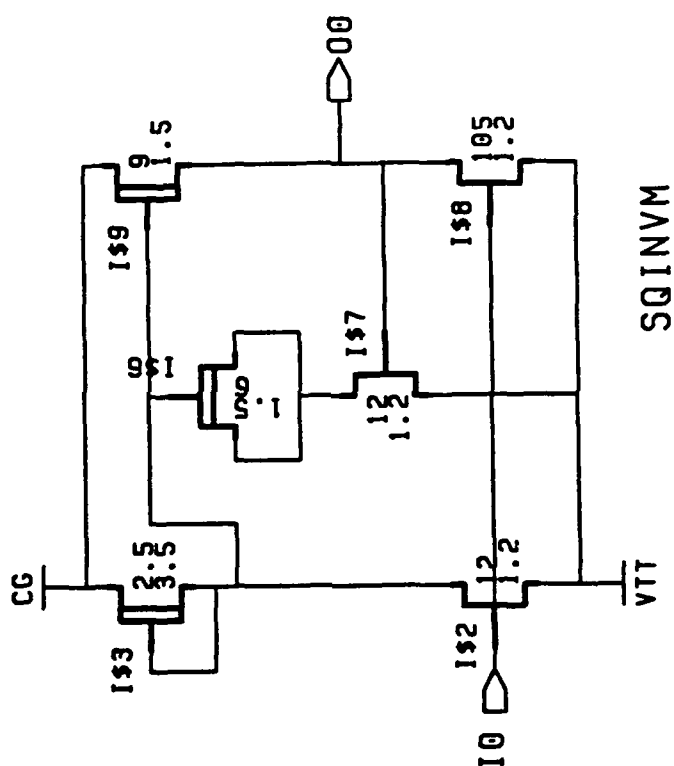


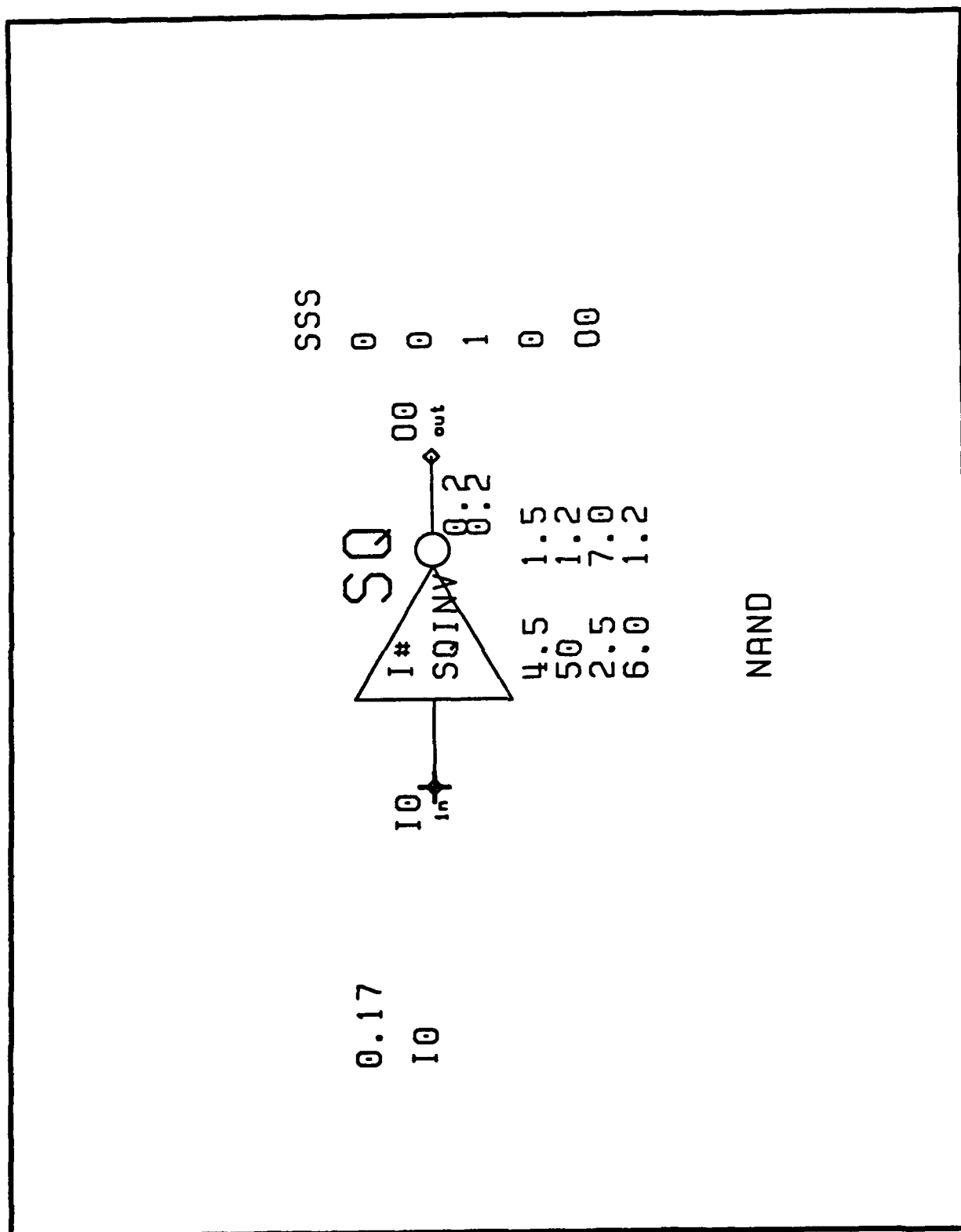


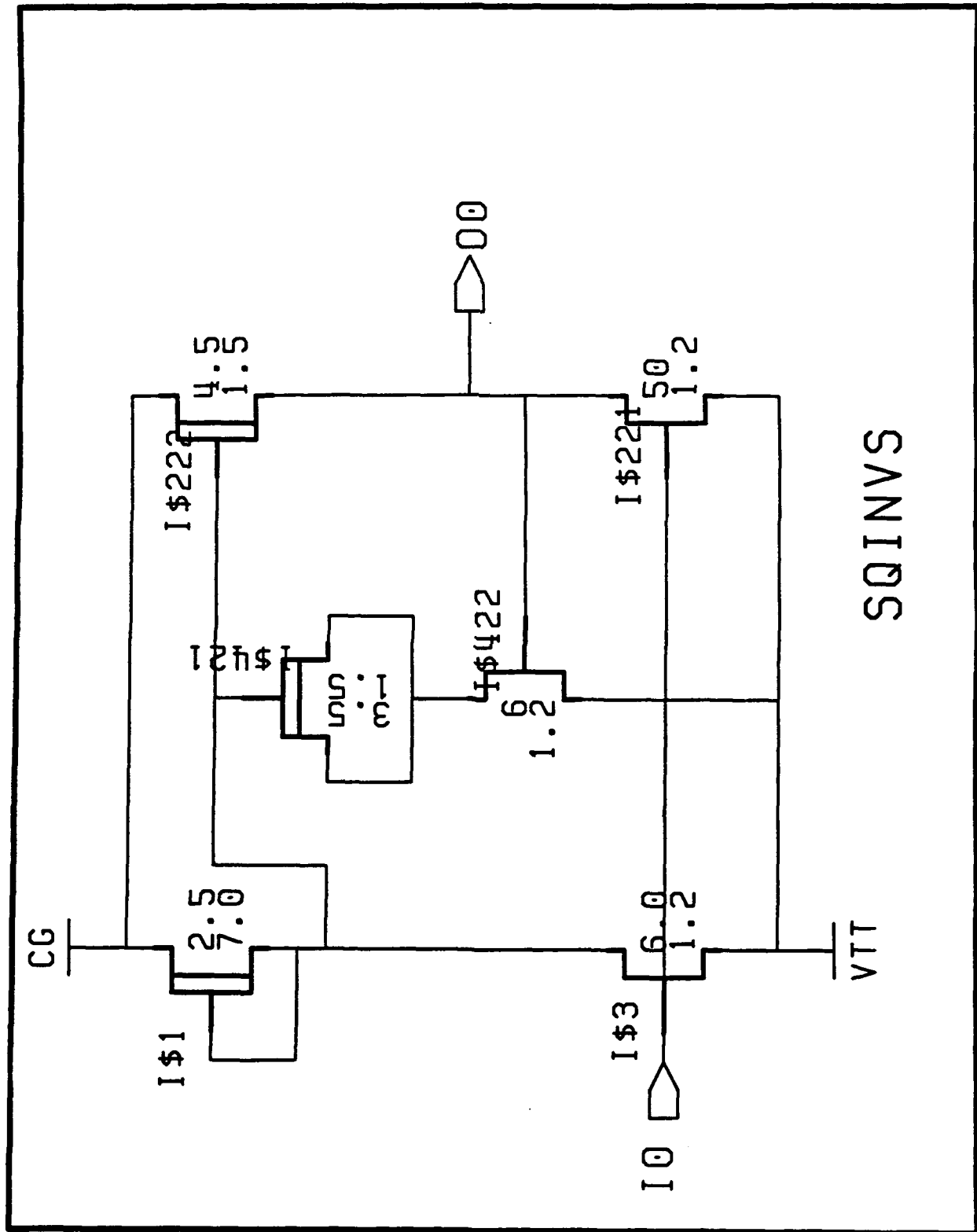


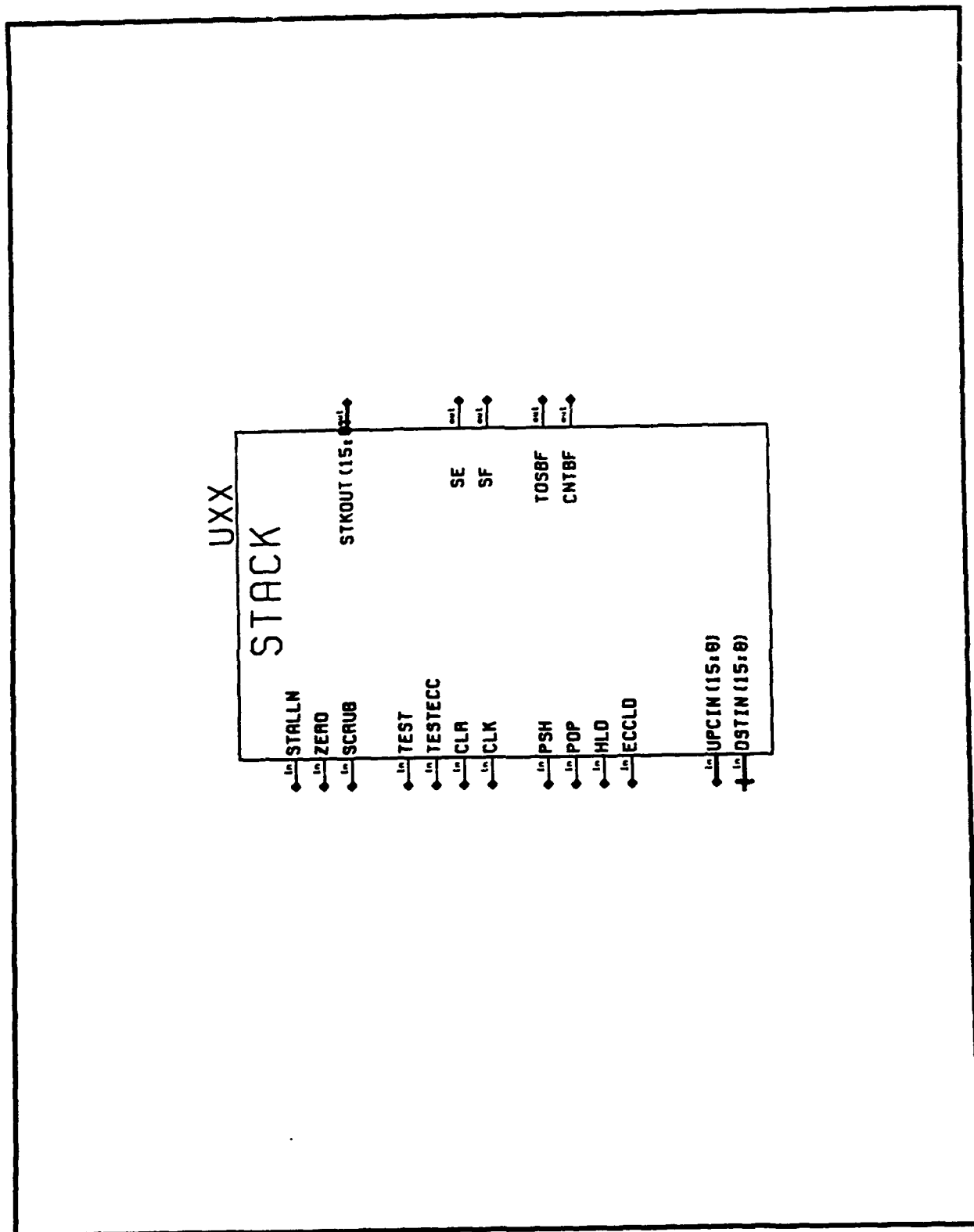




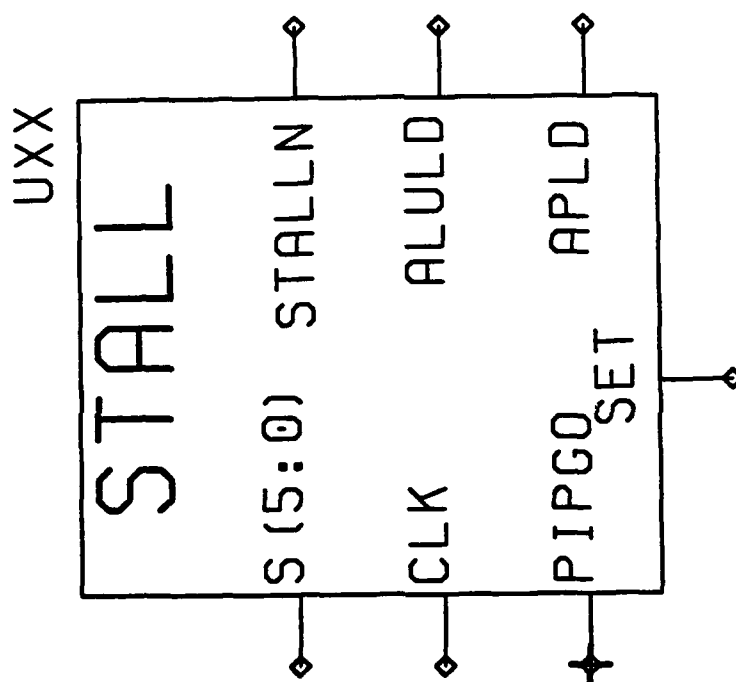


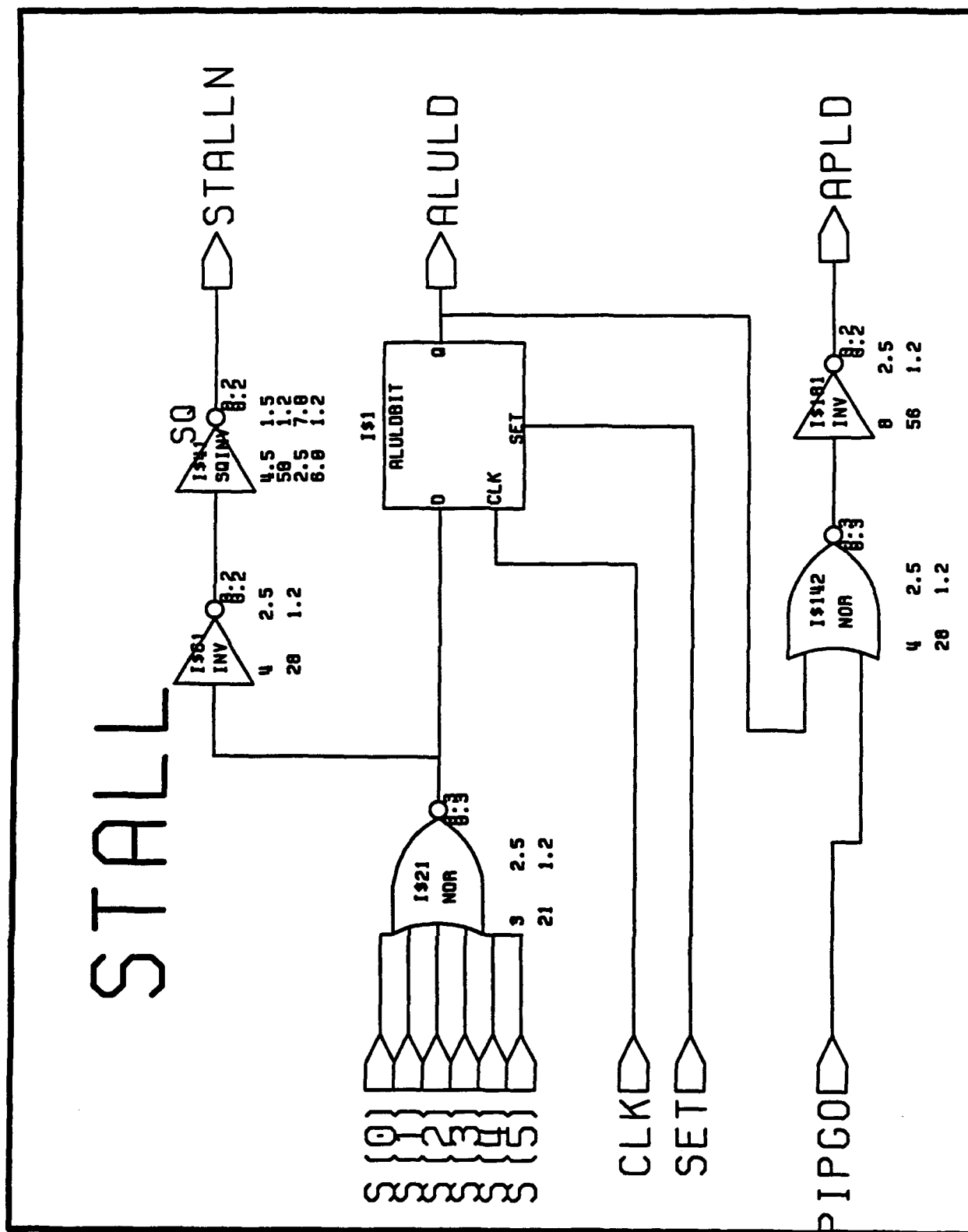


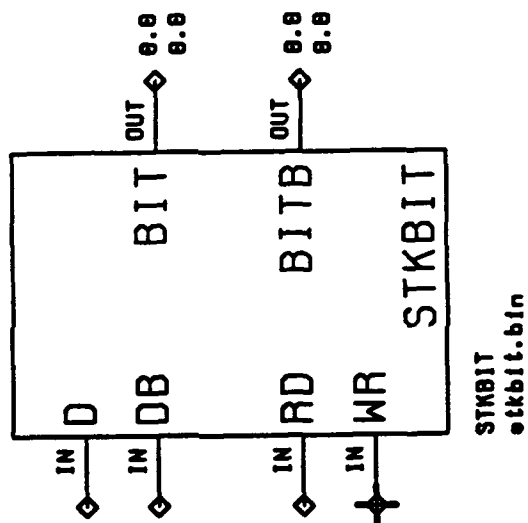




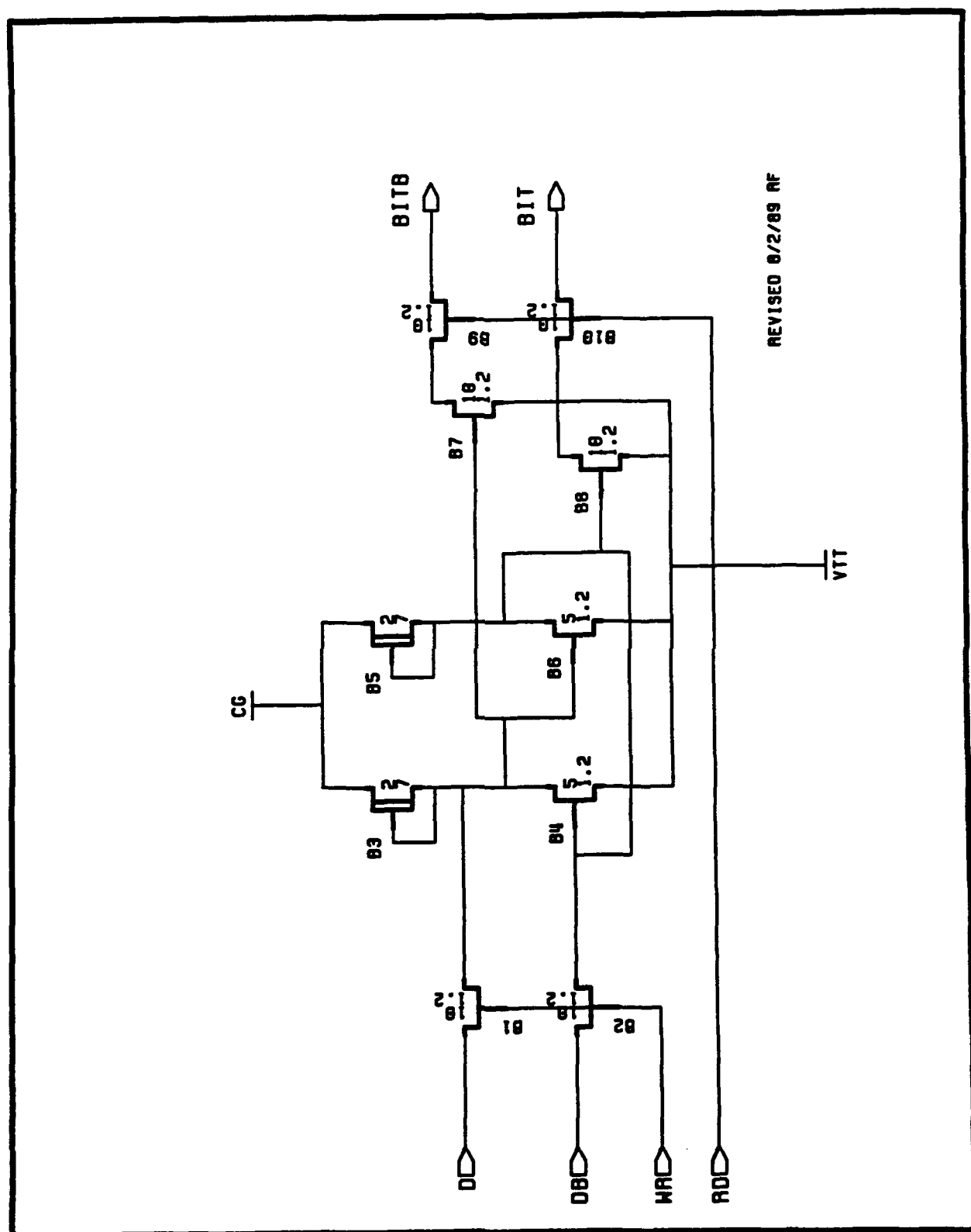


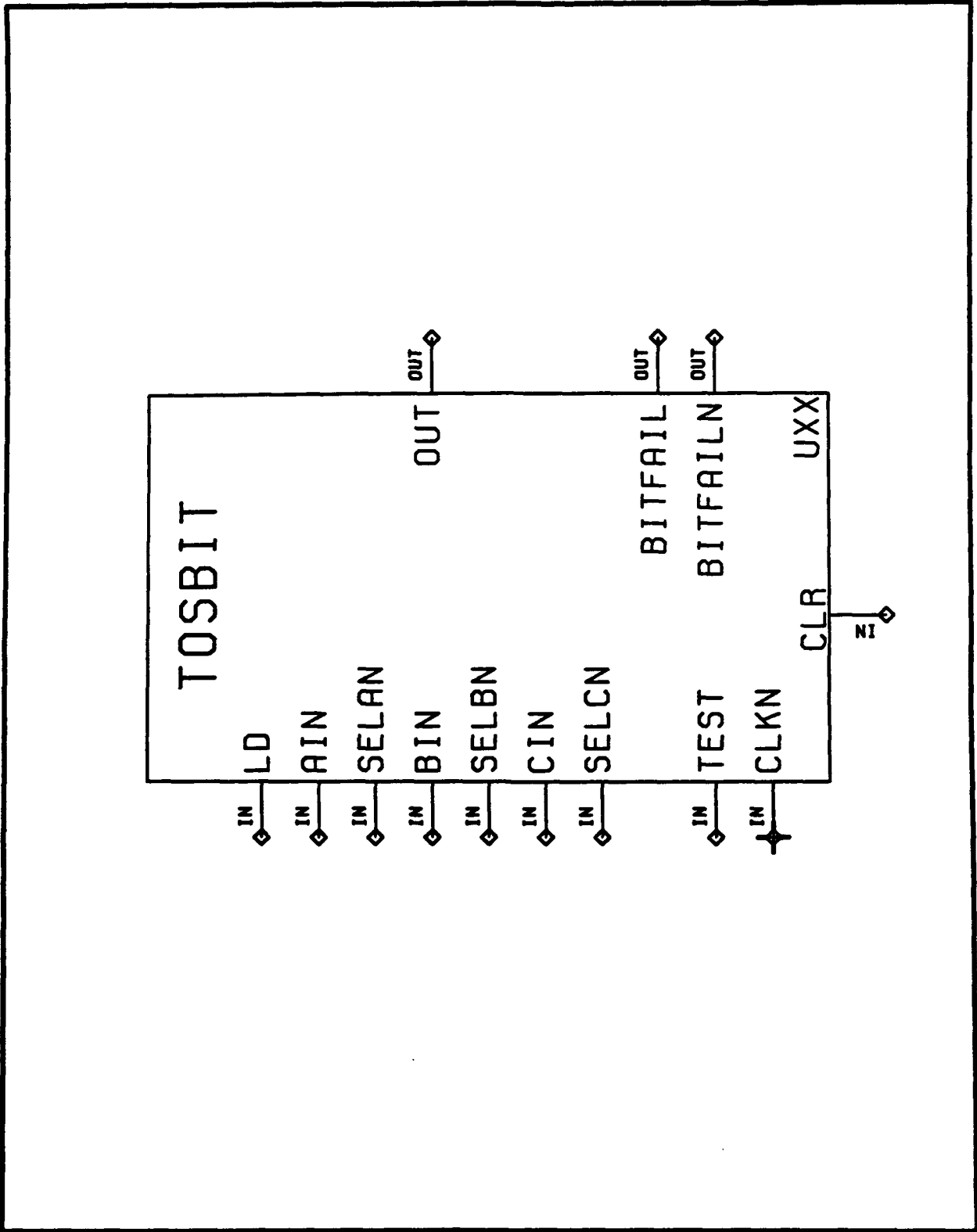


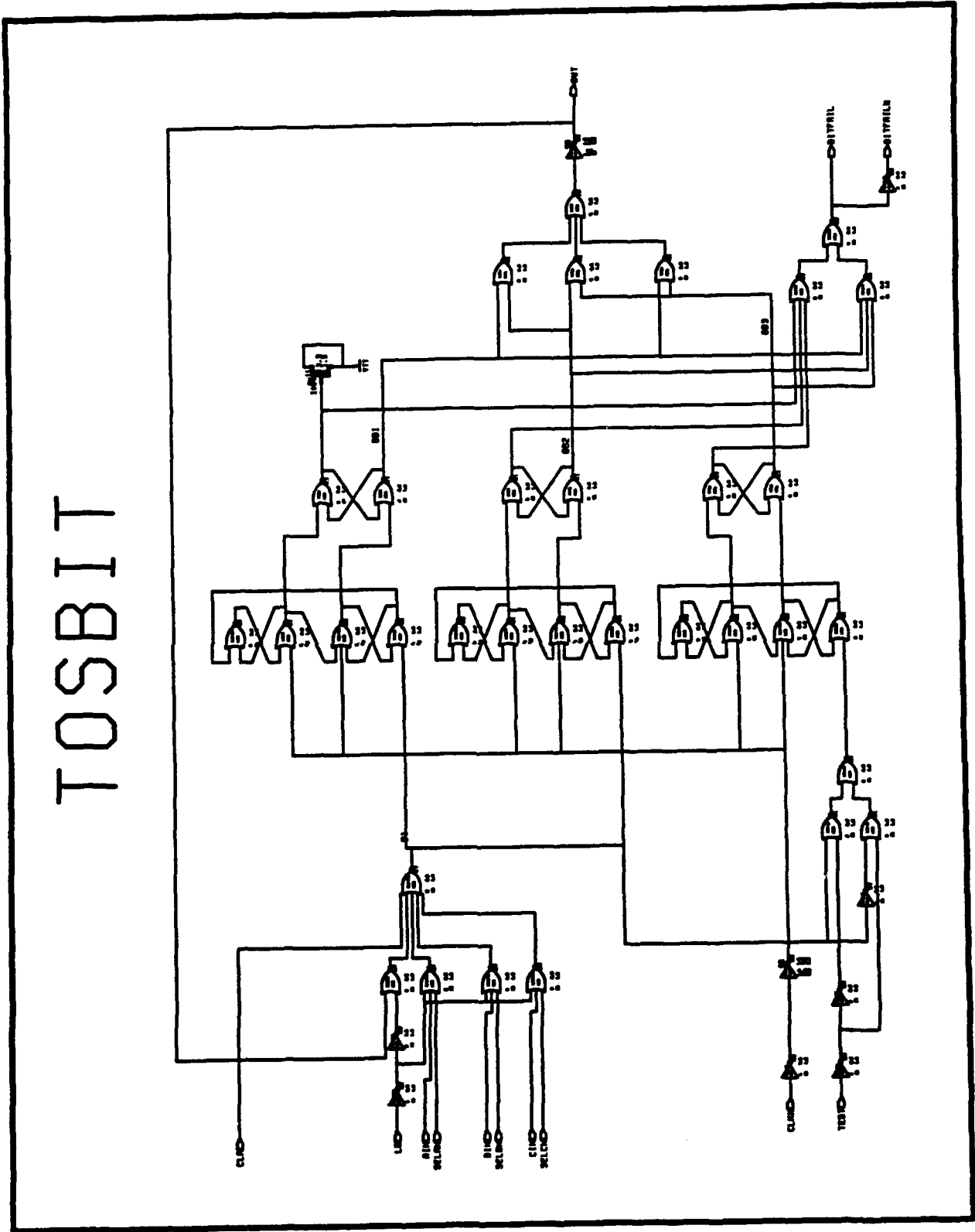


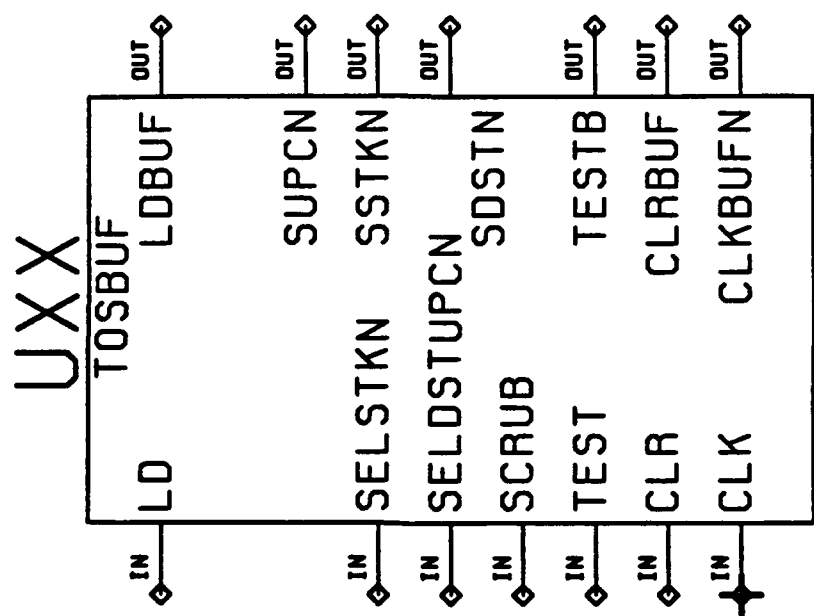


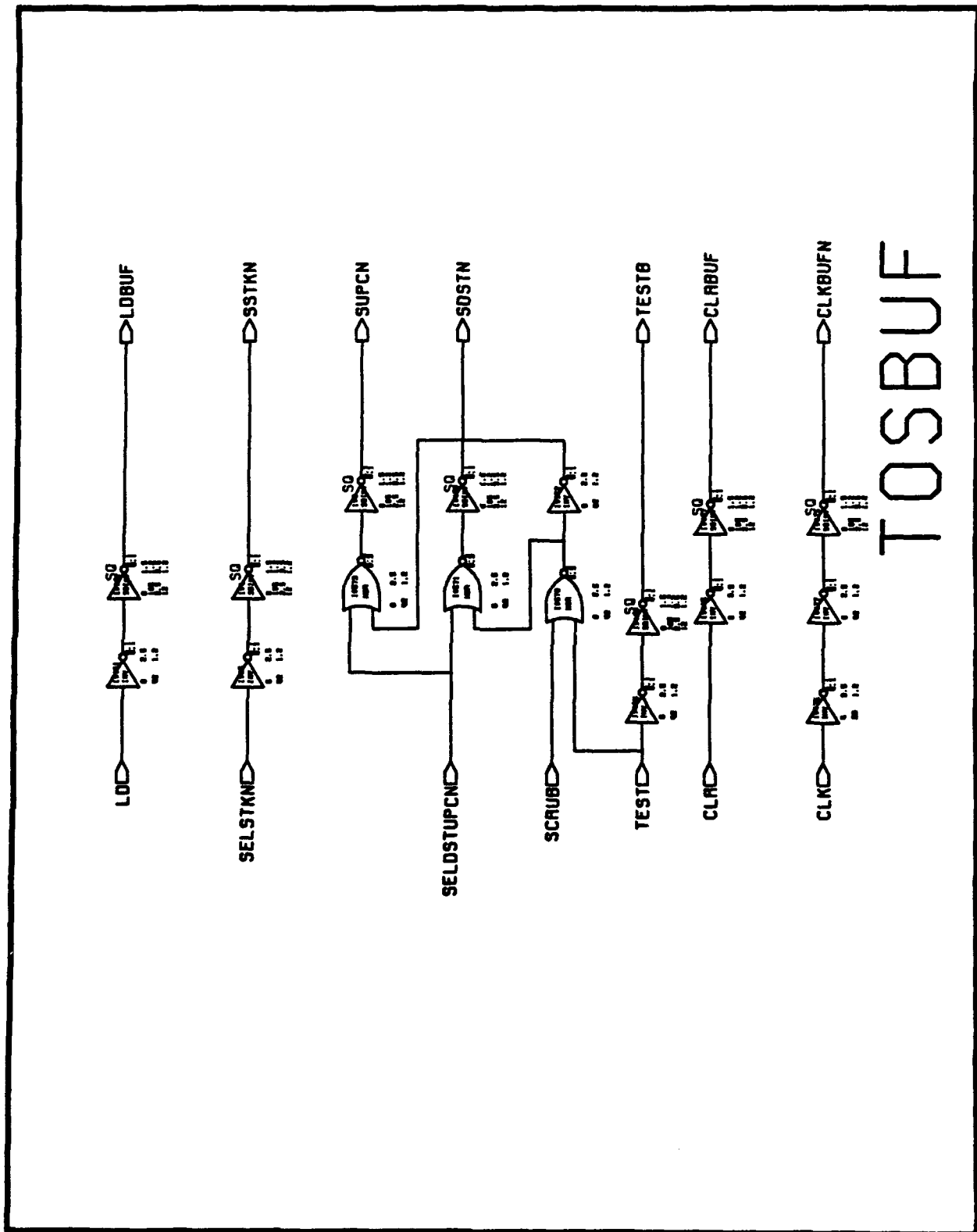


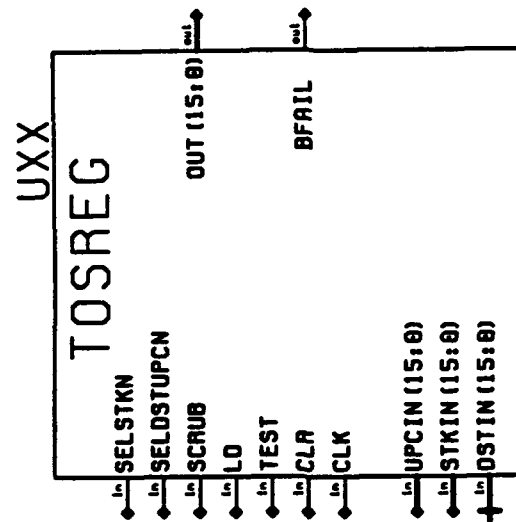


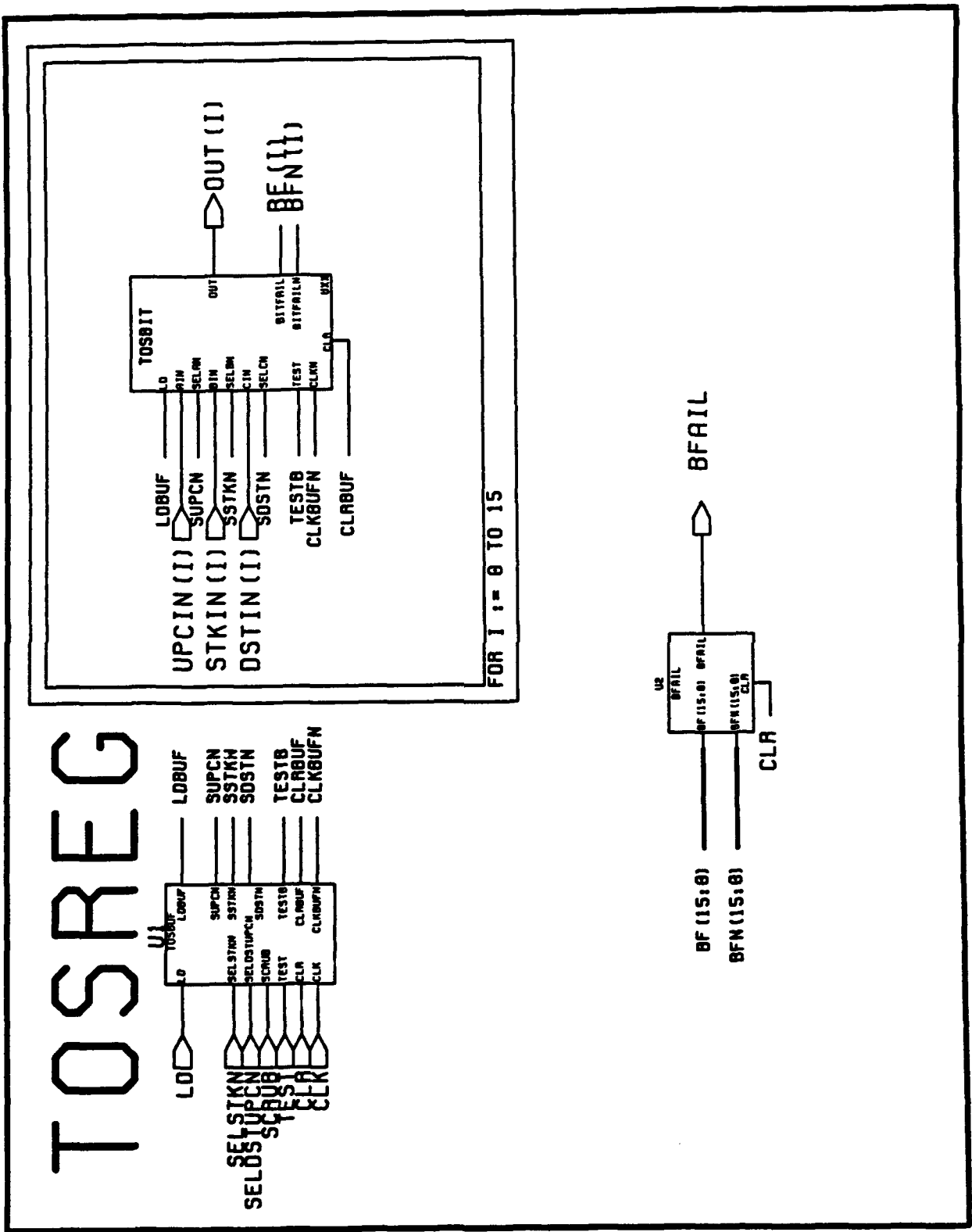


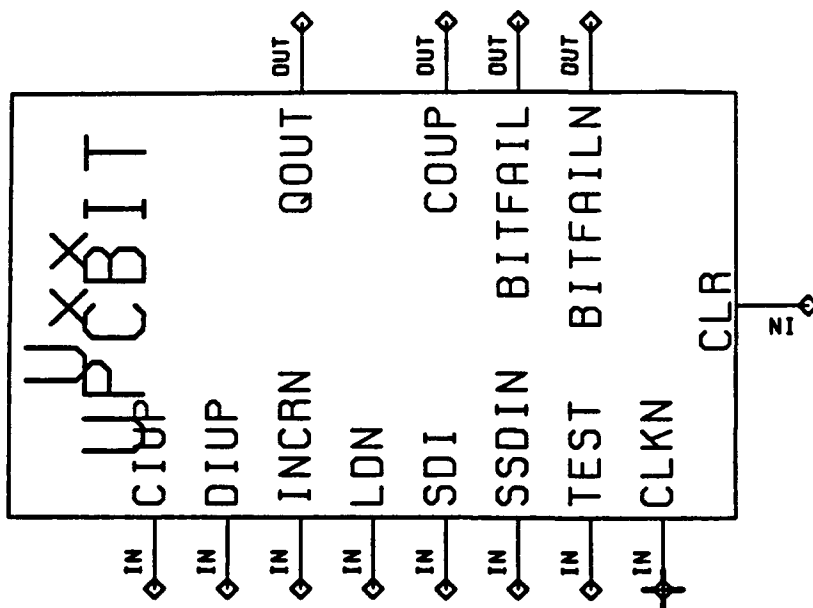




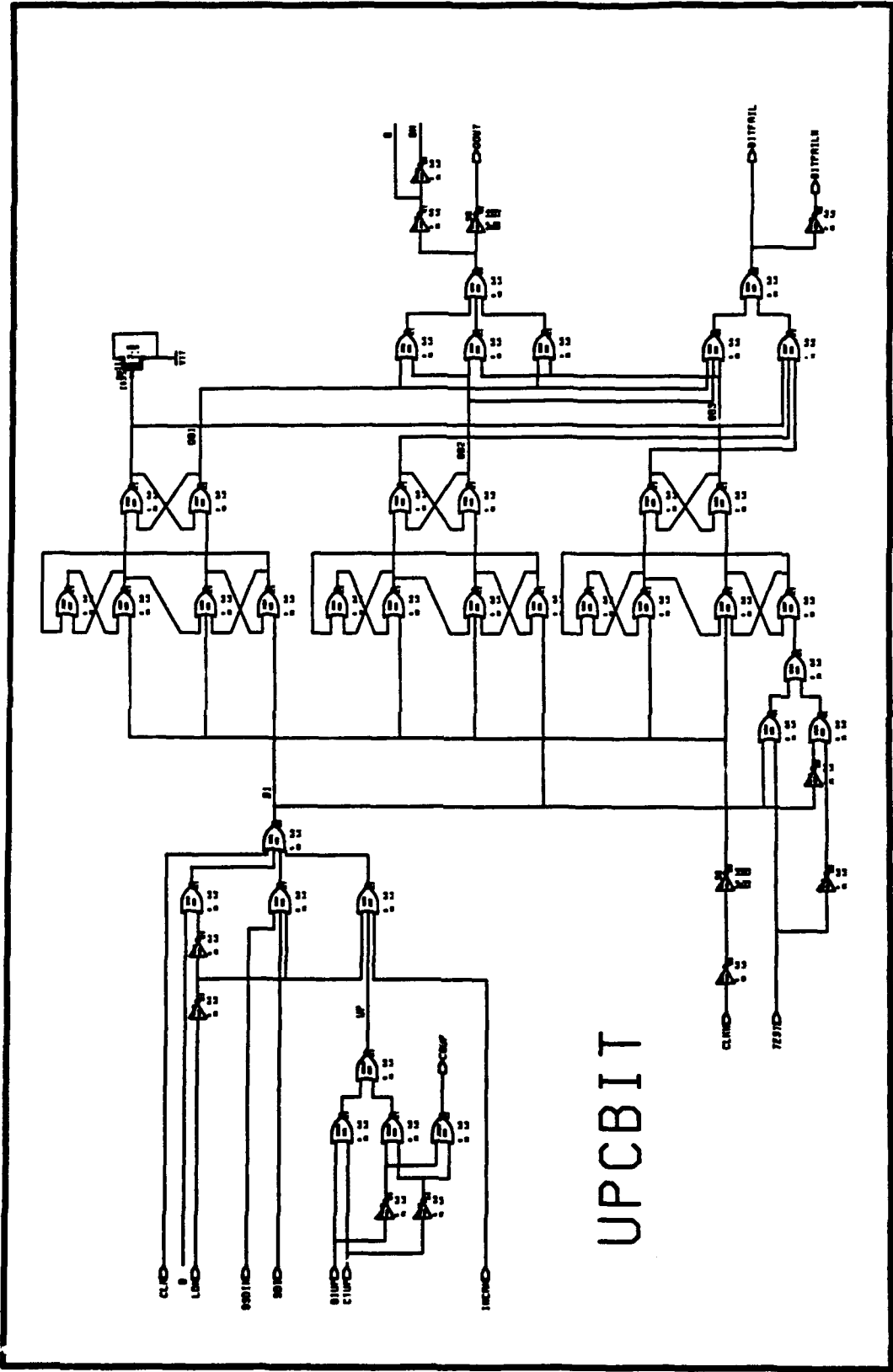


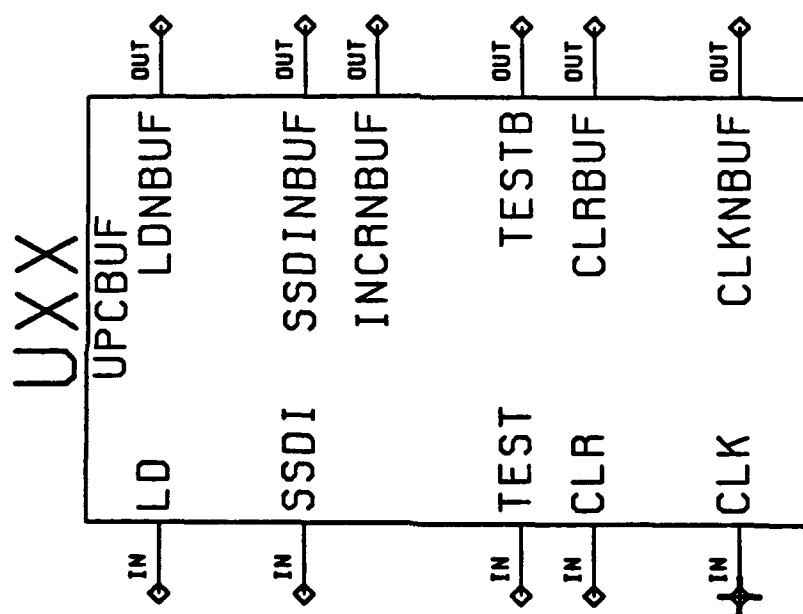


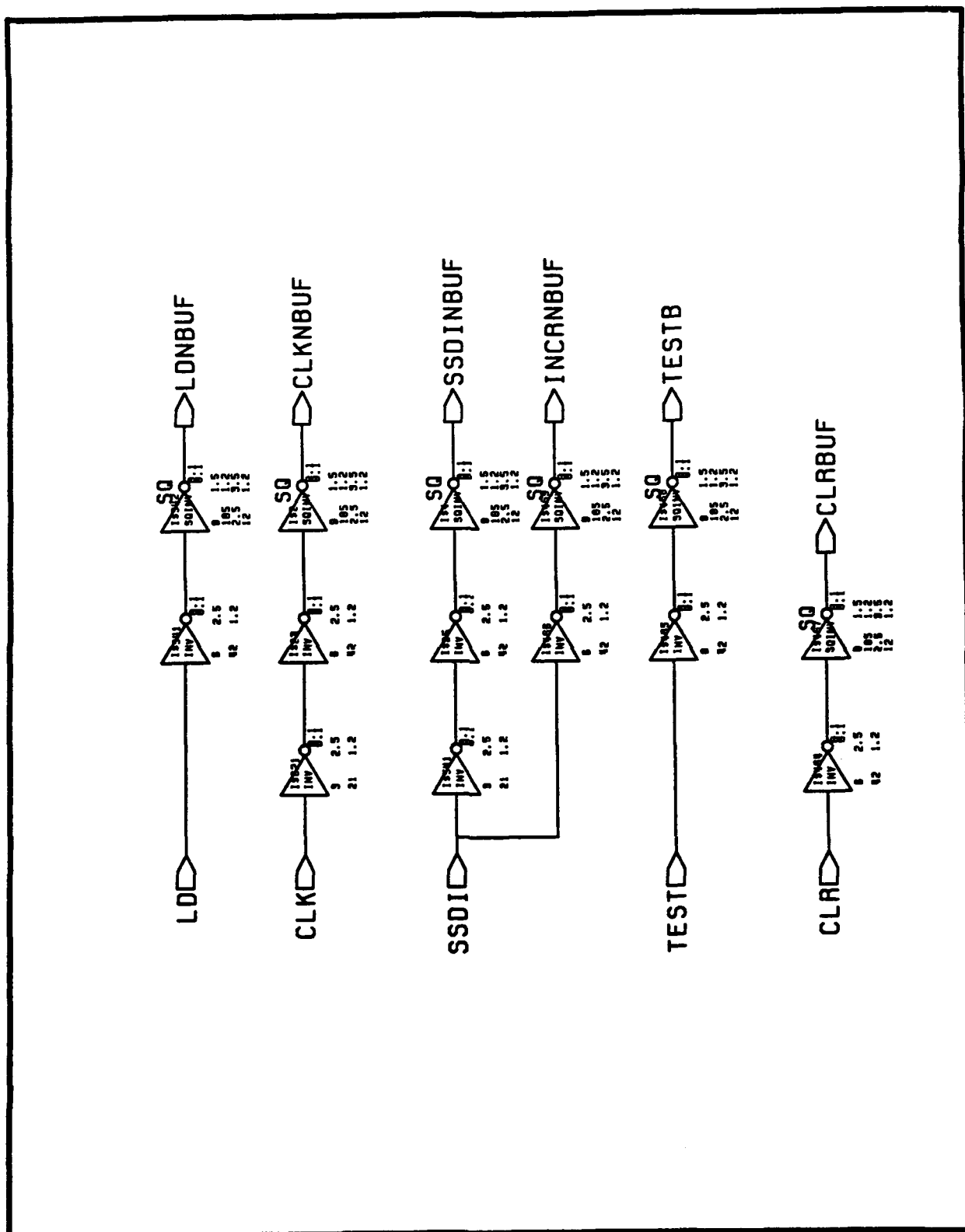


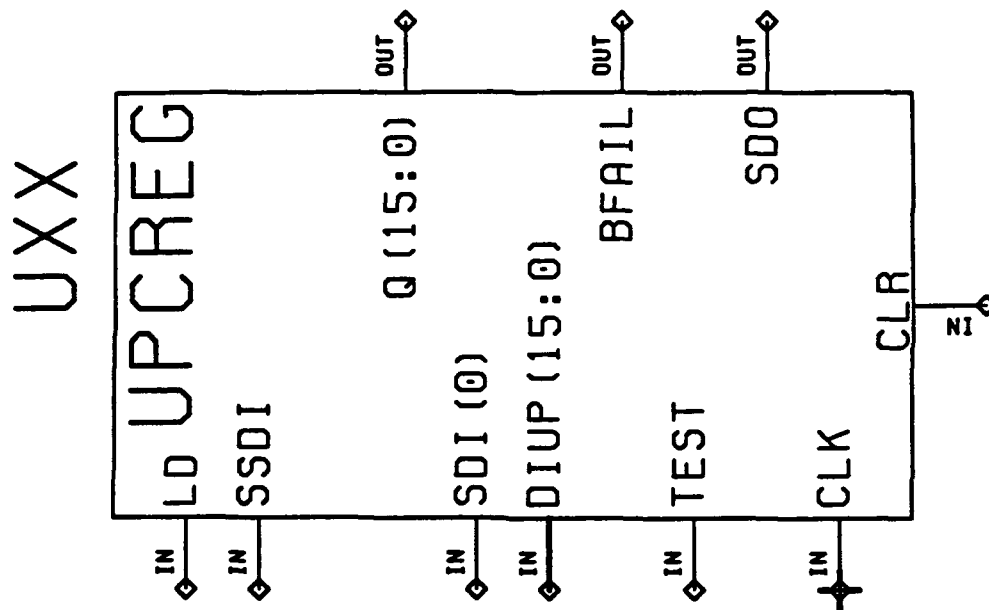




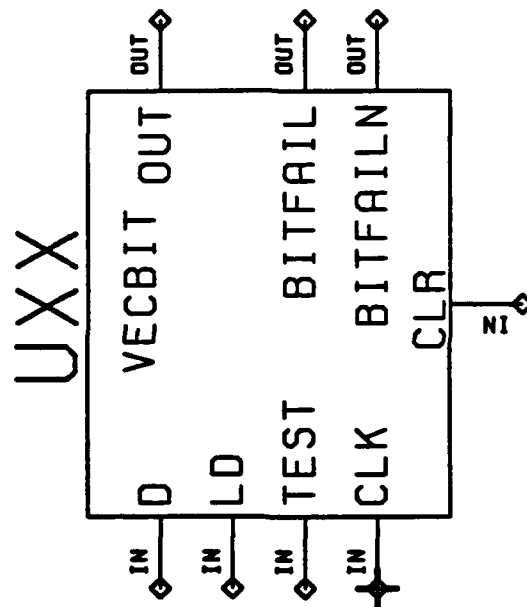


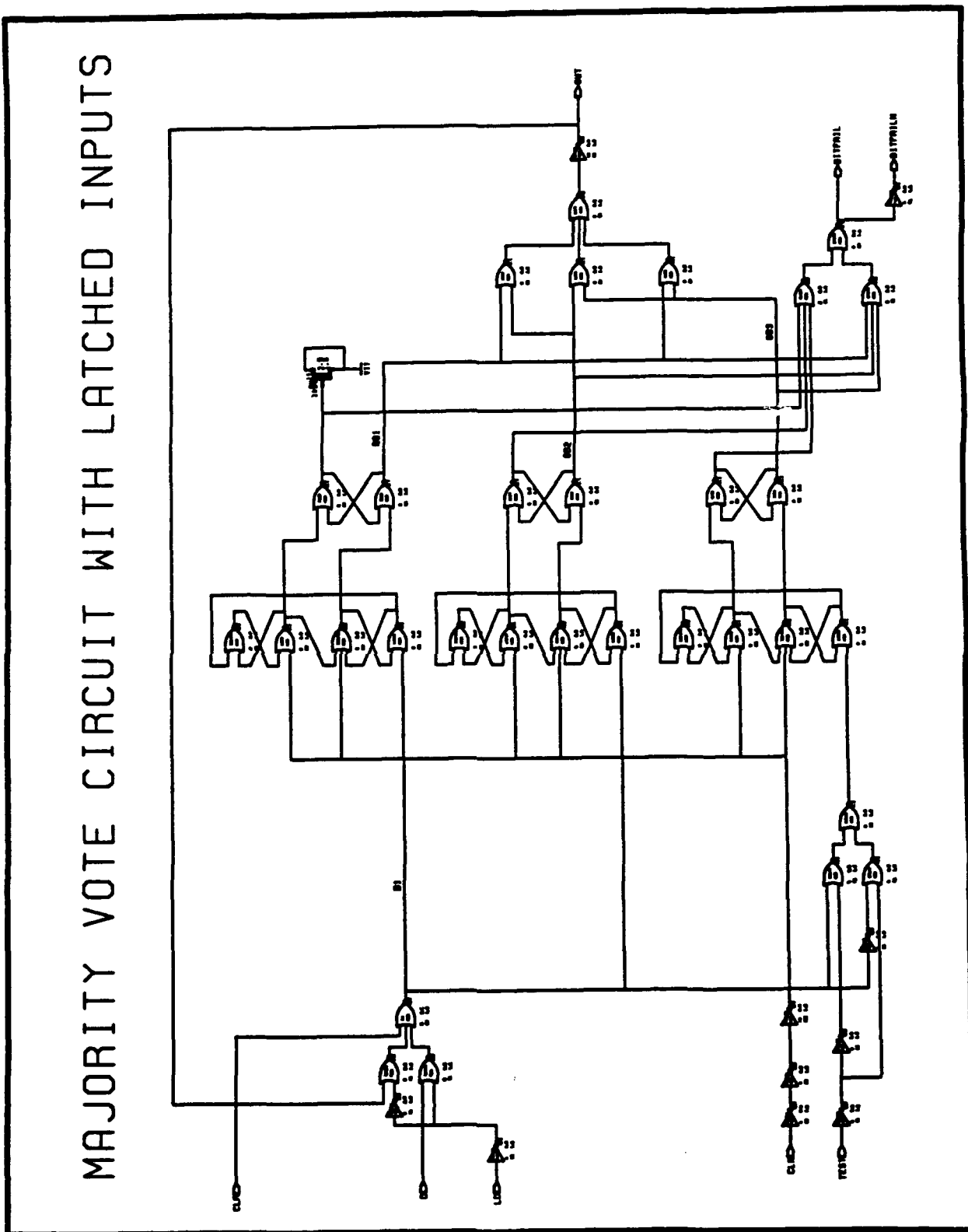


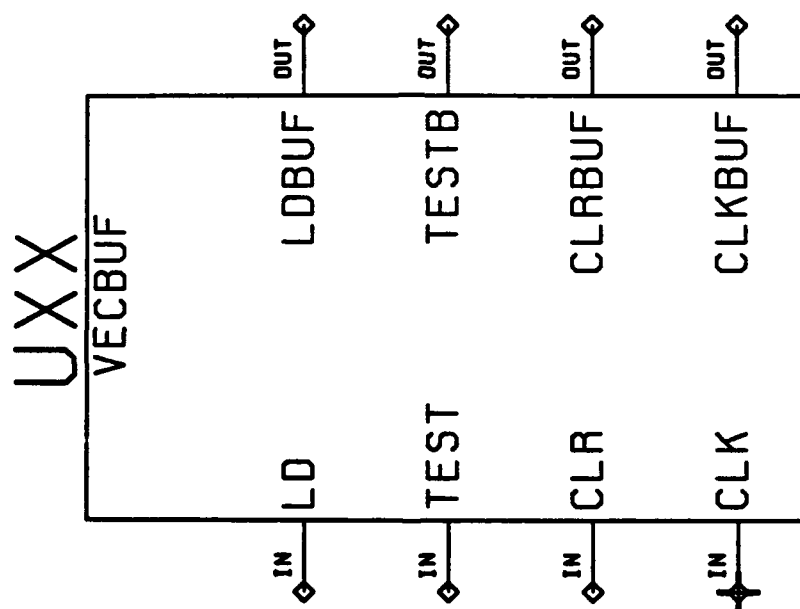




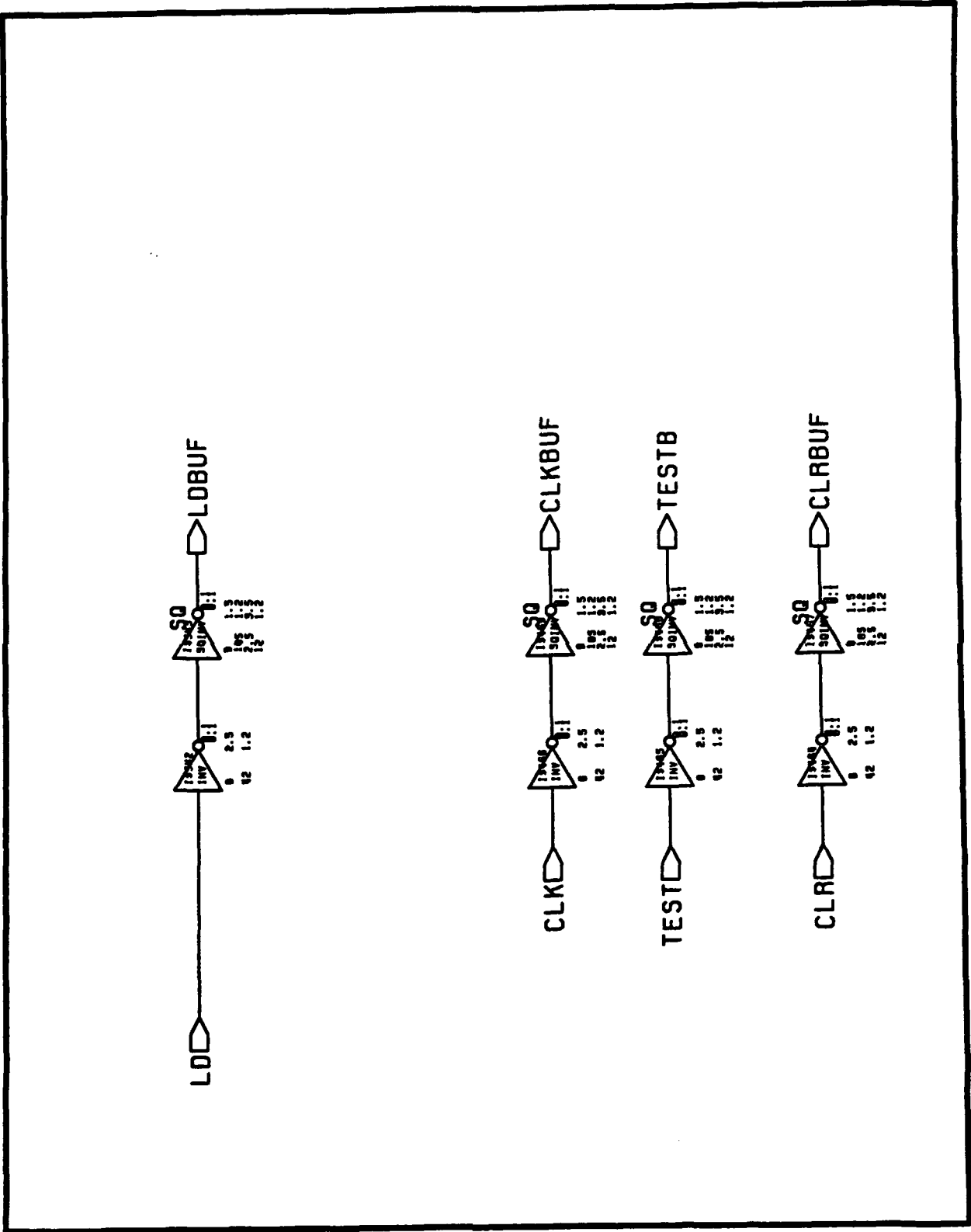


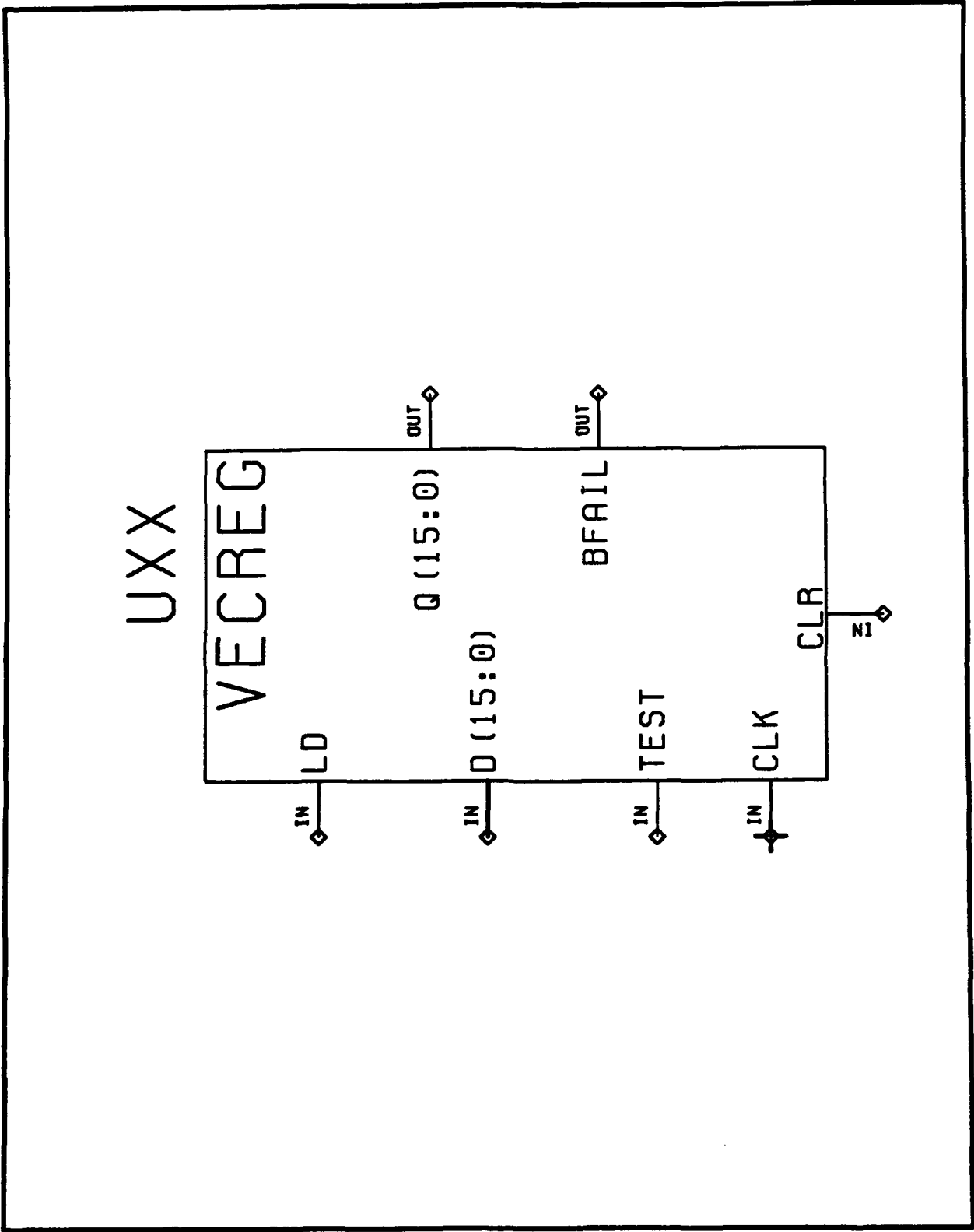


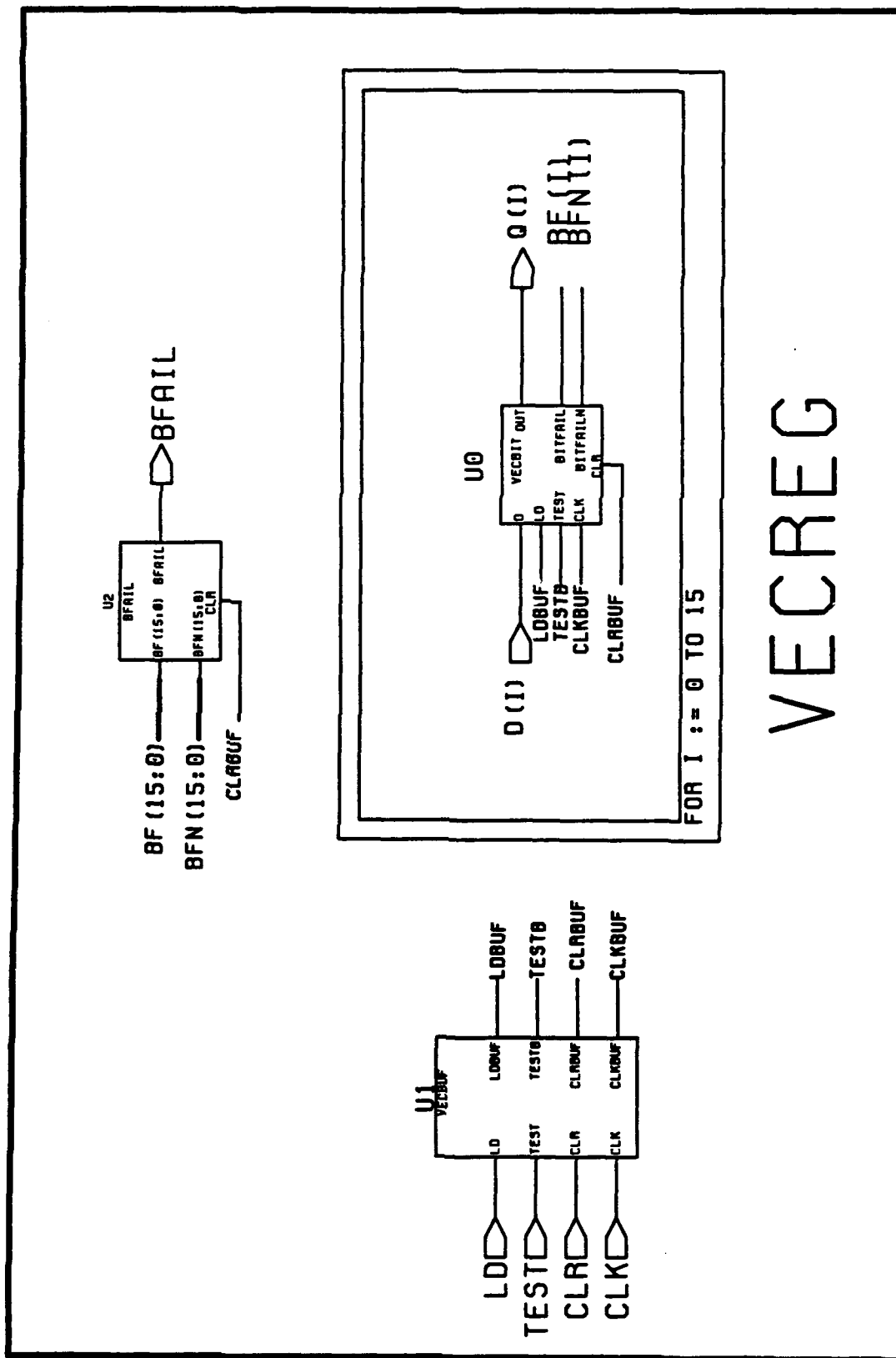


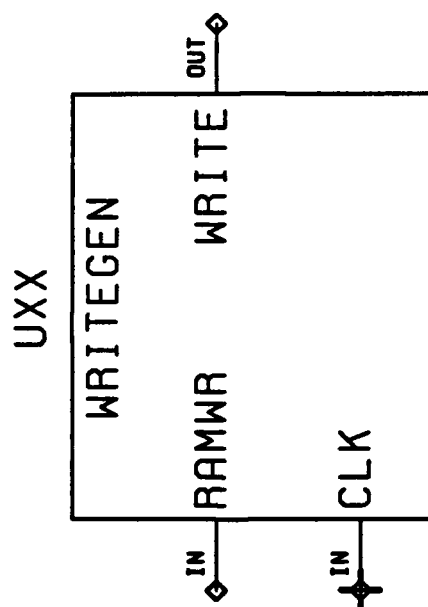


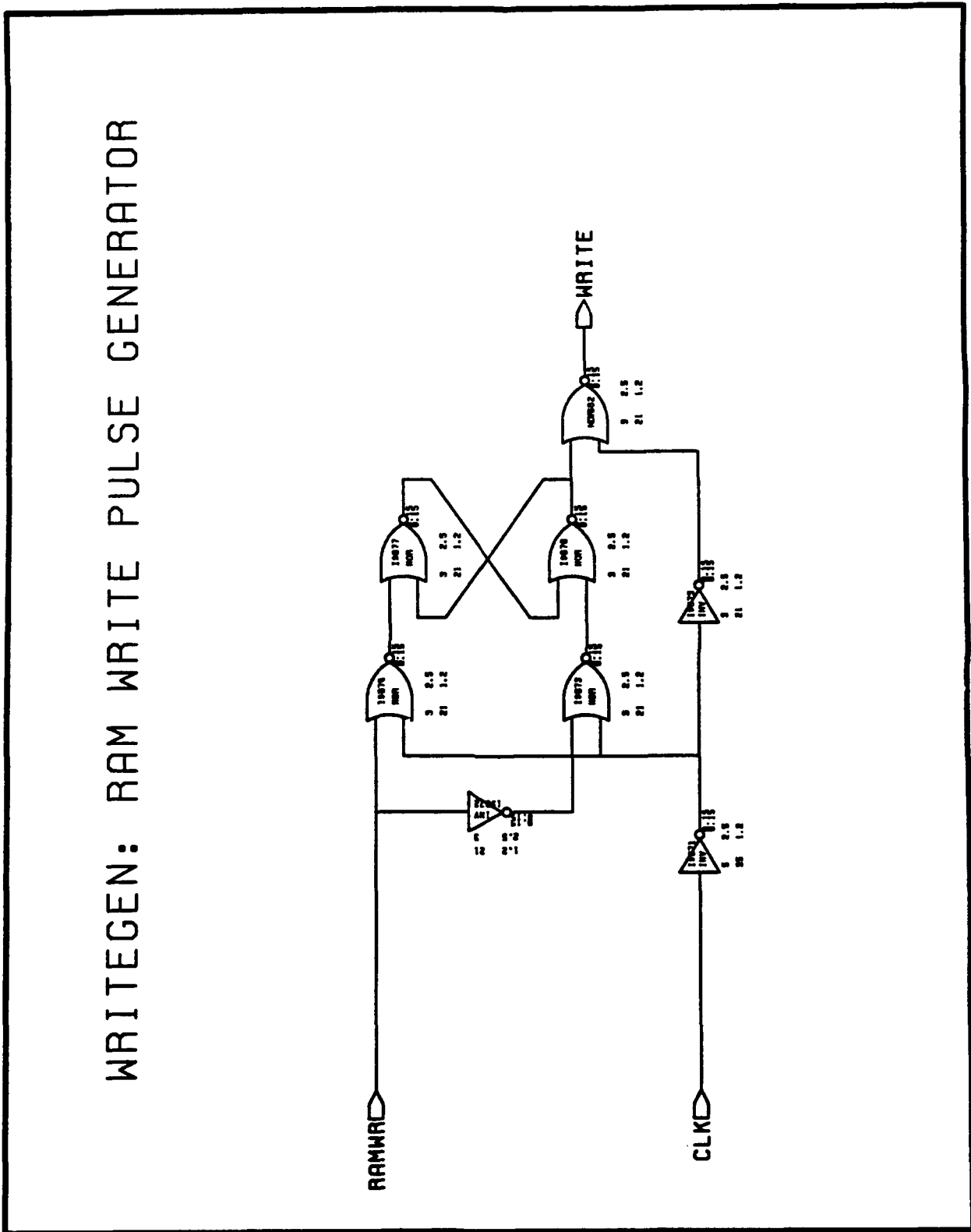


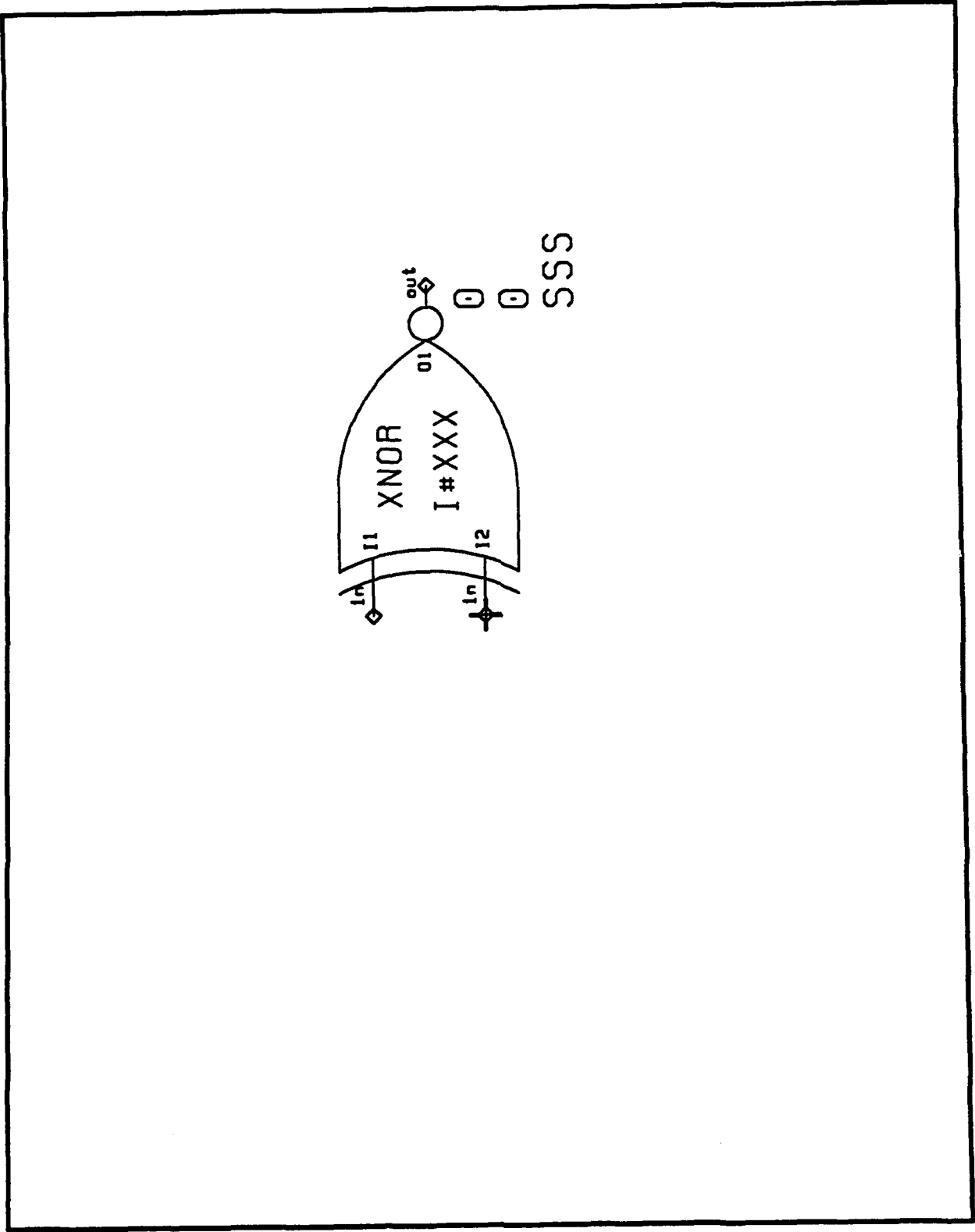


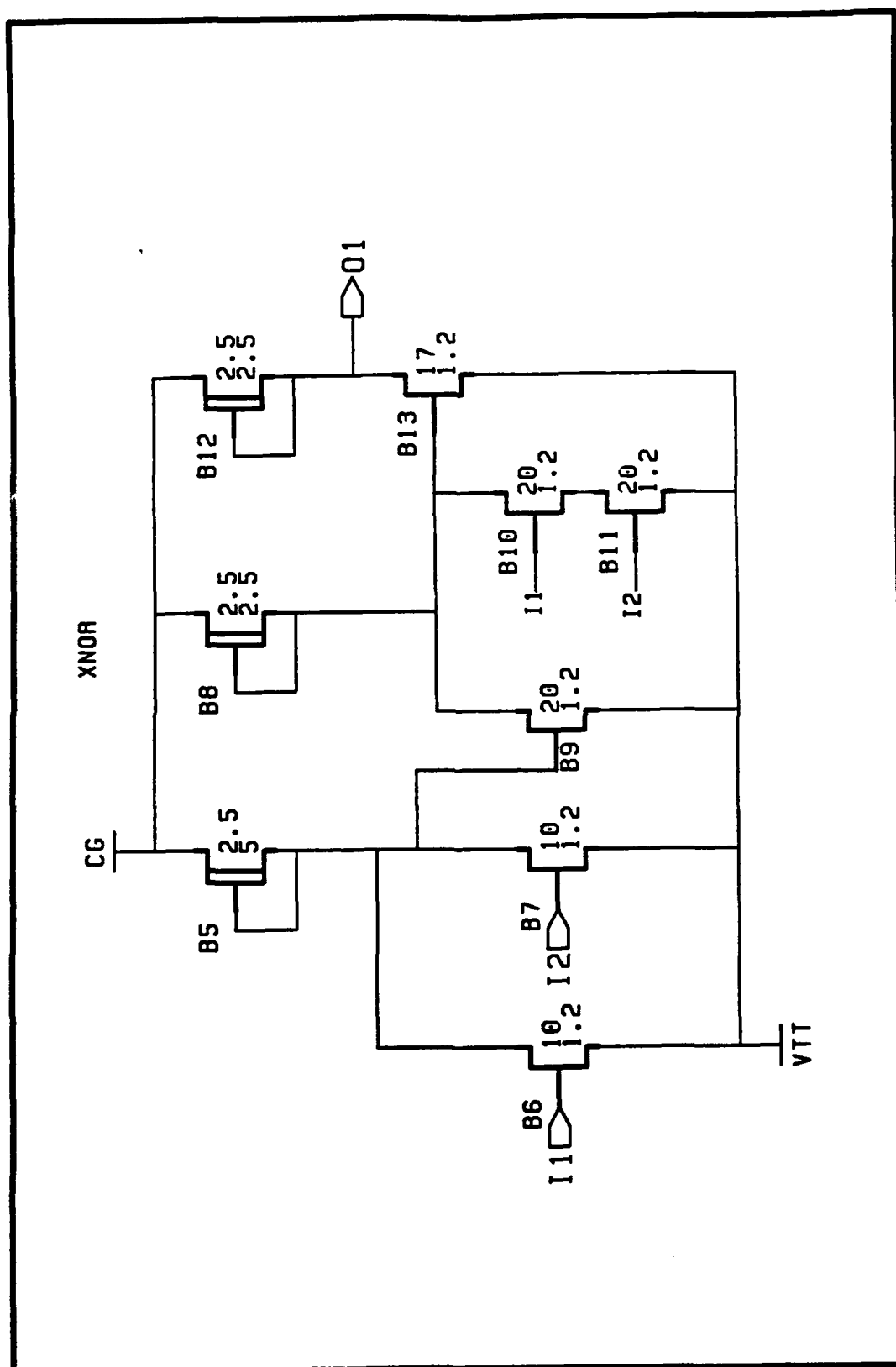


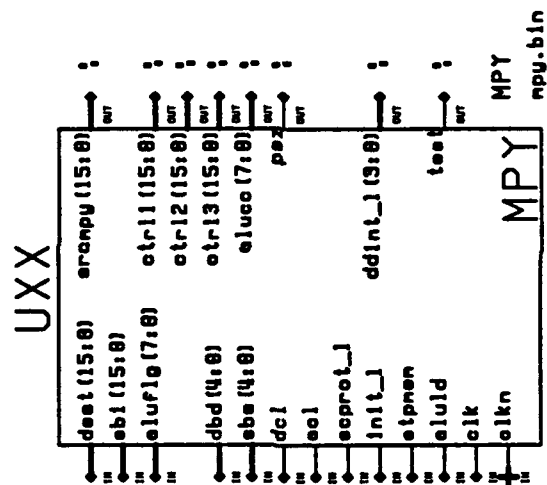




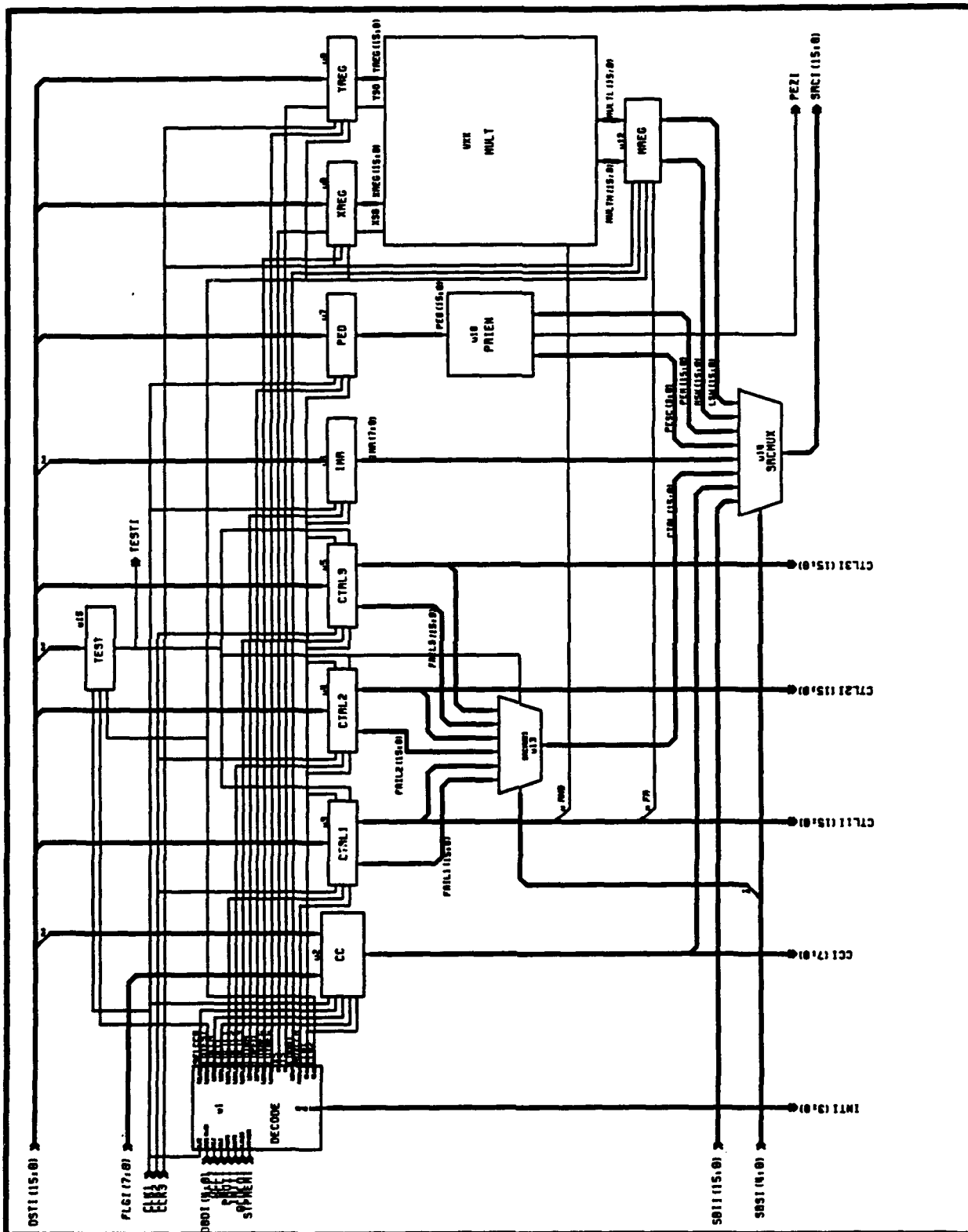


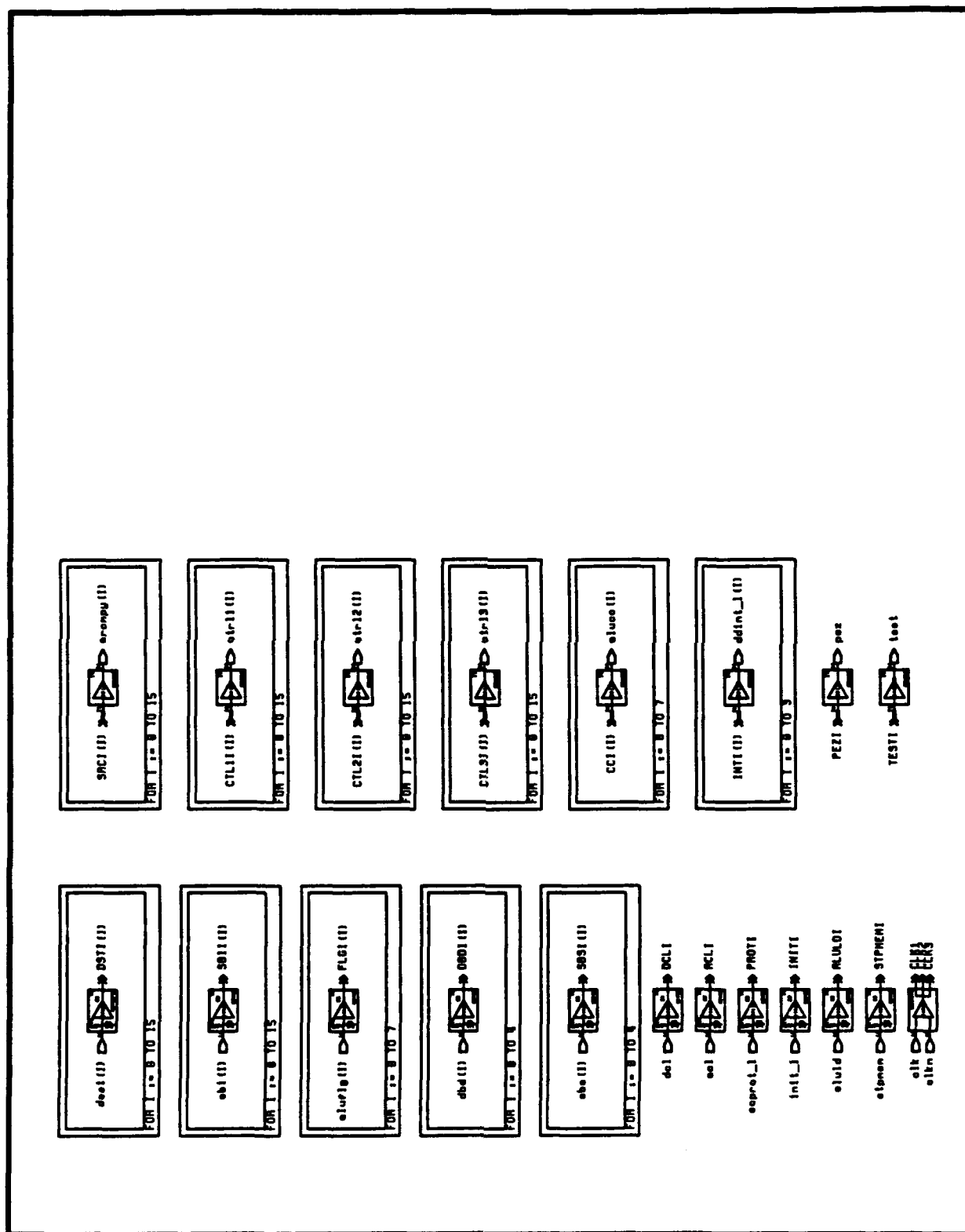


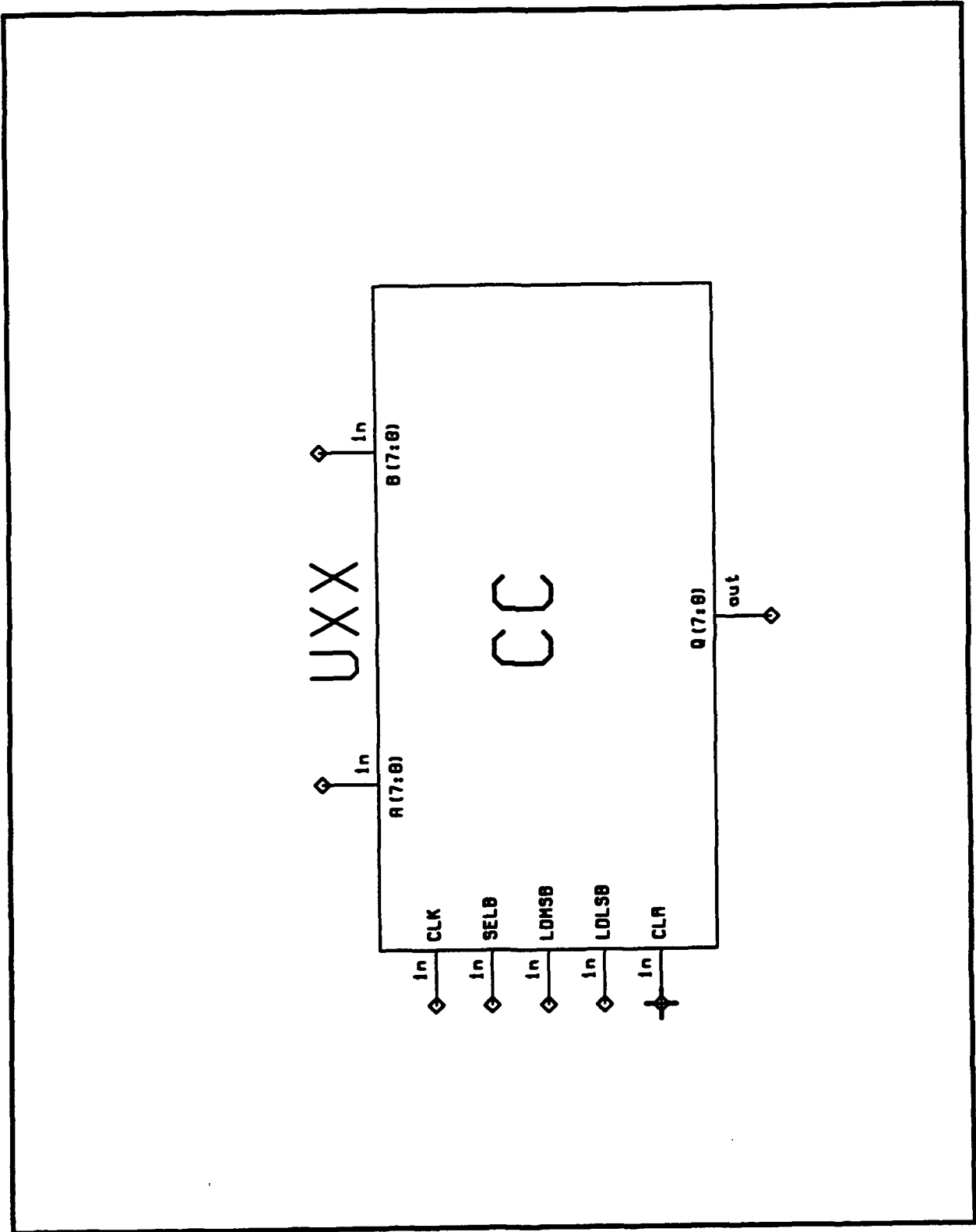


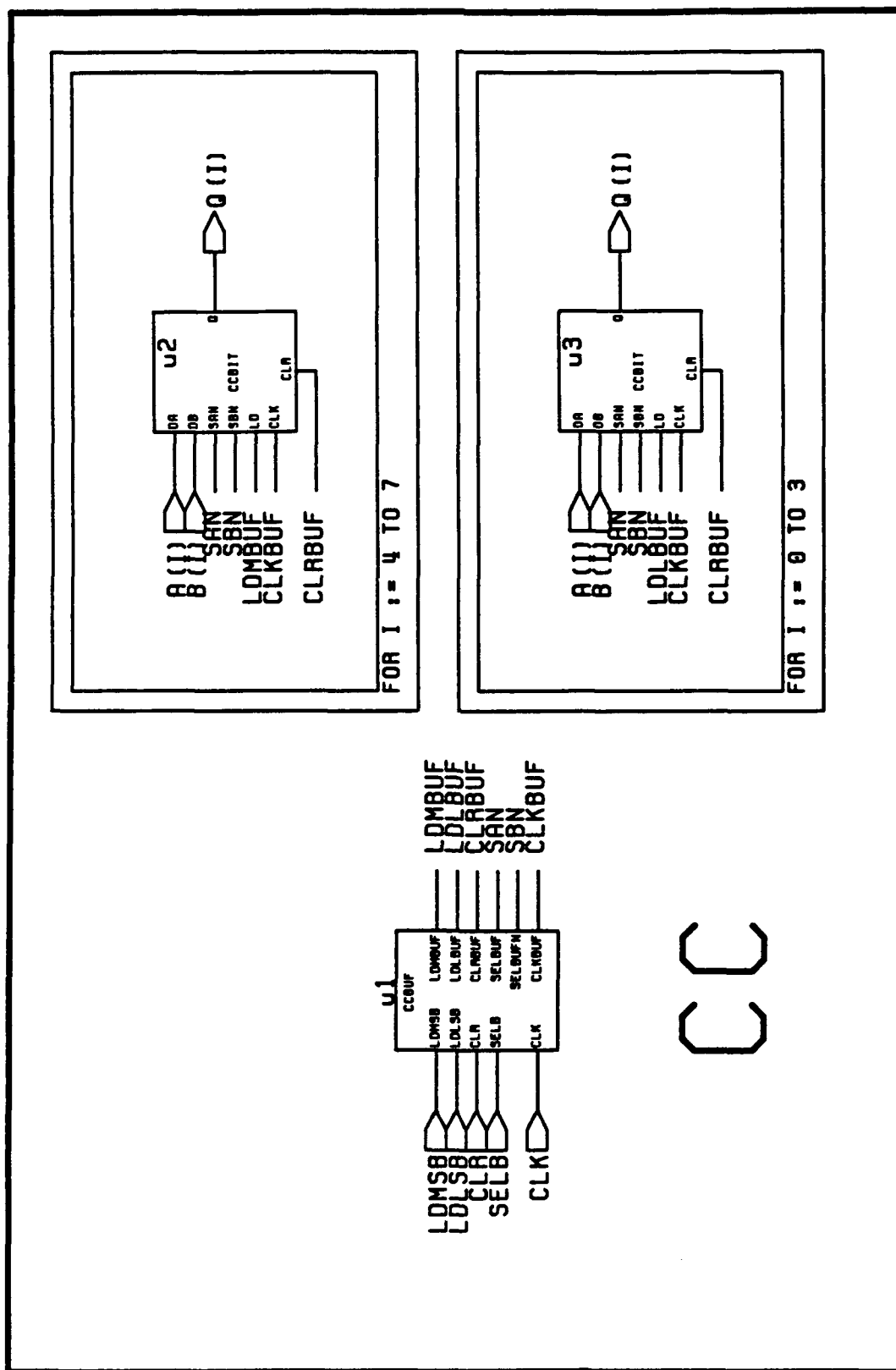


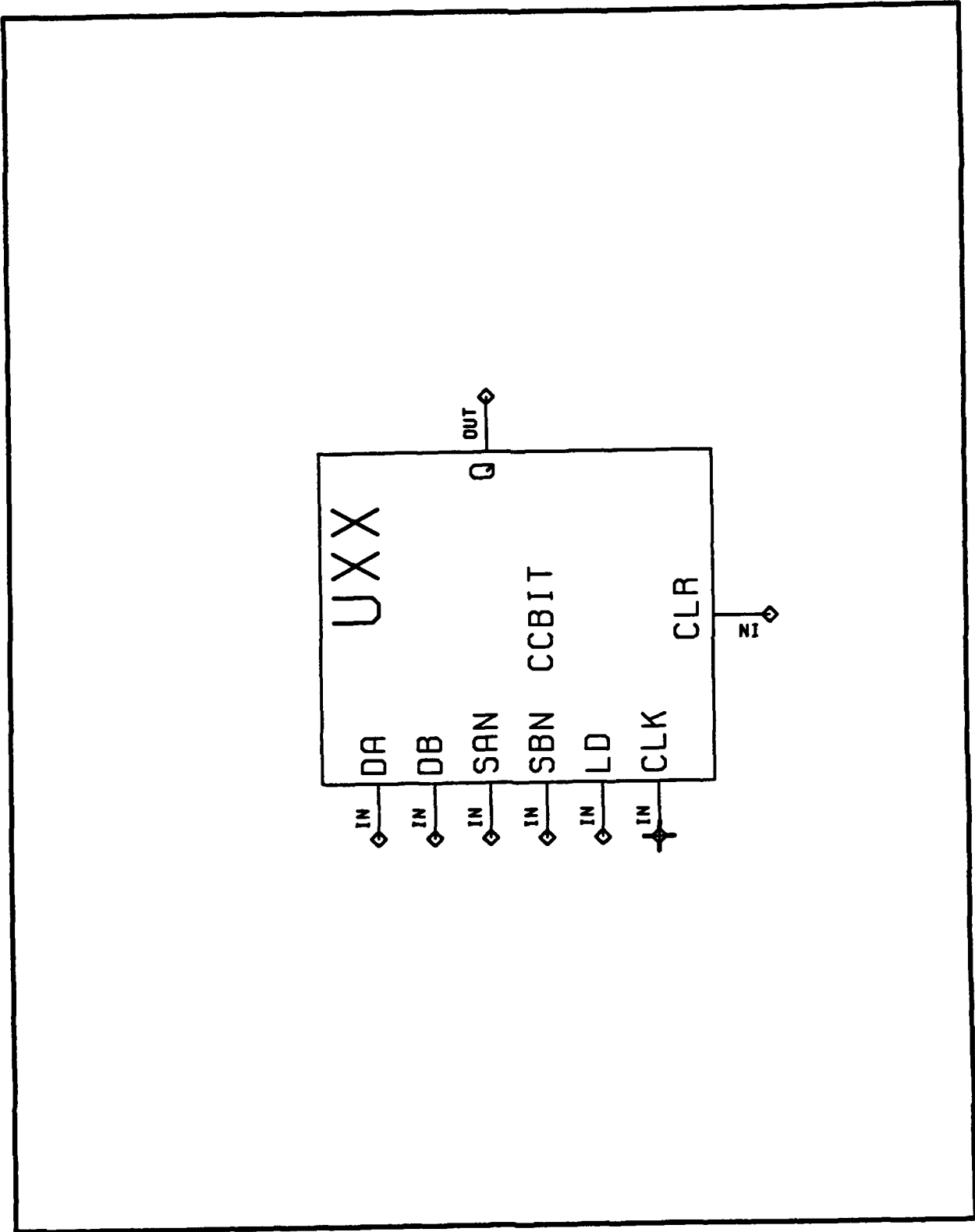


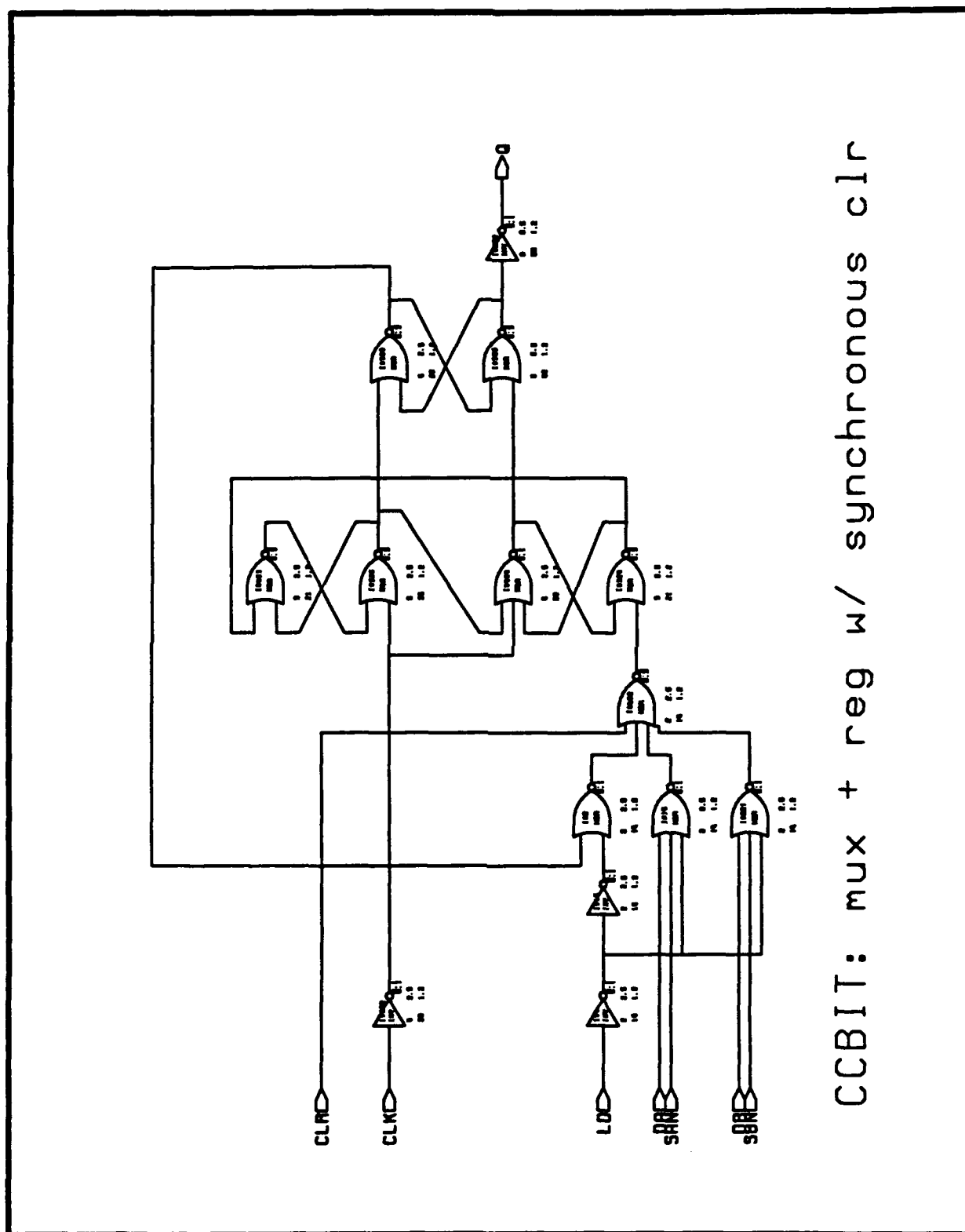


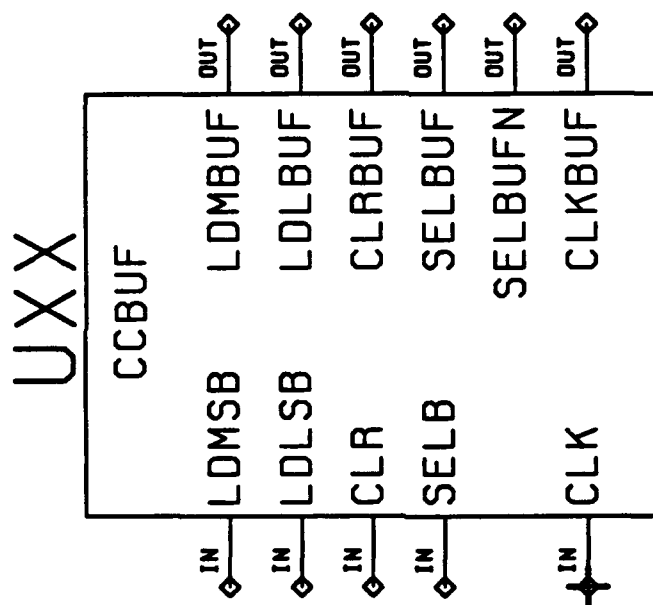


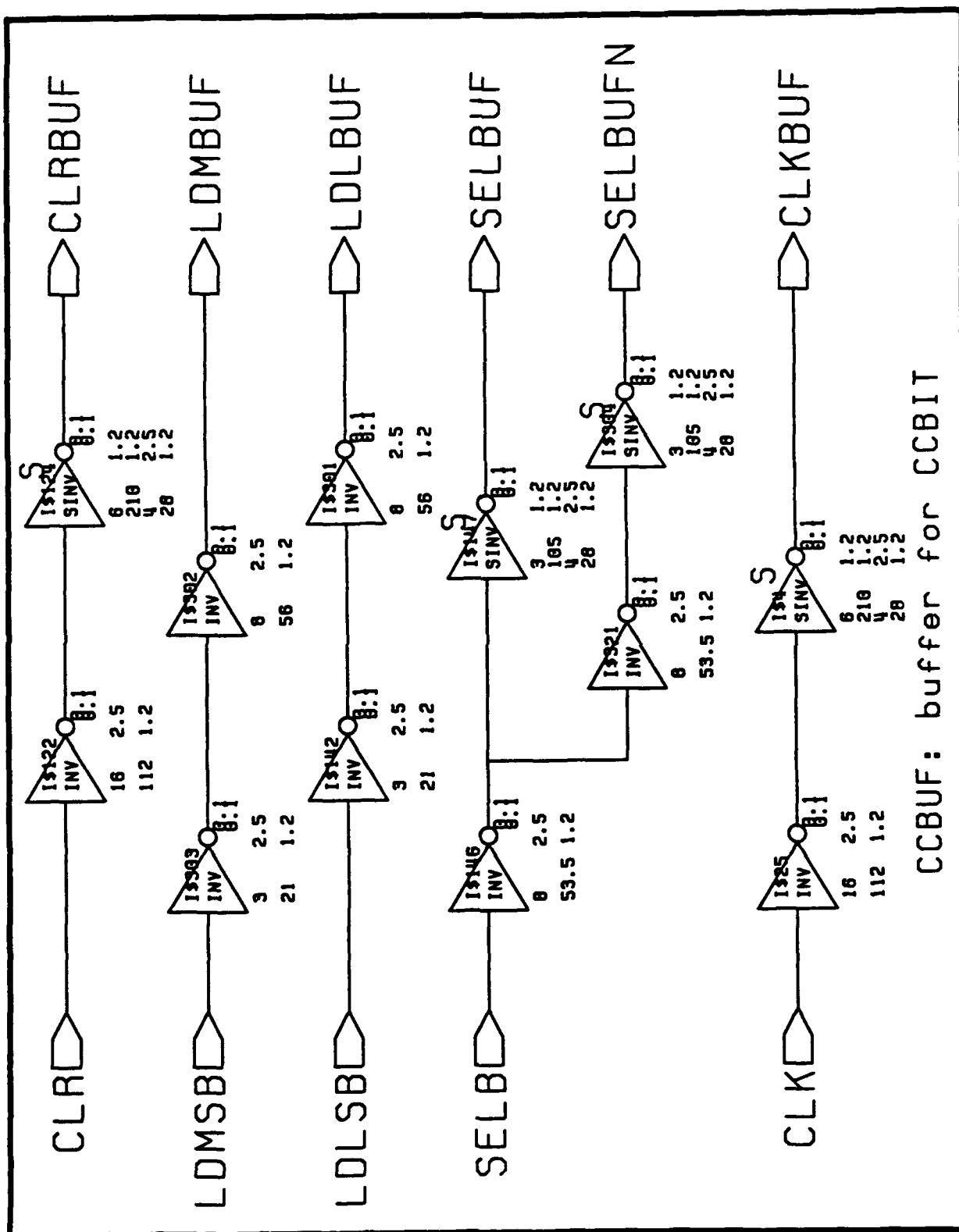








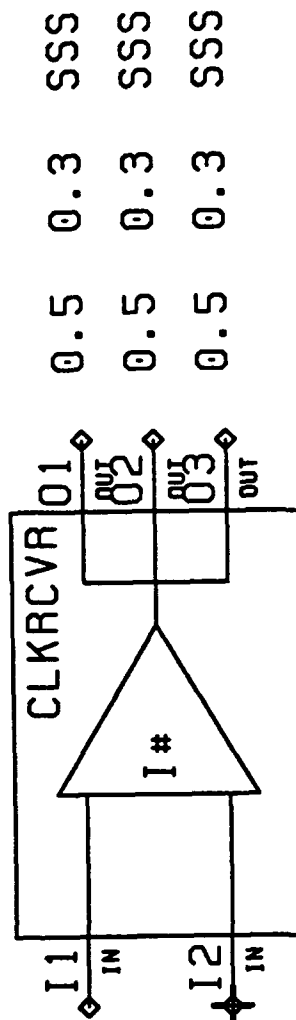




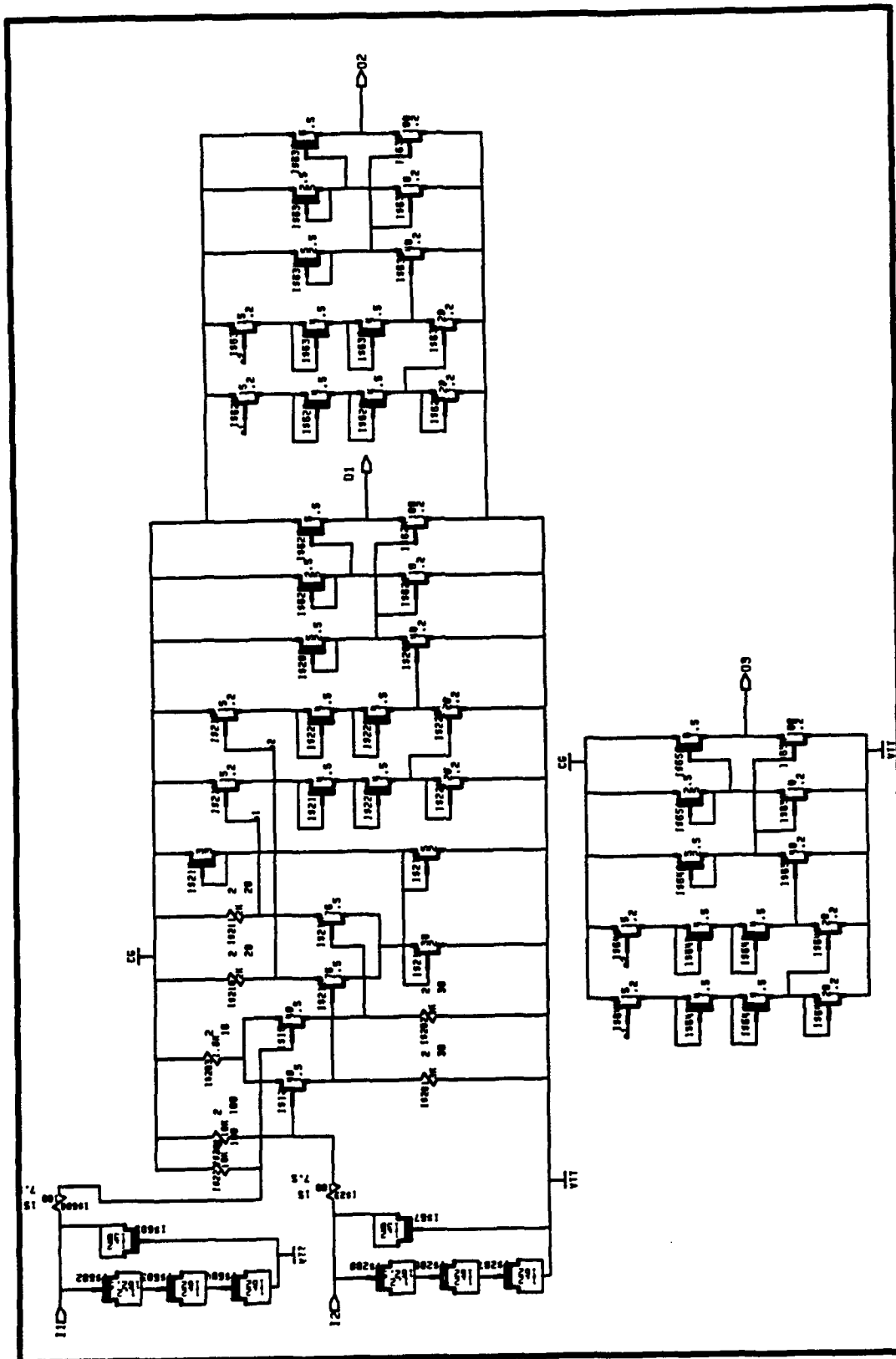


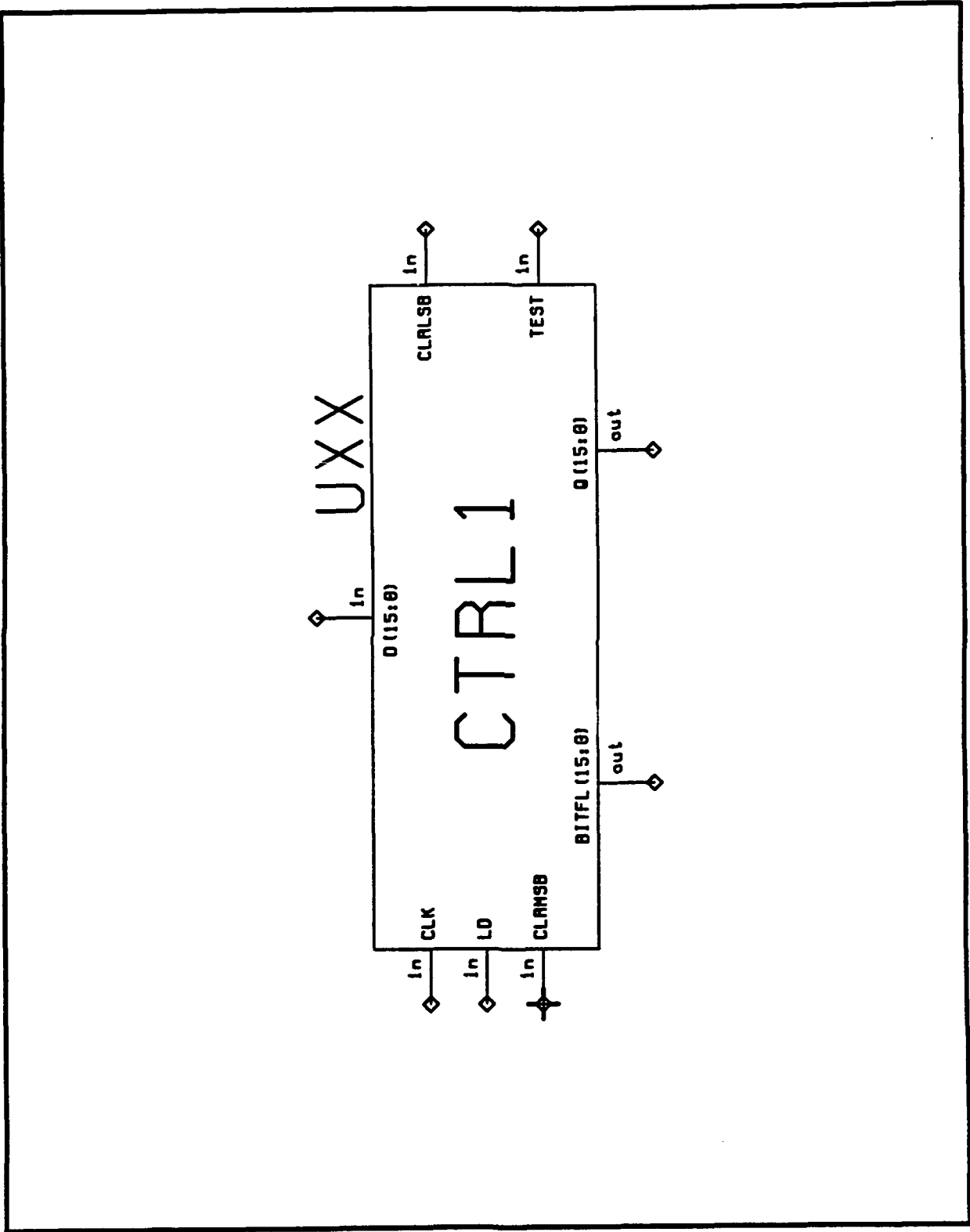
MPY LIBRARY

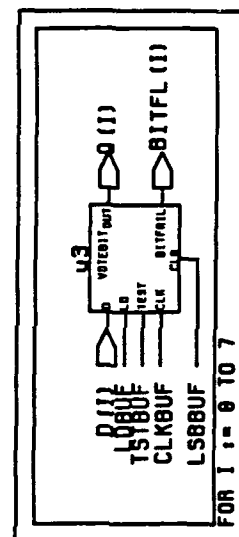
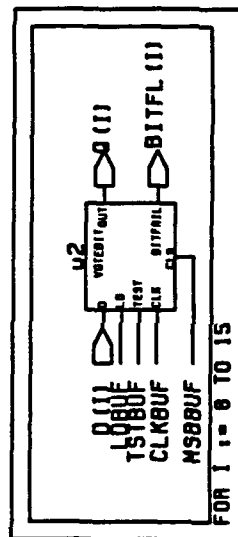
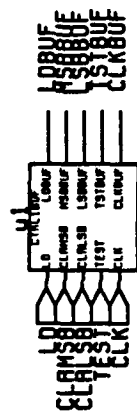
NAME: CLKRCVR FOR MPY  
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER



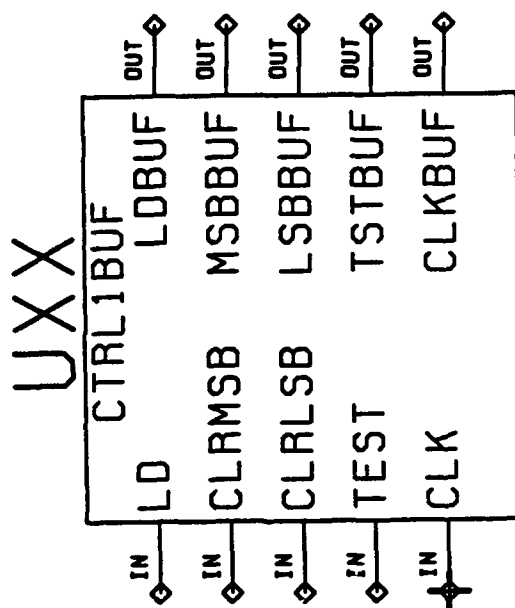
CLKRCVR  
clkrcvr.bin

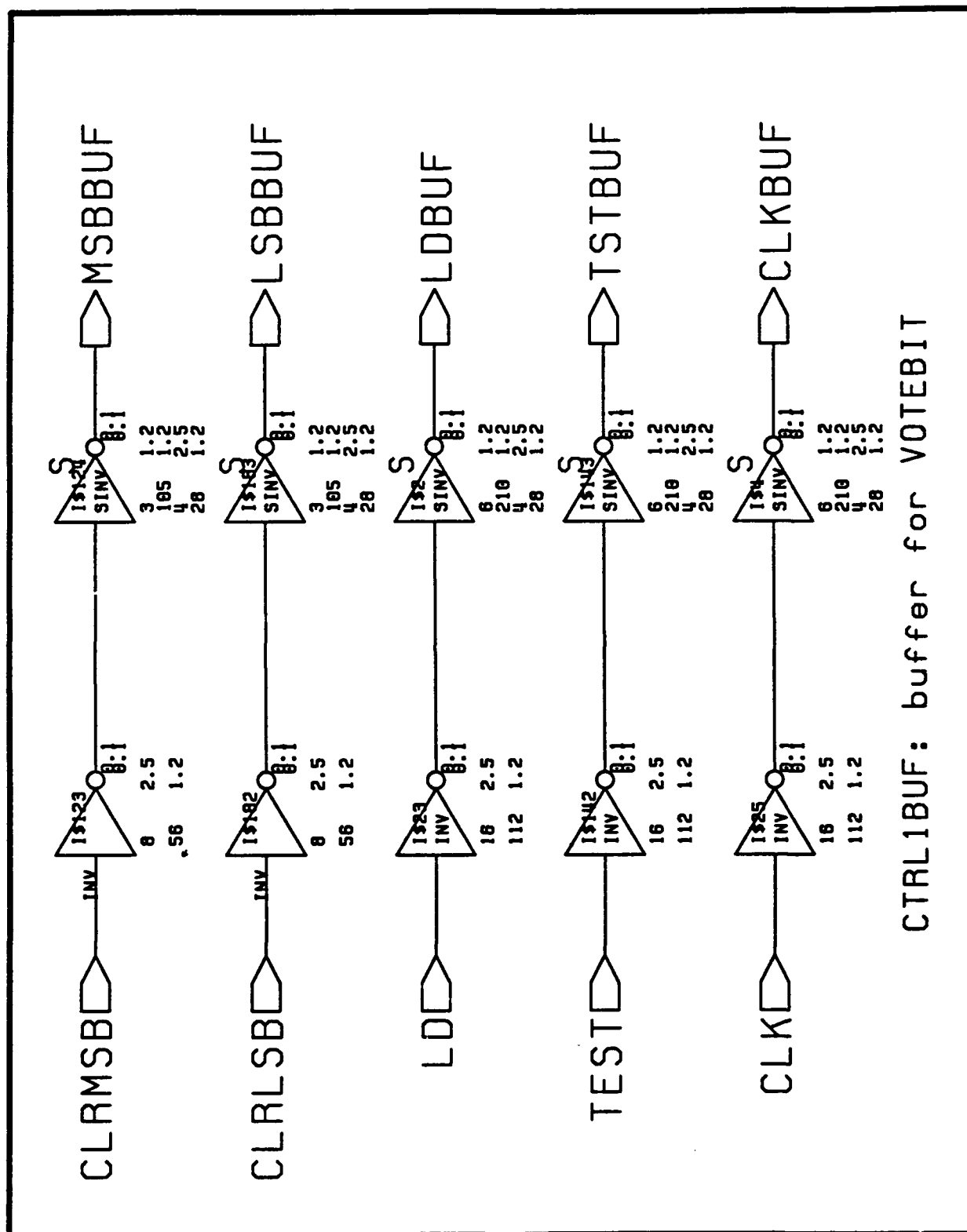


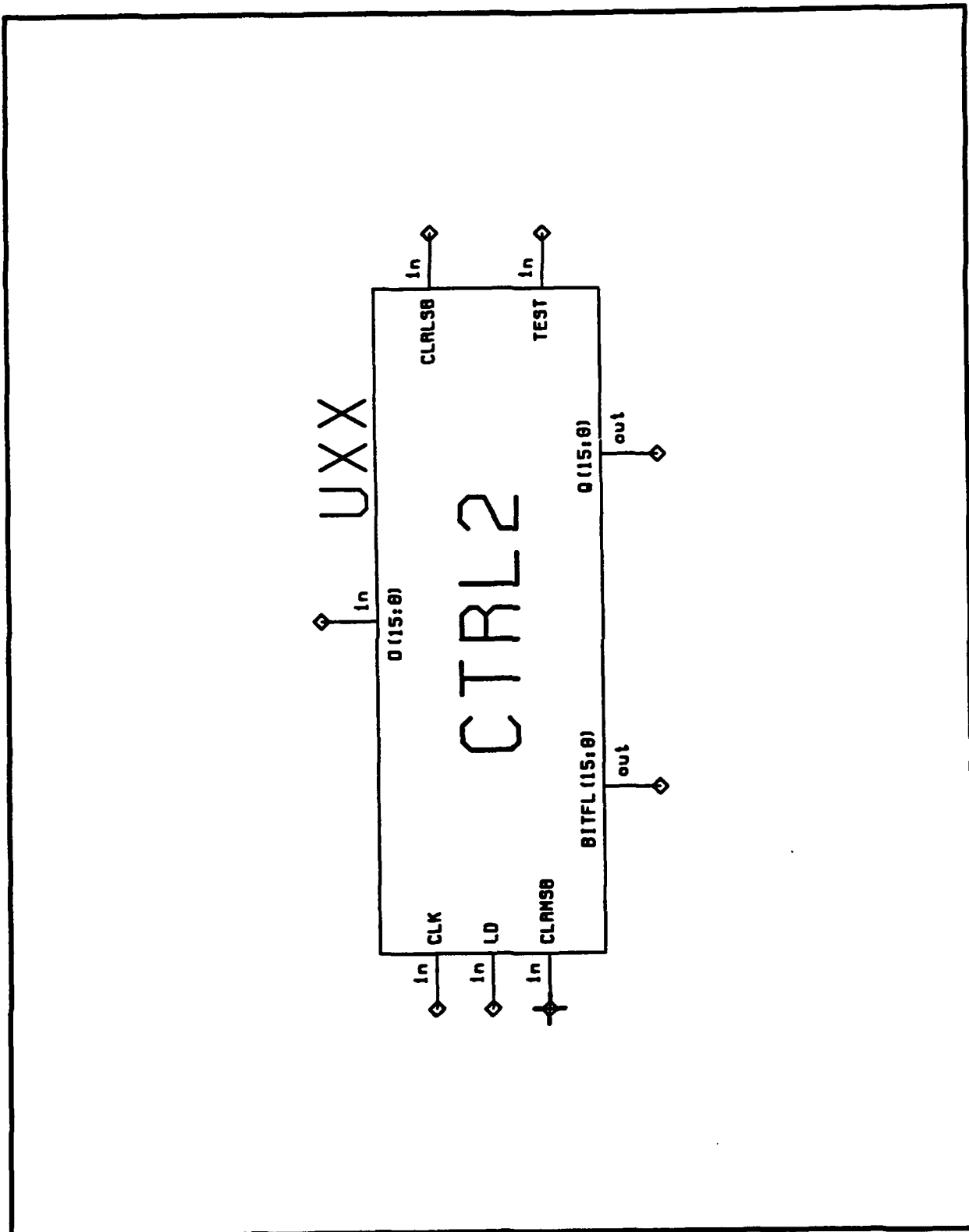


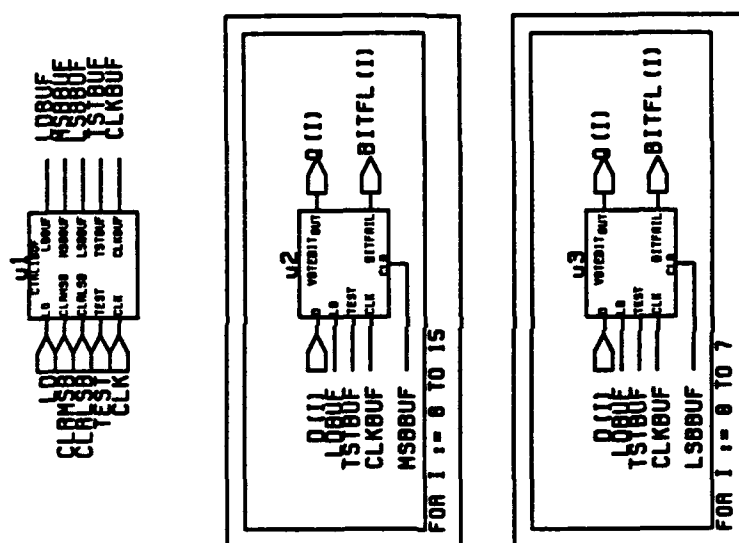


CTRL1



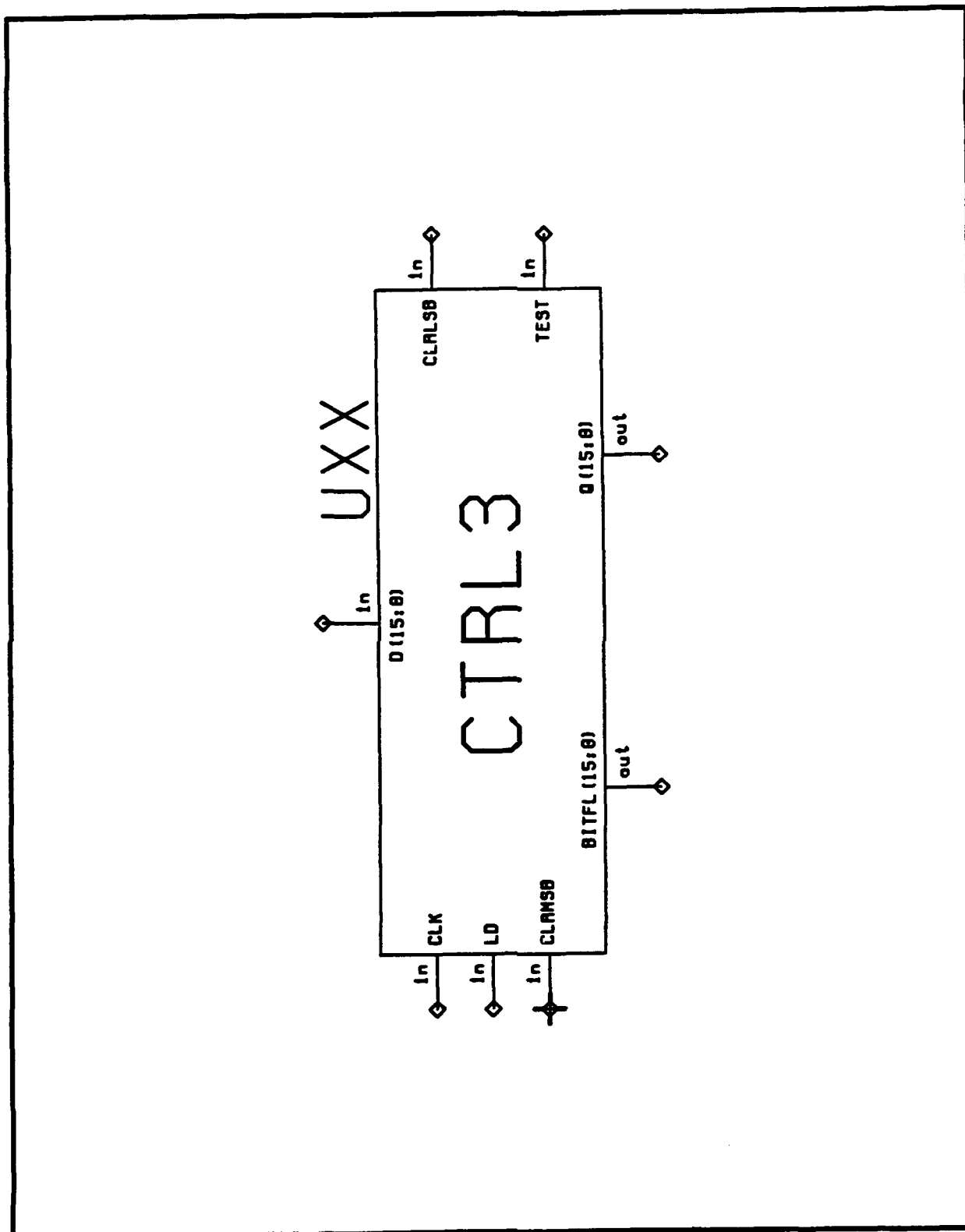


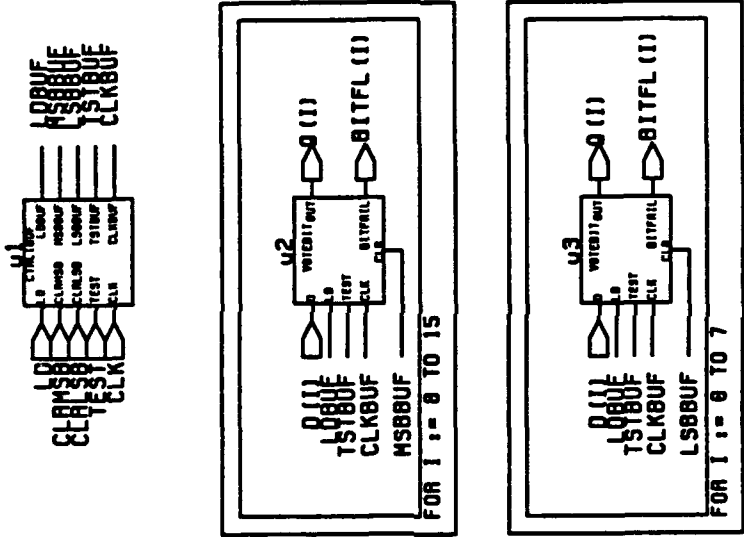




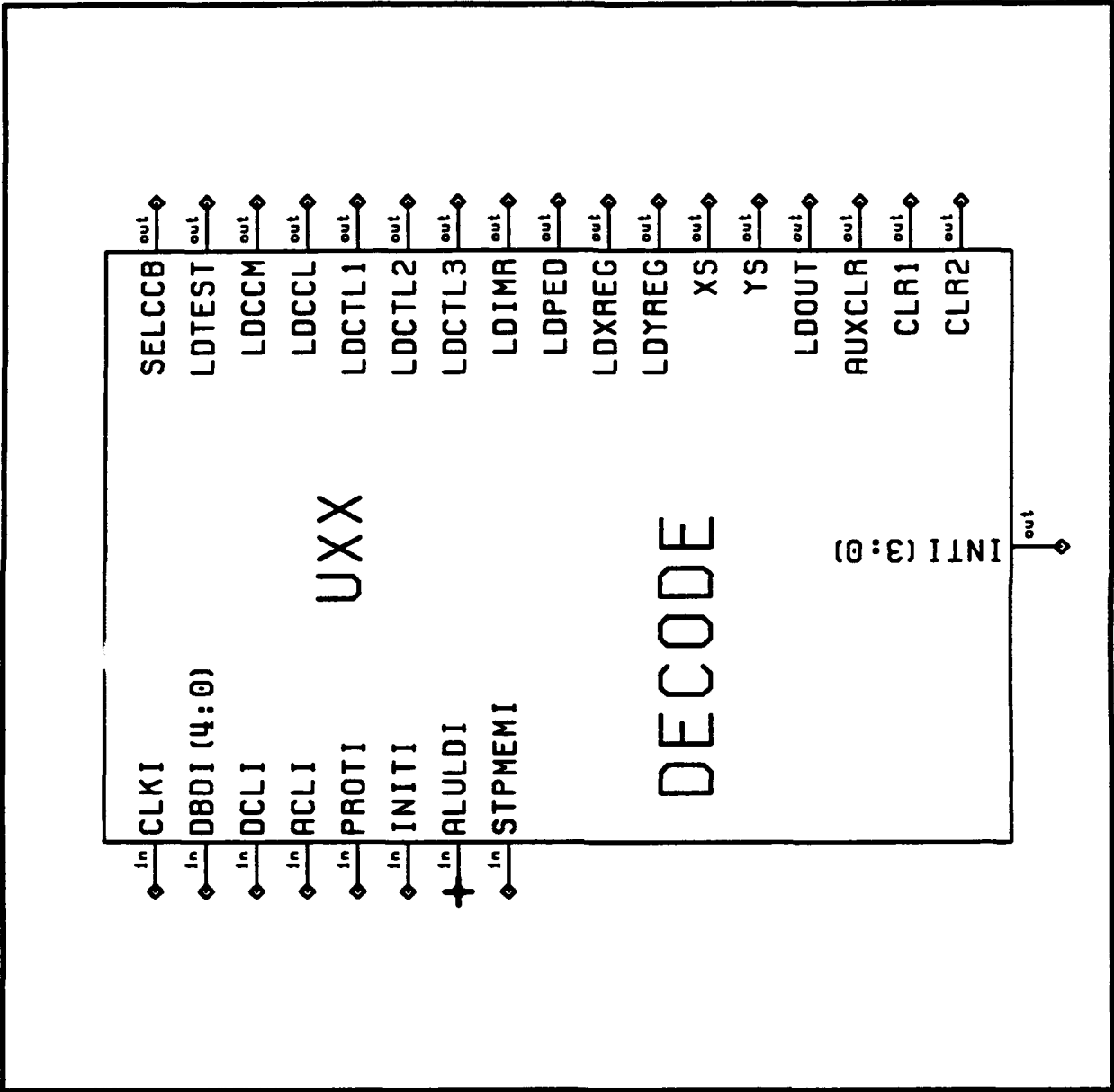
218

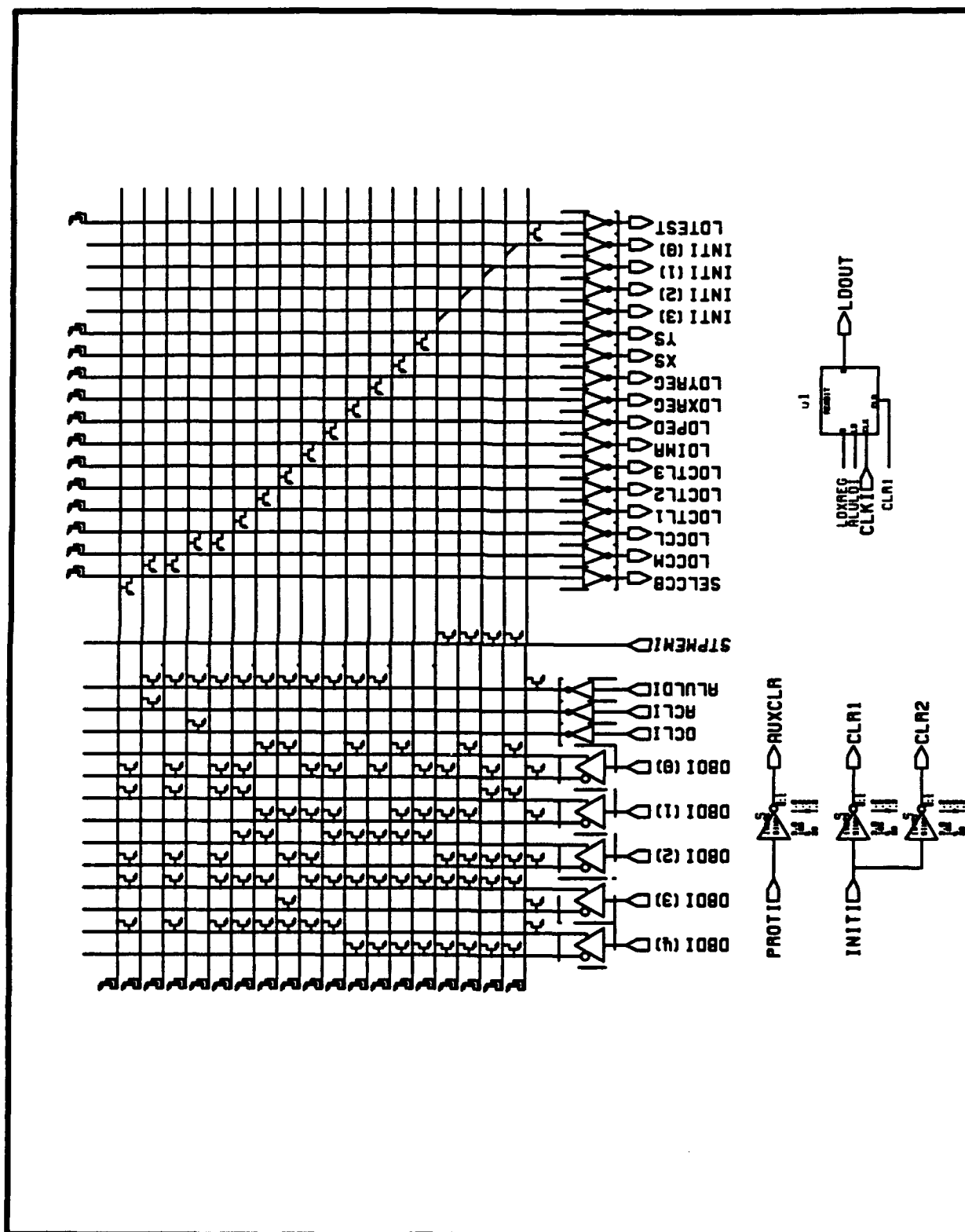






CTRL3



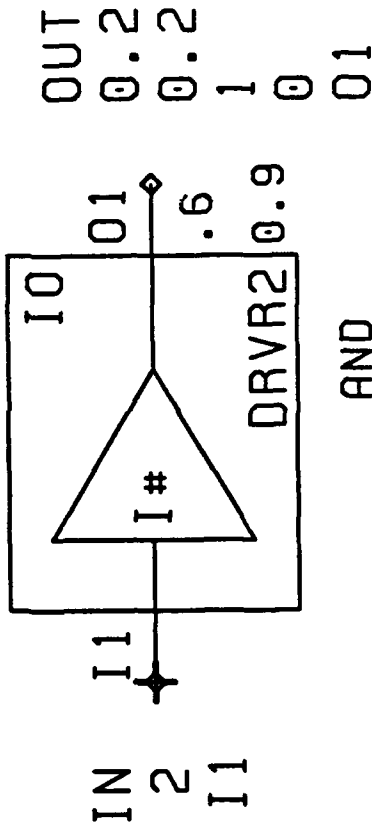


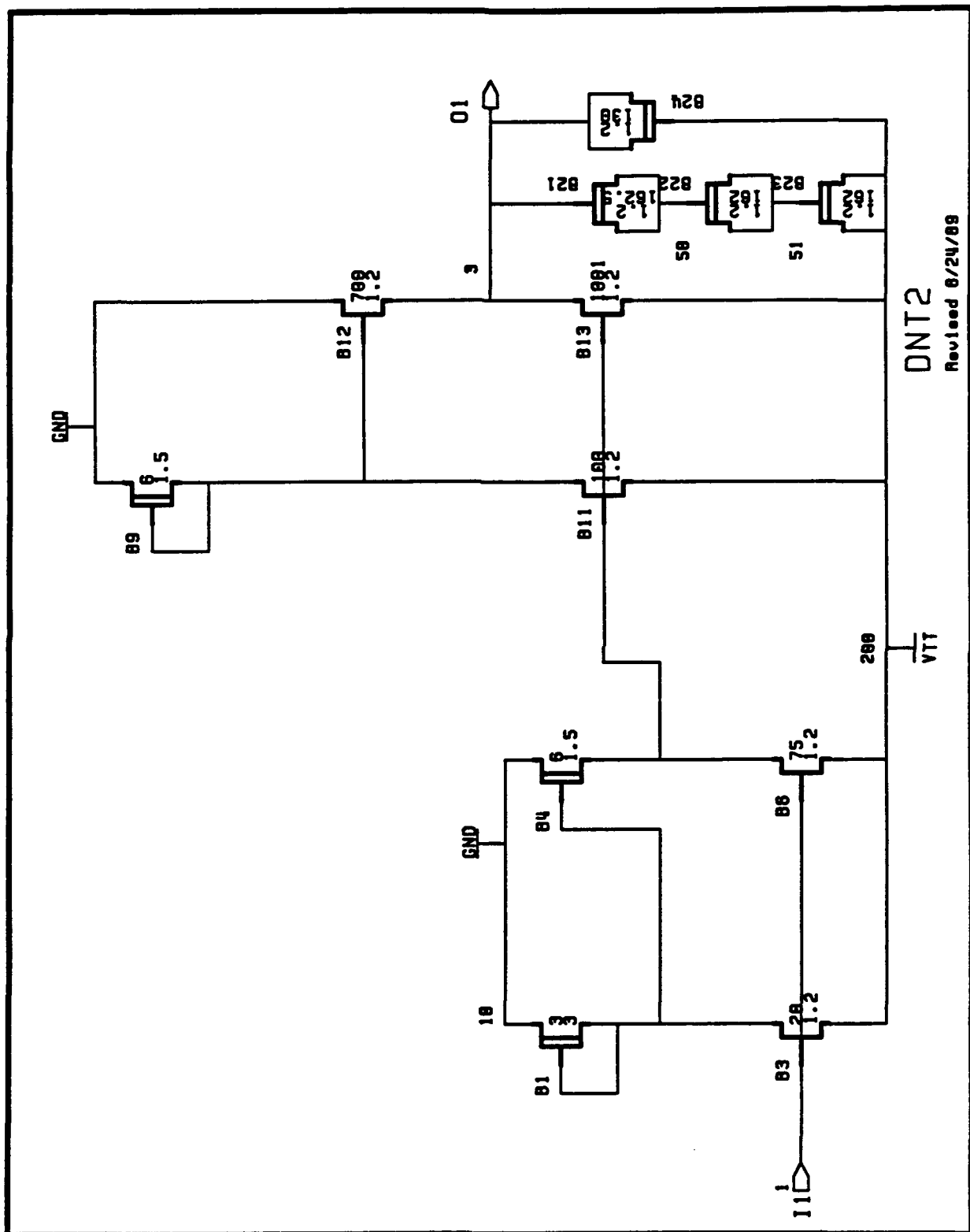
VITESSE GAAS CELL LIBRARY

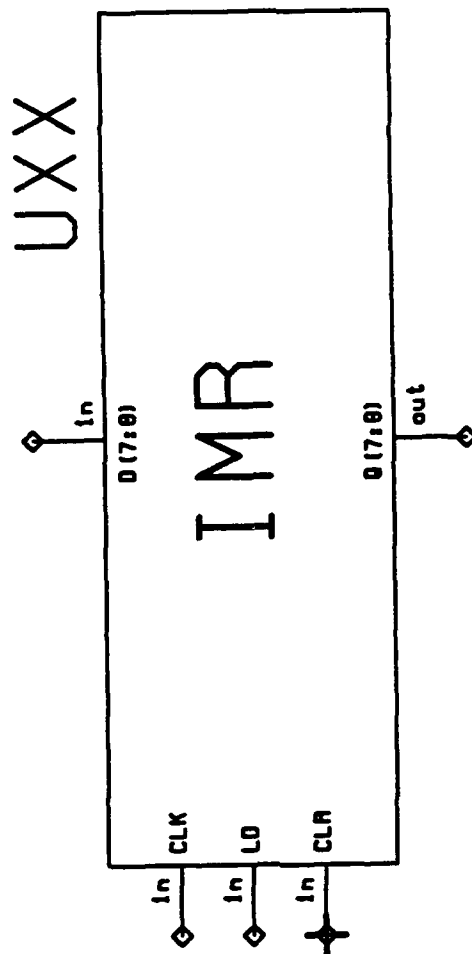
Version 0.8

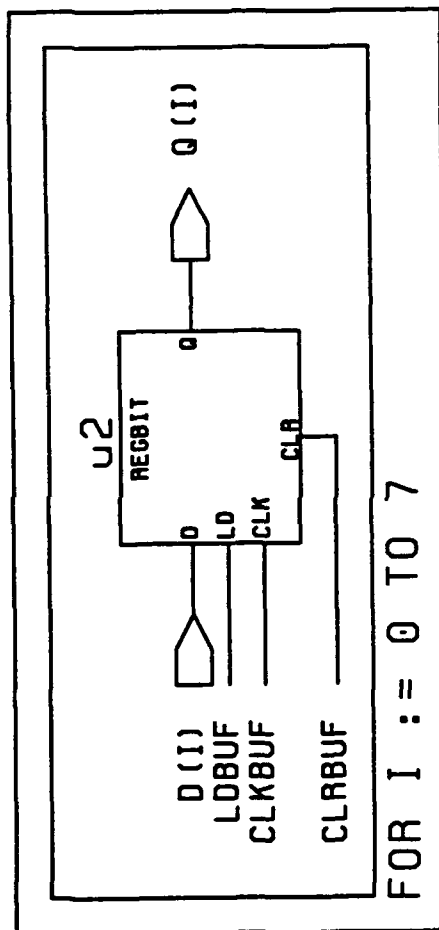
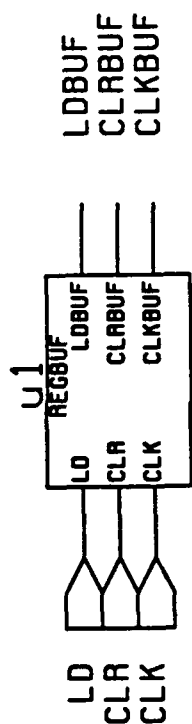
NAME:           DRVR2

DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD



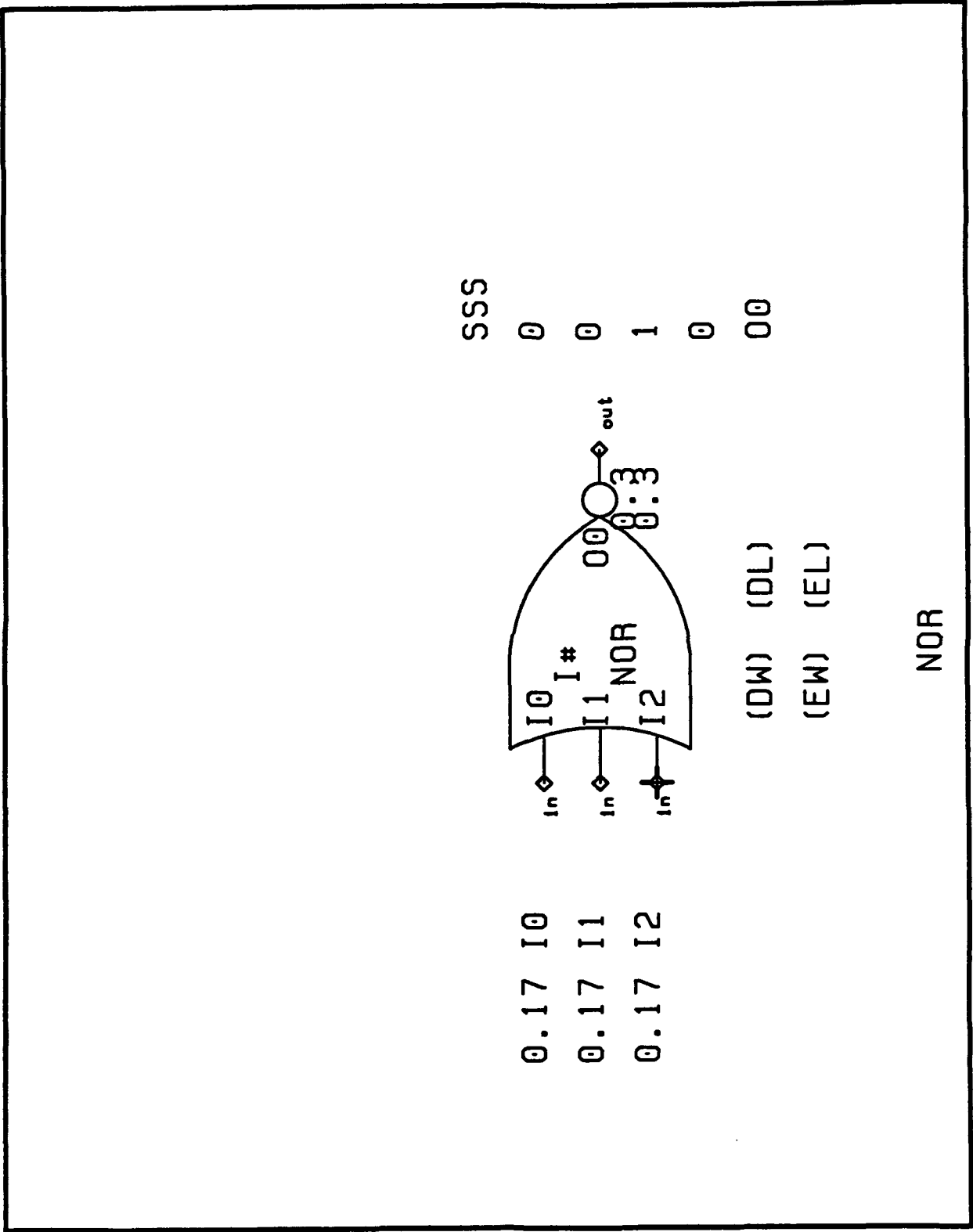


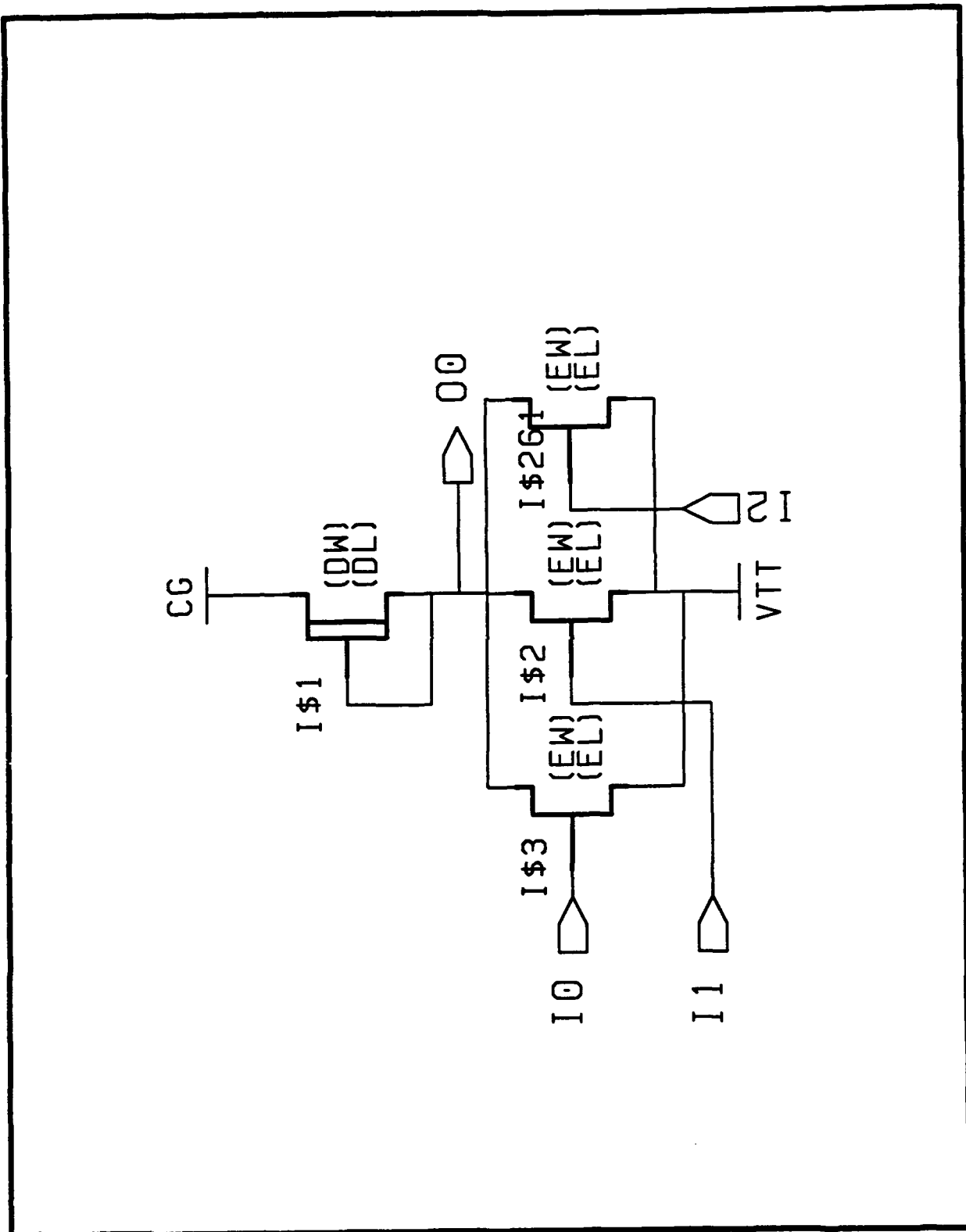


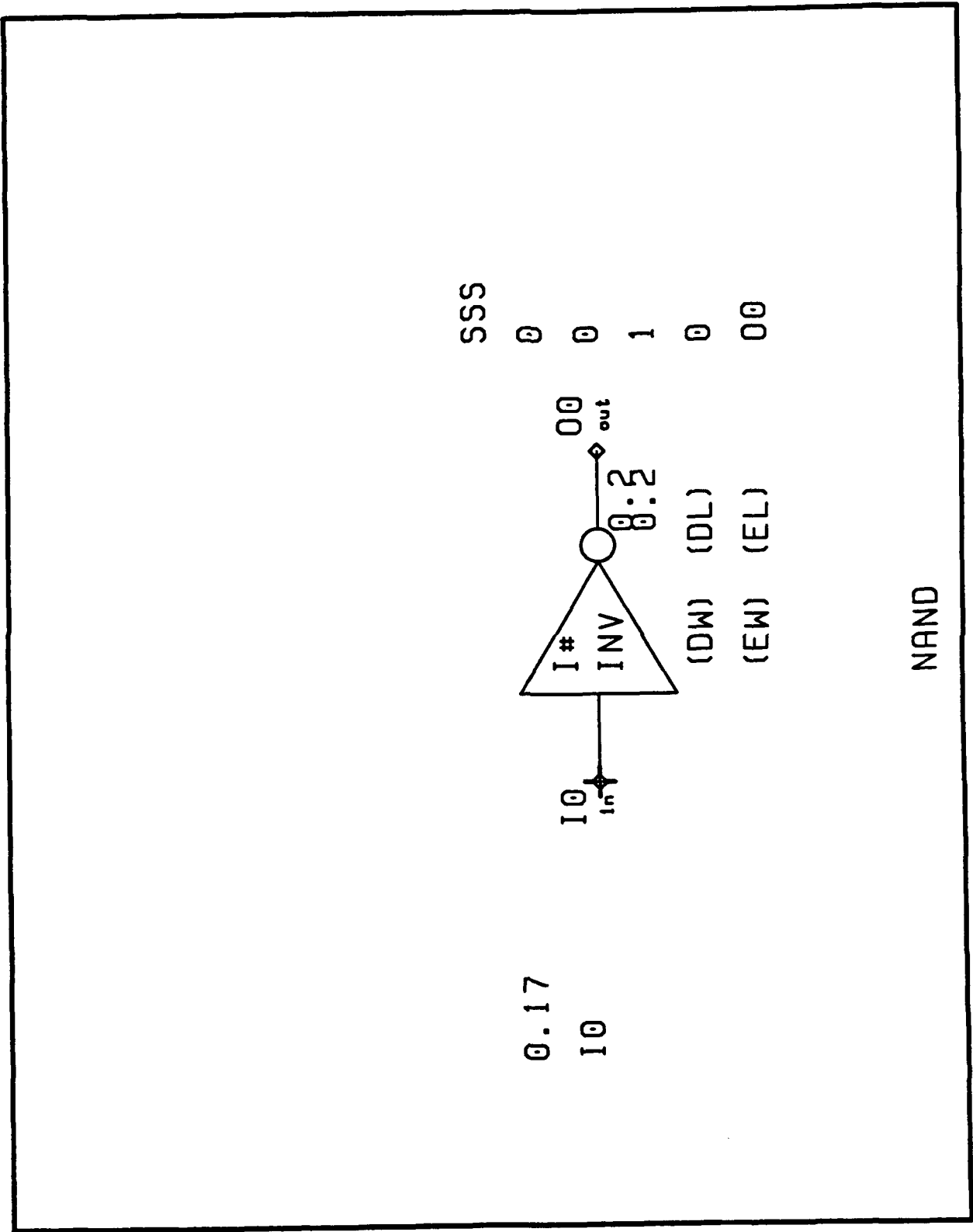


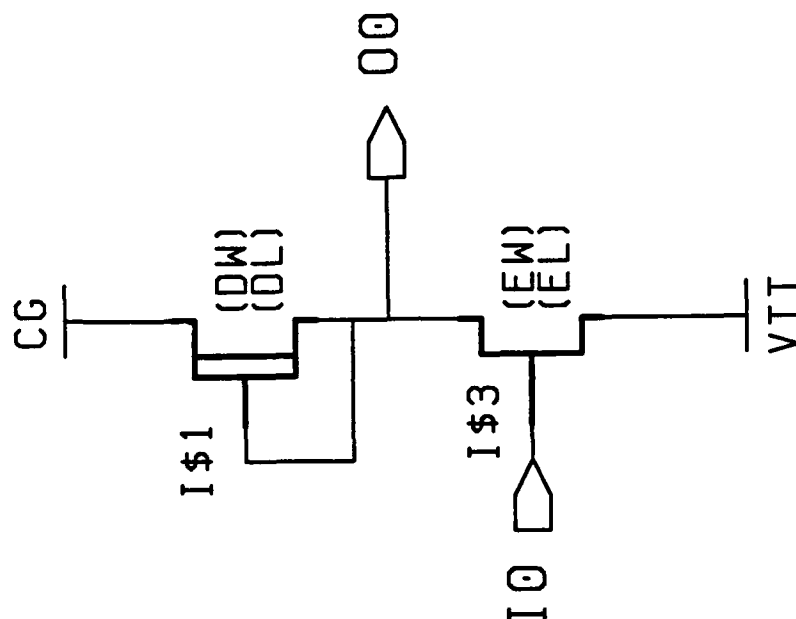
IMR

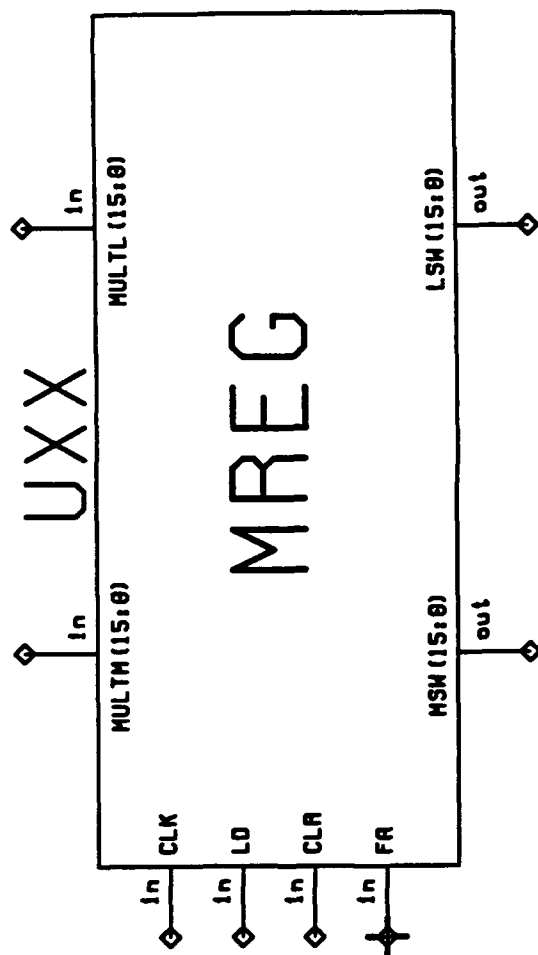


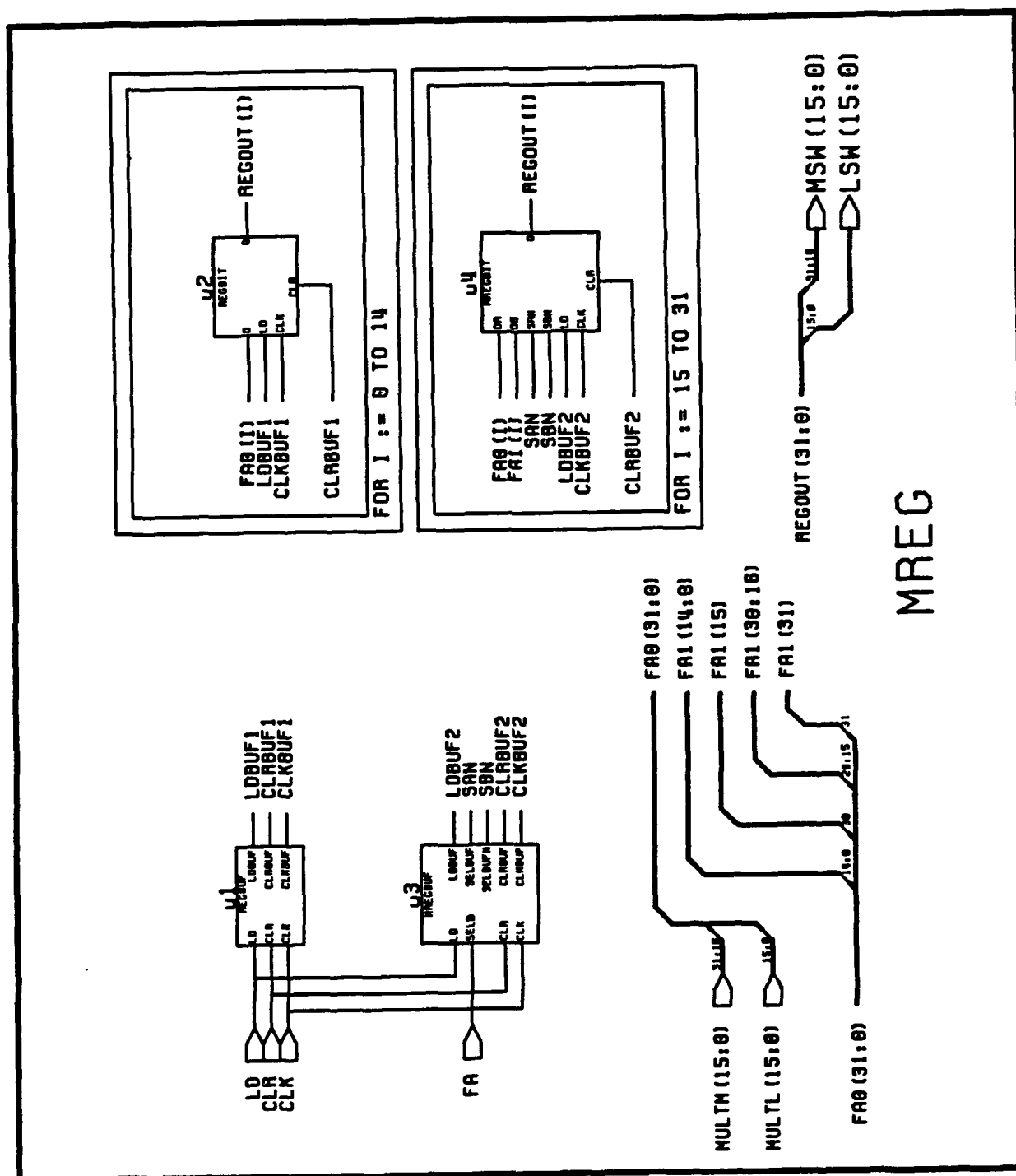


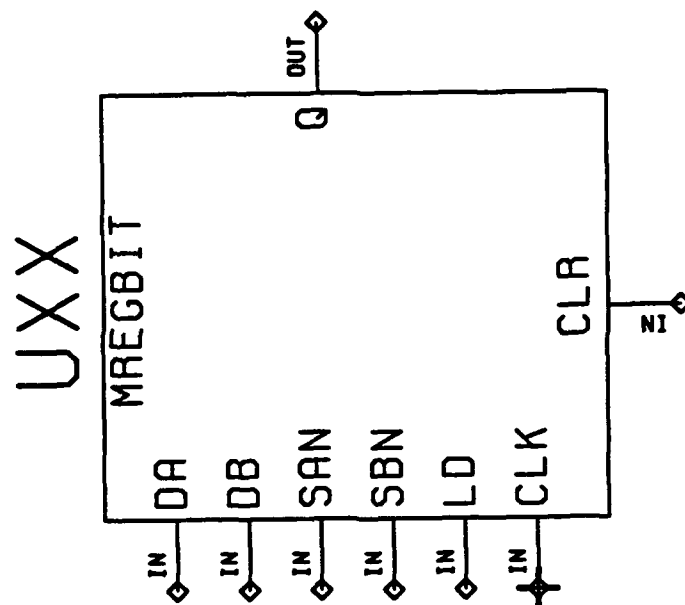


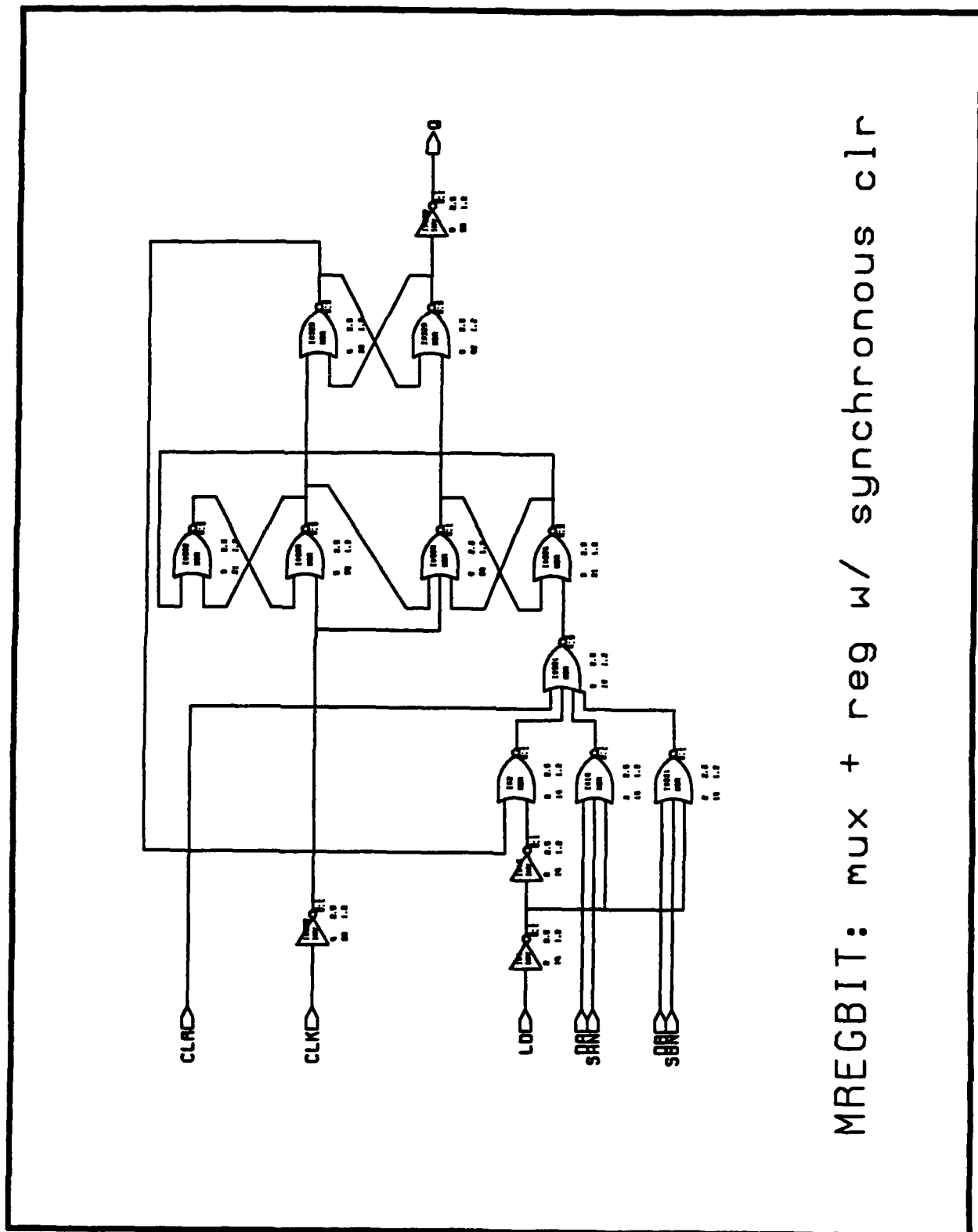




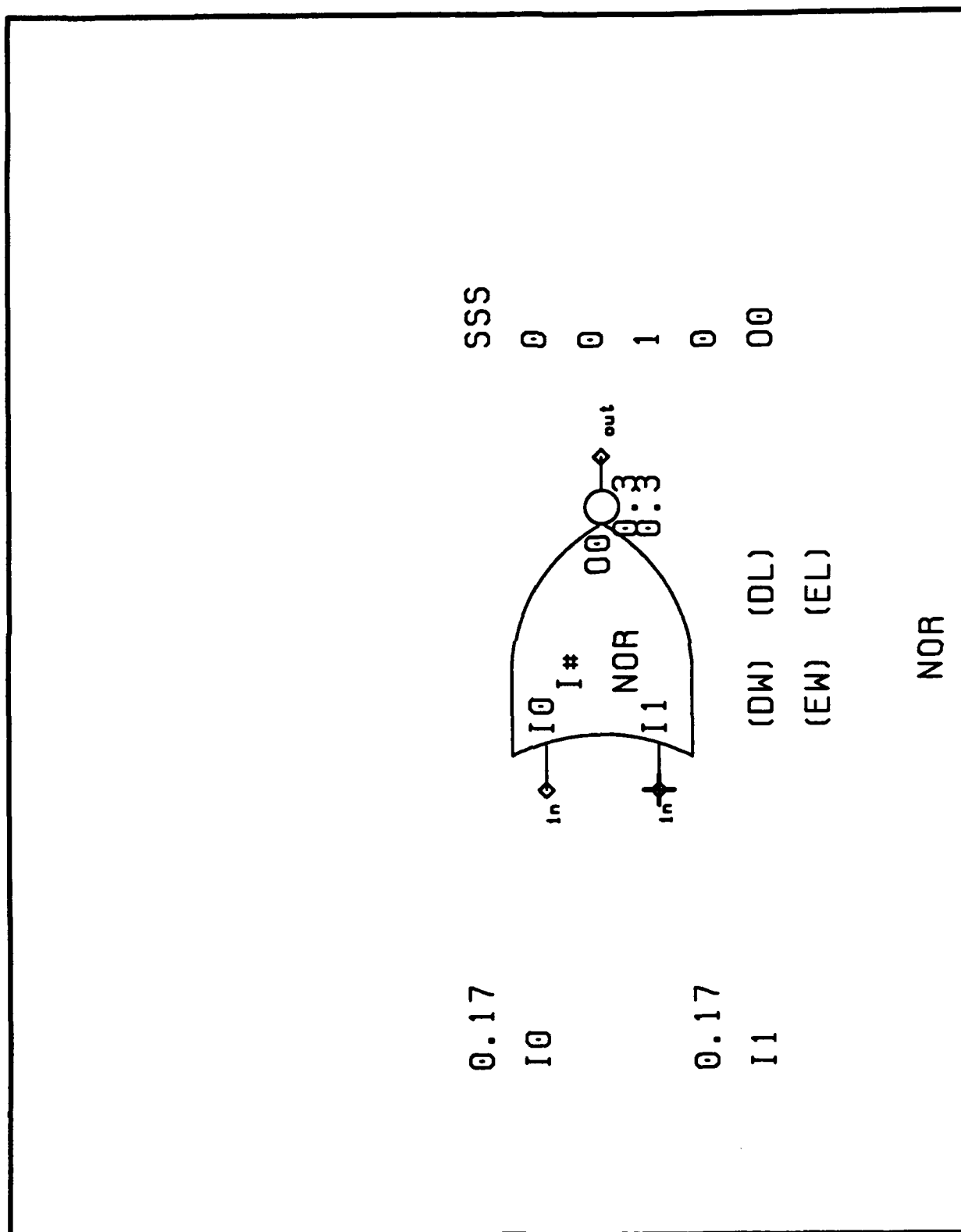


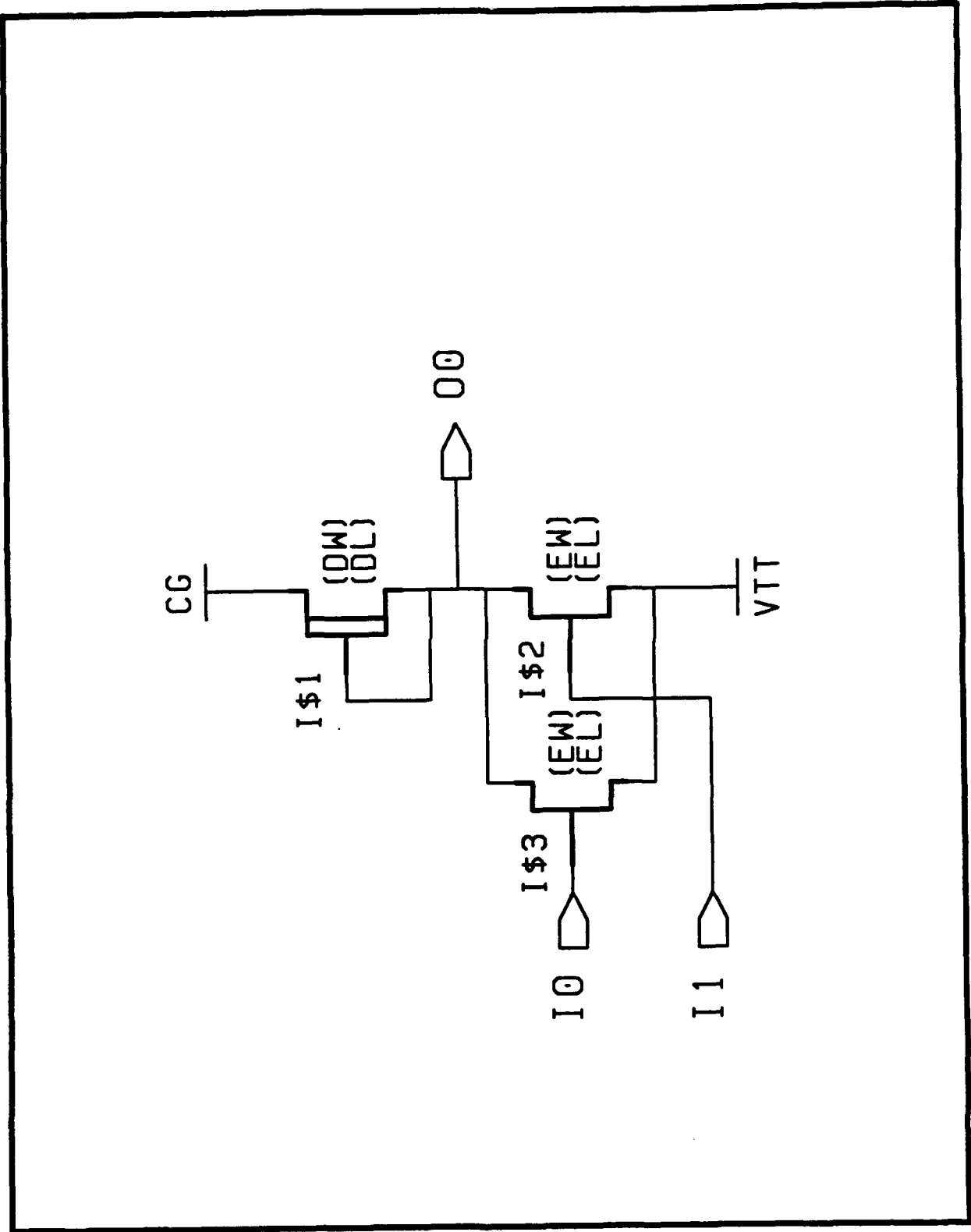


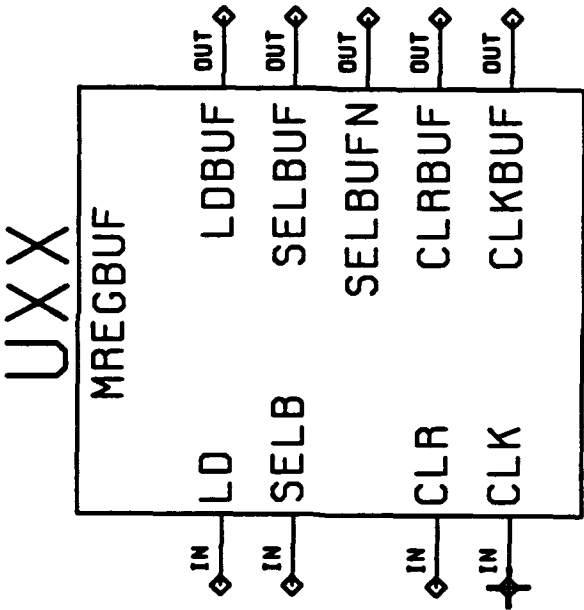


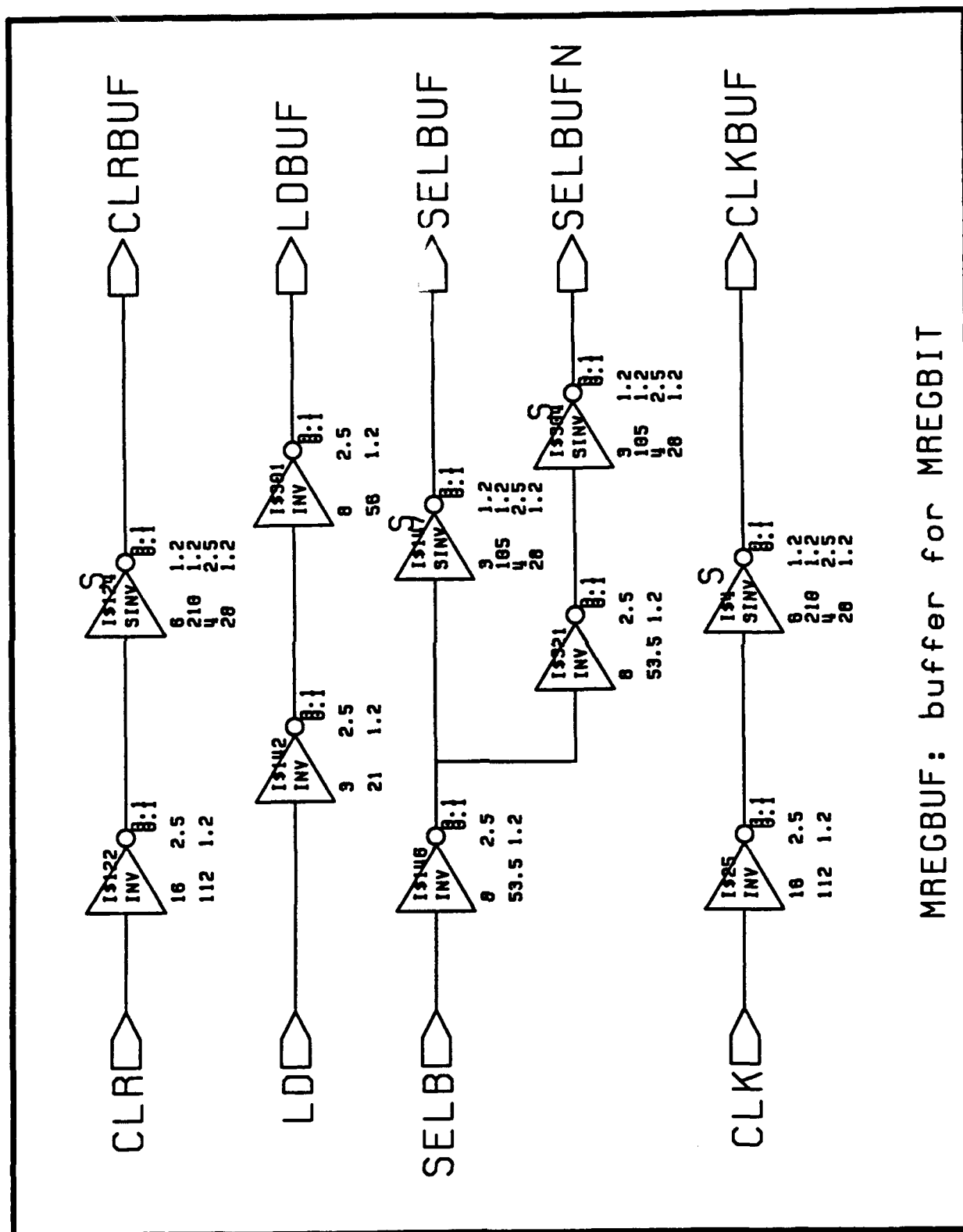




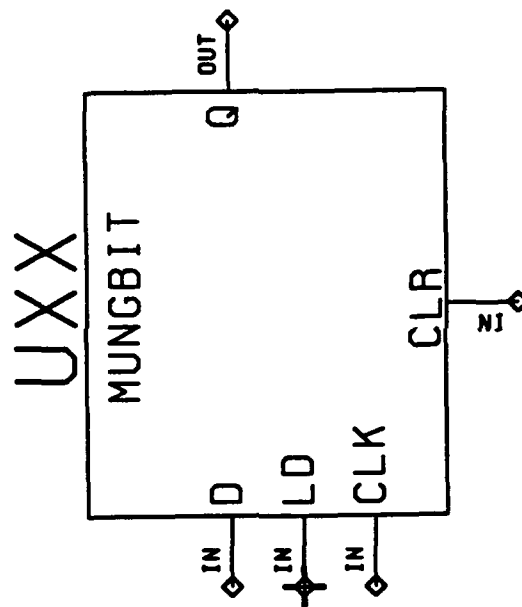


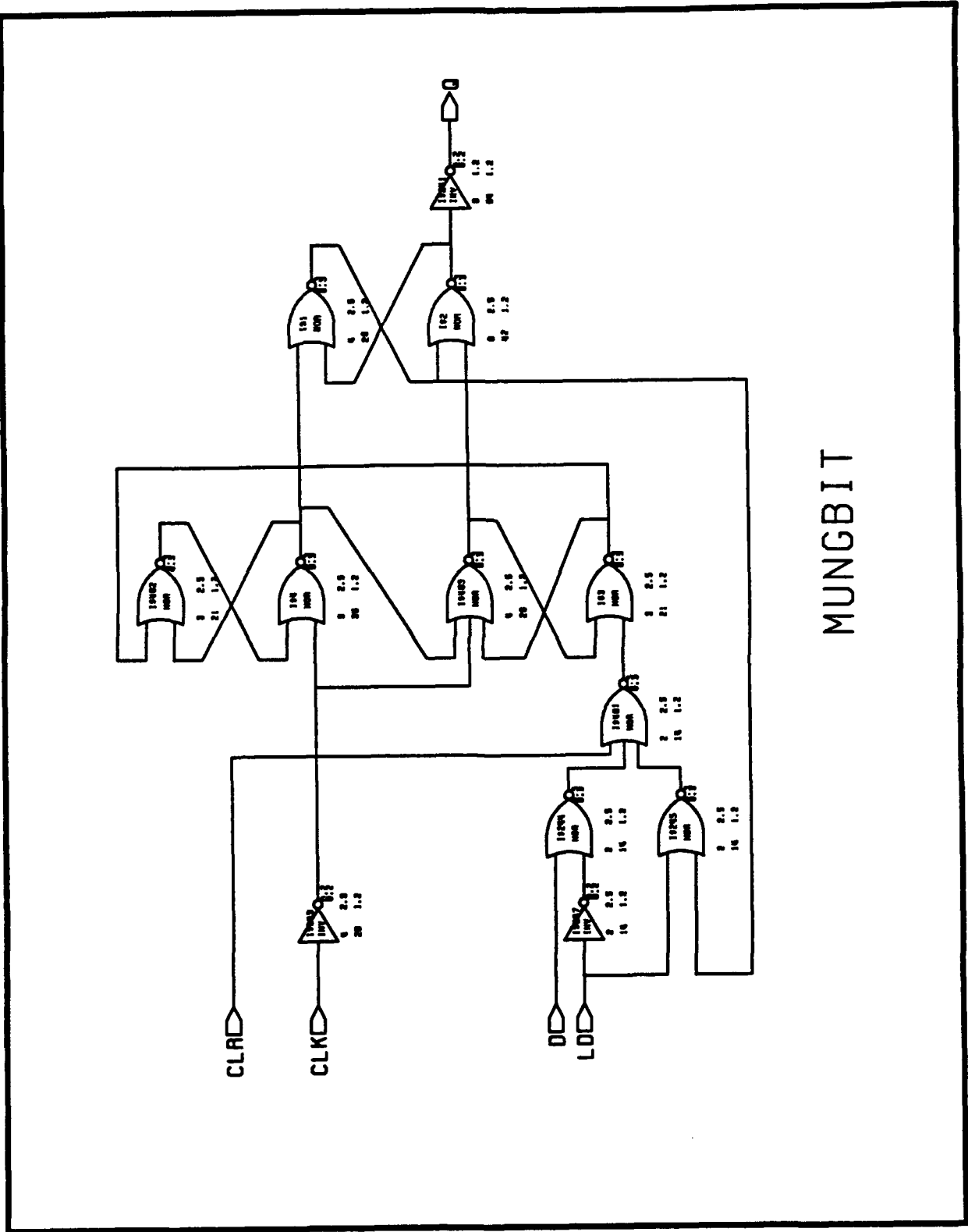


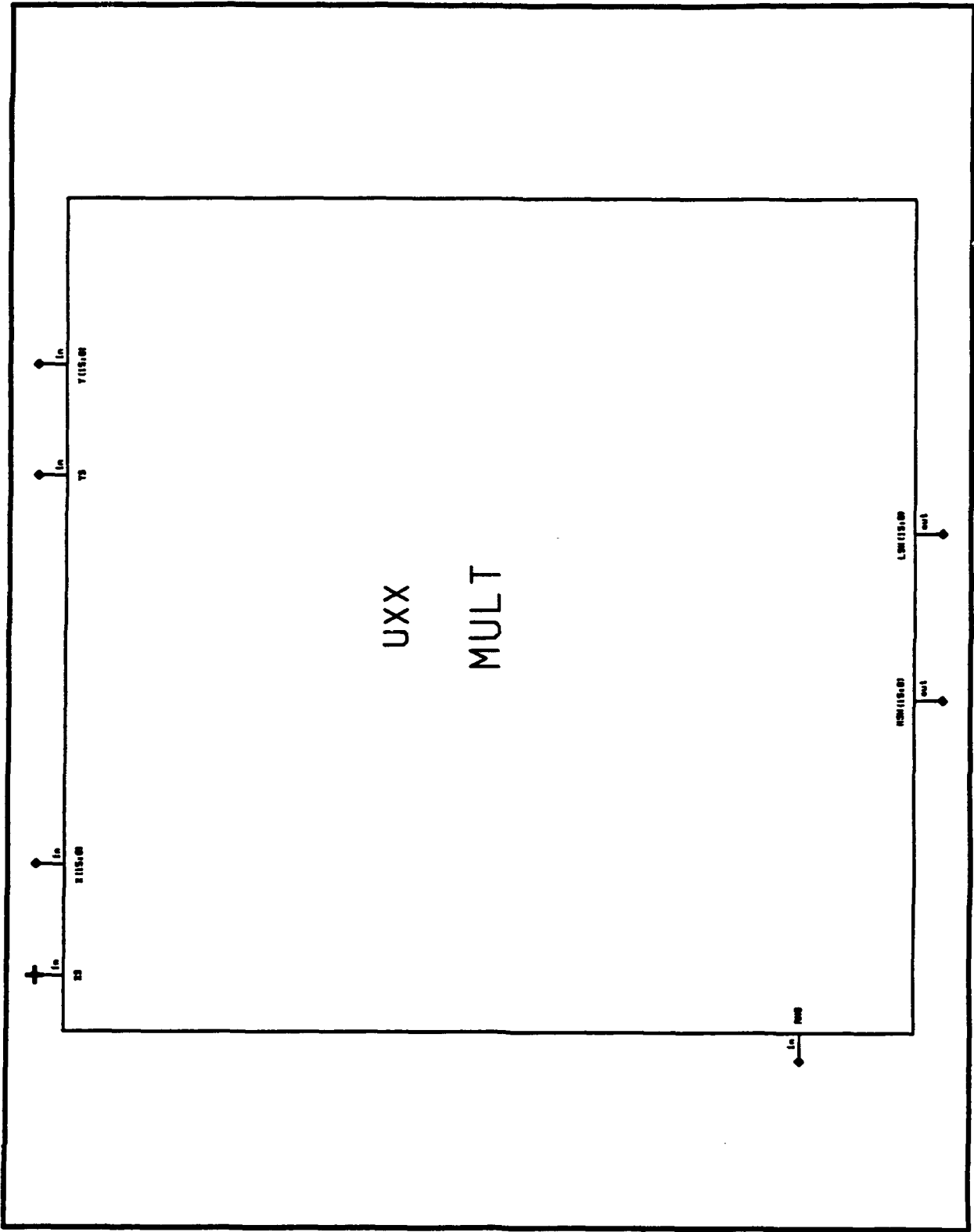


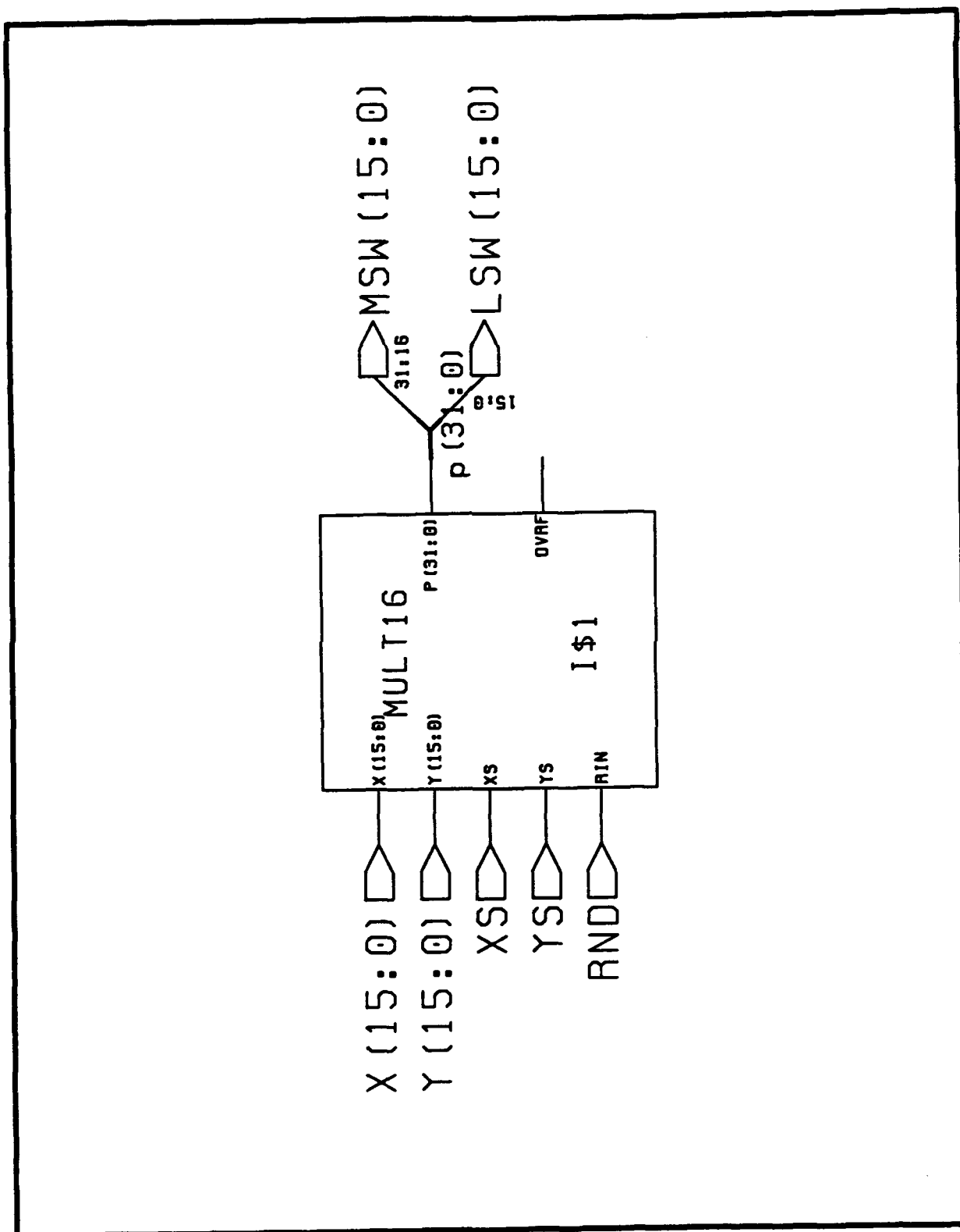


MREGBUF: buffer for MREGBIT

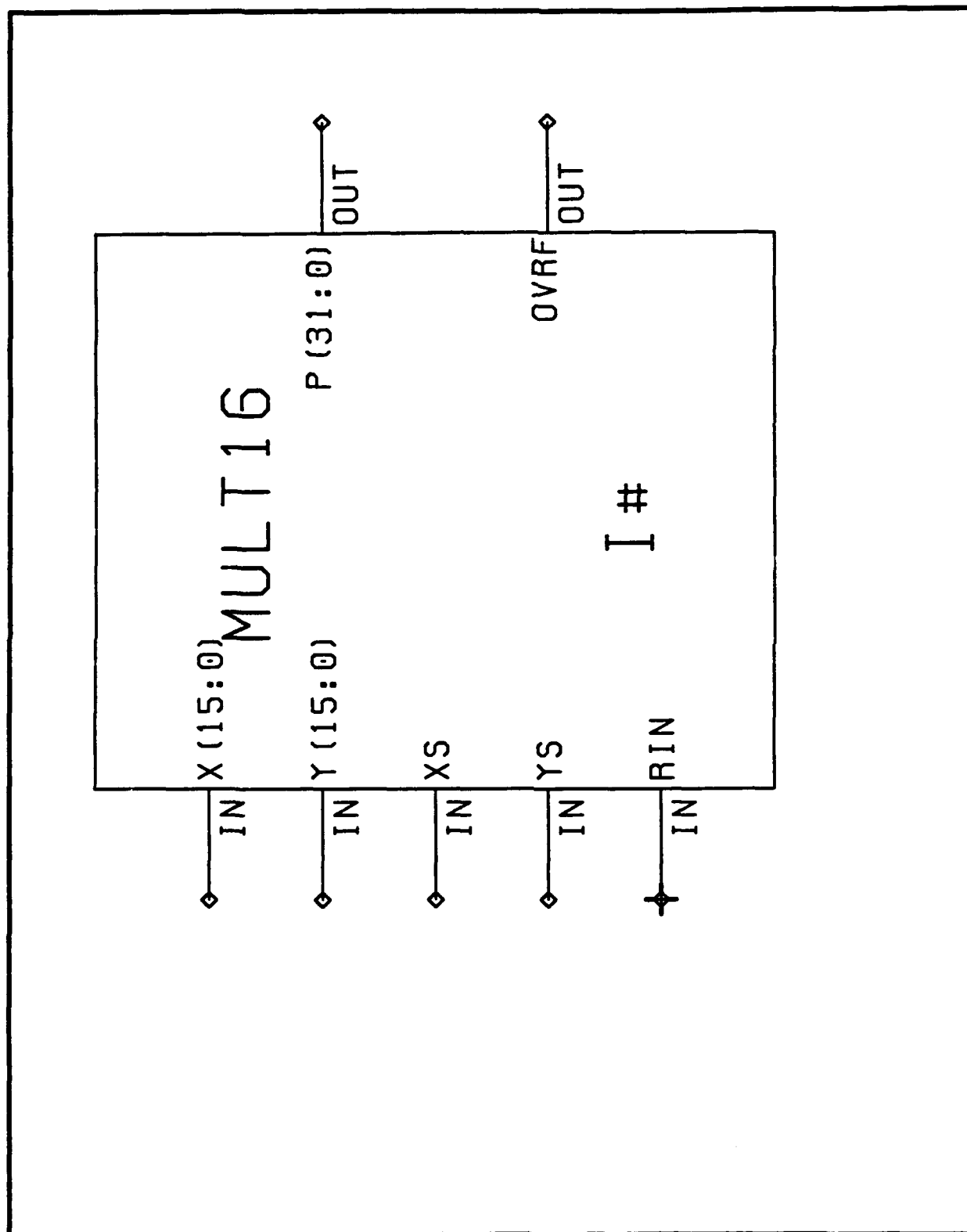


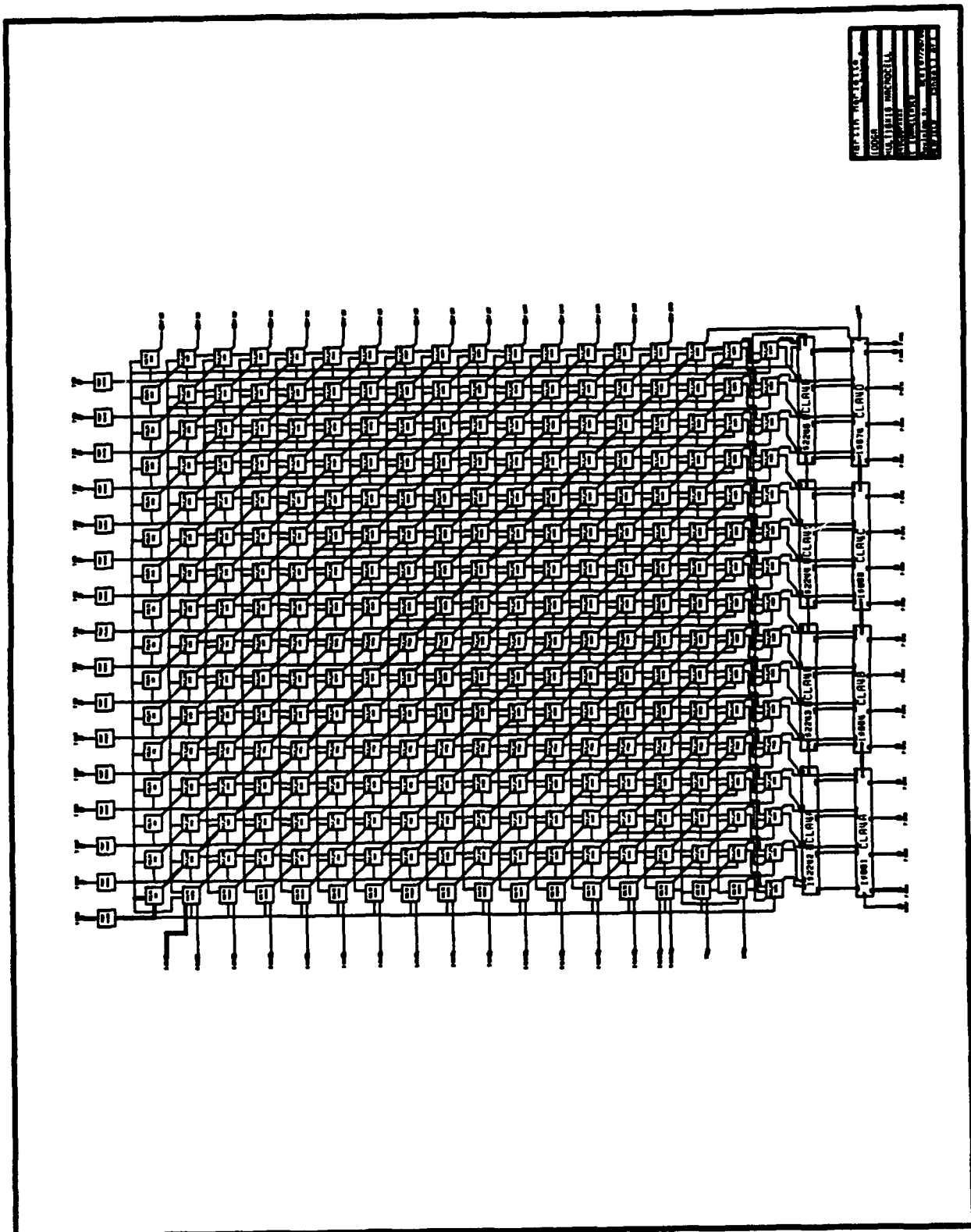


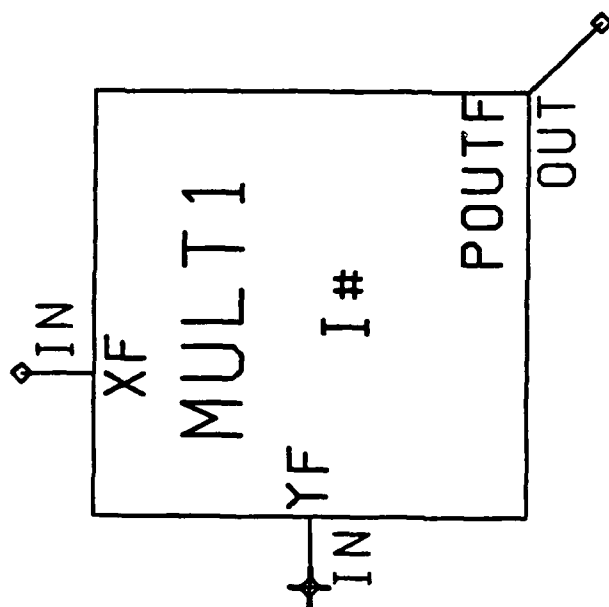




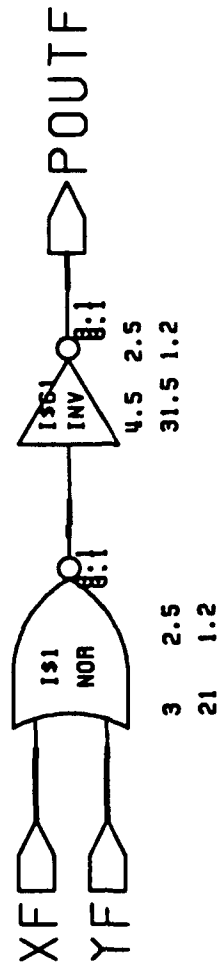


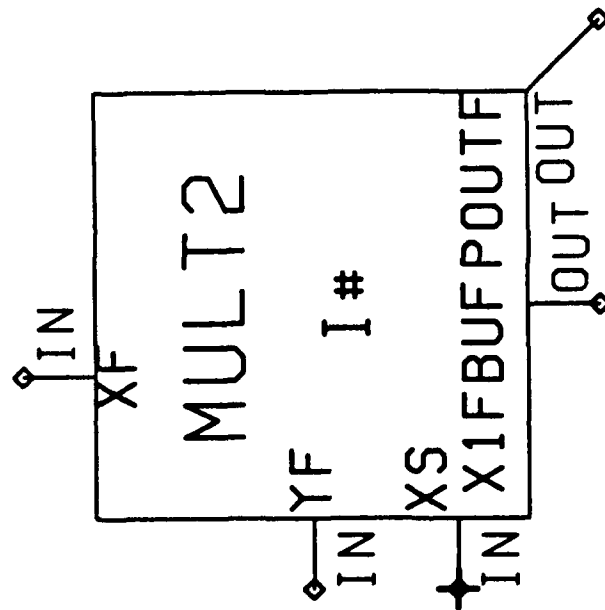




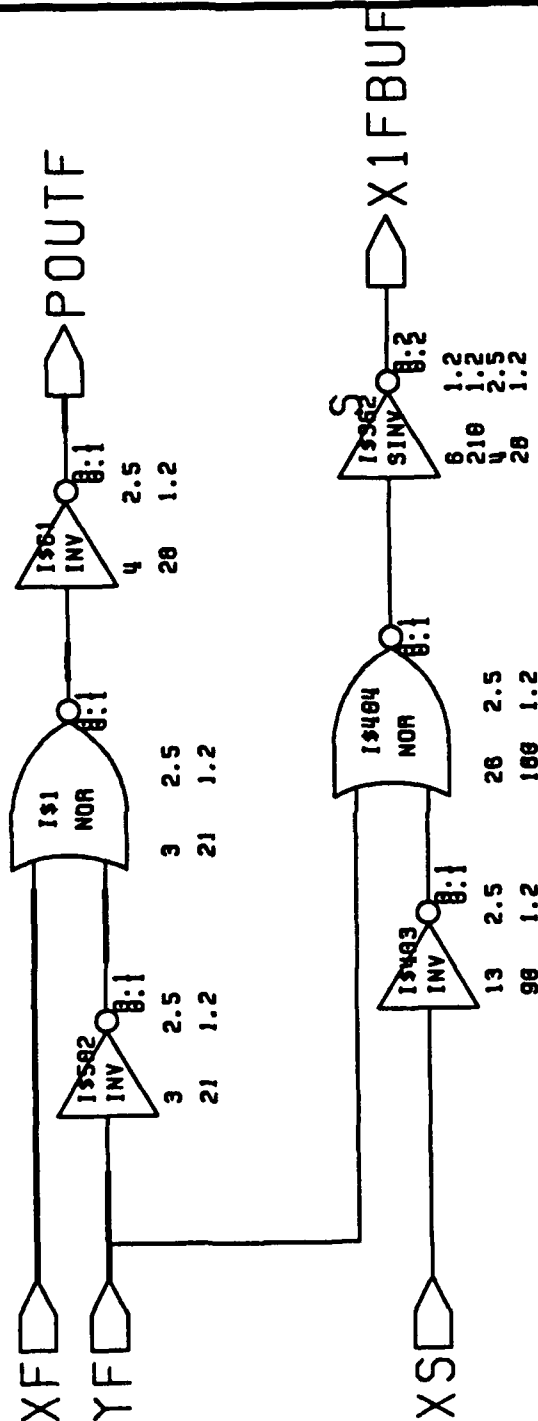


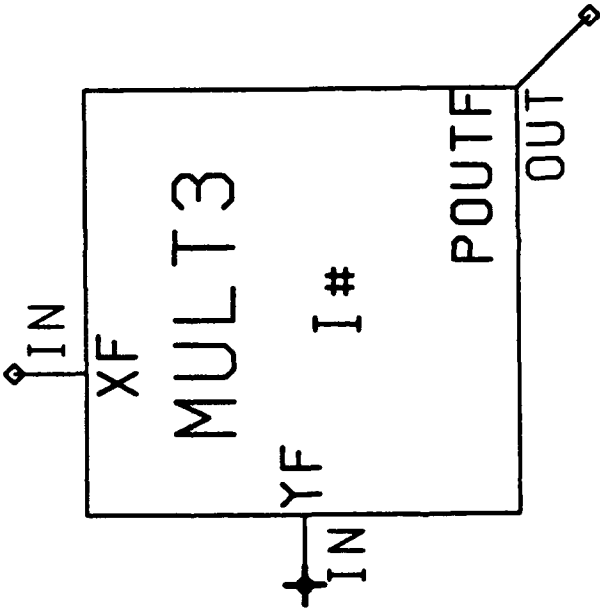
# 16 X 16 MULTIPLIER: MULT1



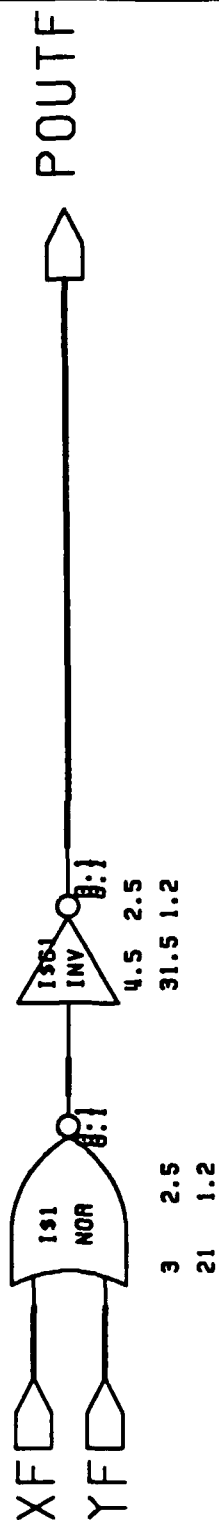


# 16 X 16 MULTIPLIER: MULT2

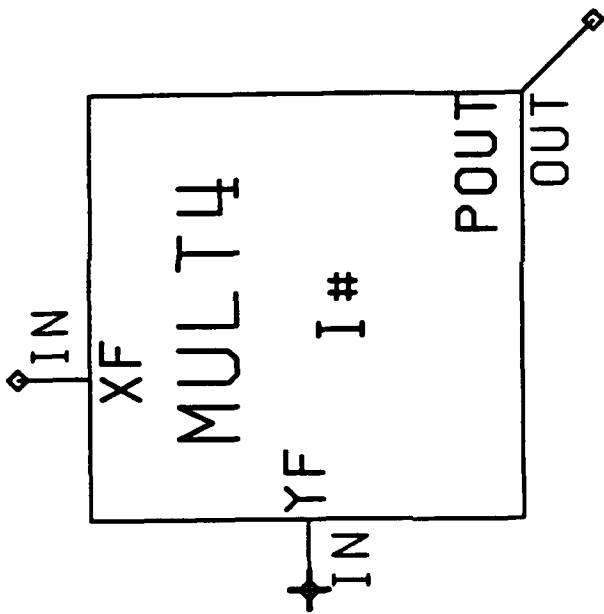




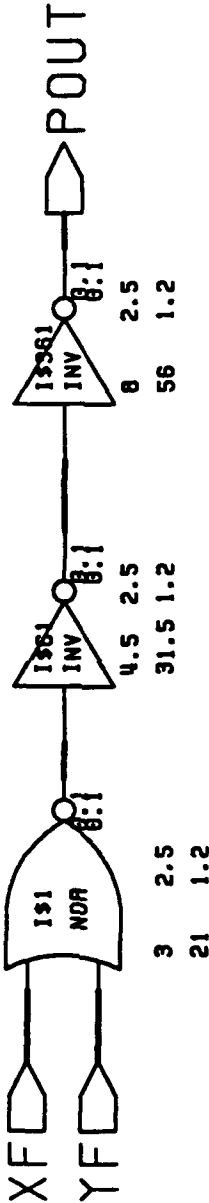
# 16 X 16 MULTIPLIER: MULT3

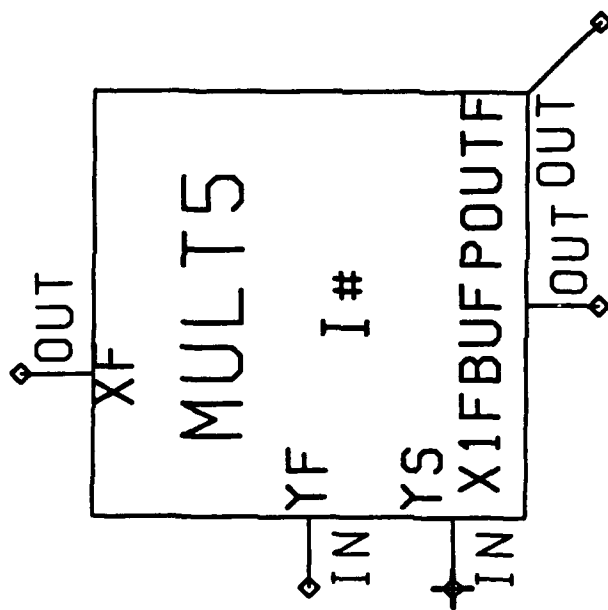




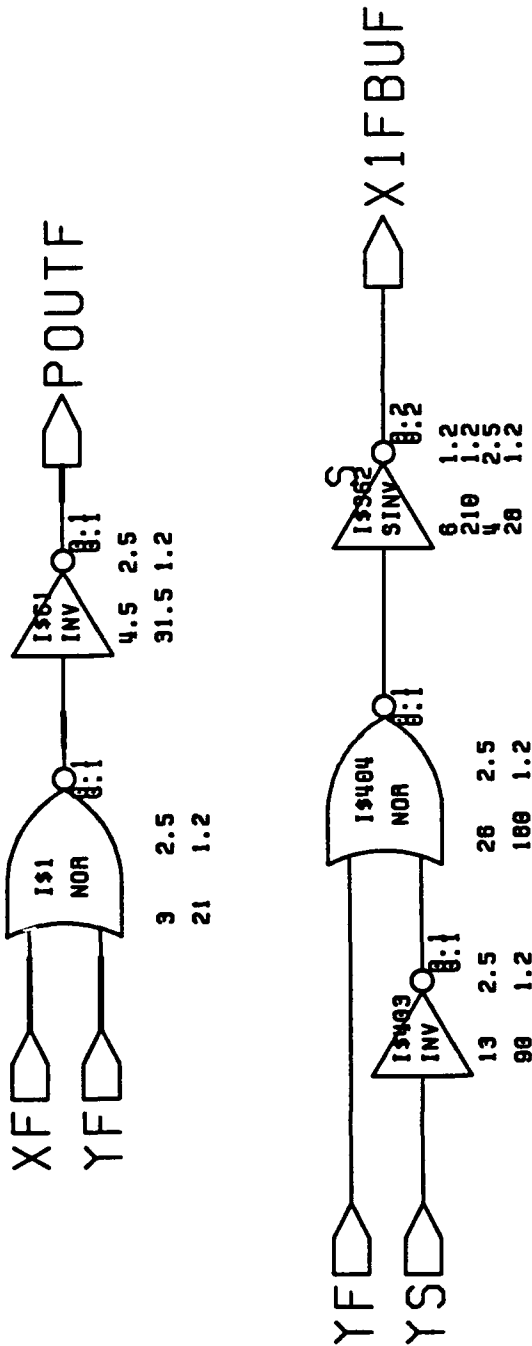


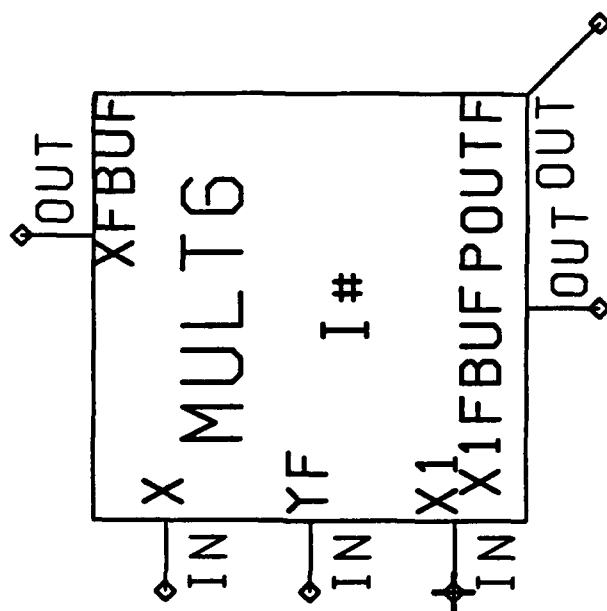
16 X 16 MULTIPLIER: MULT4



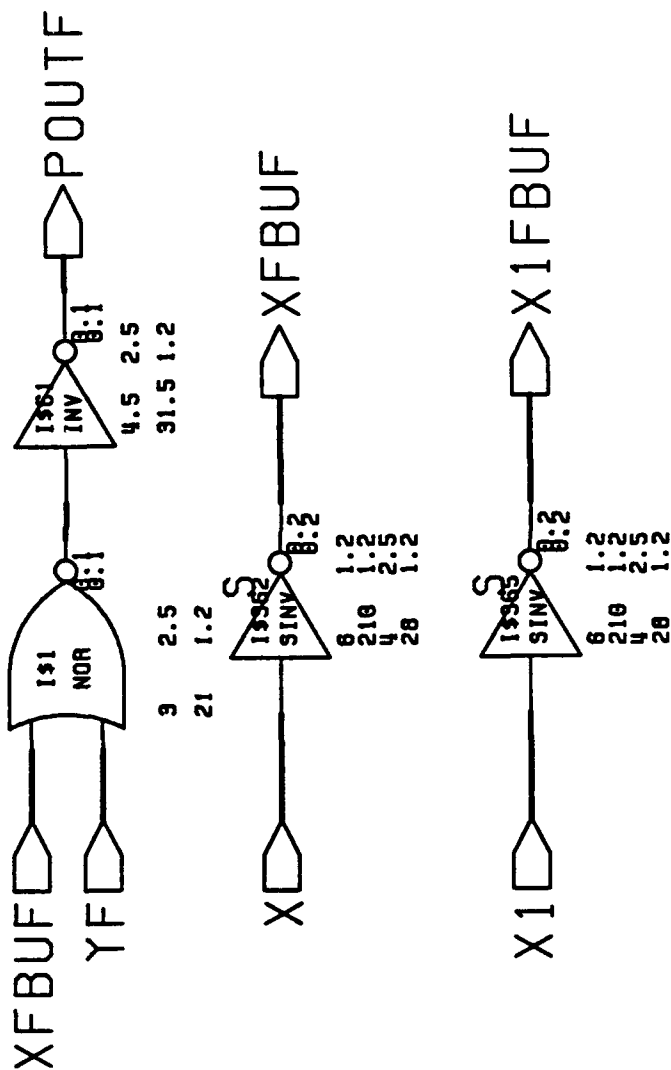


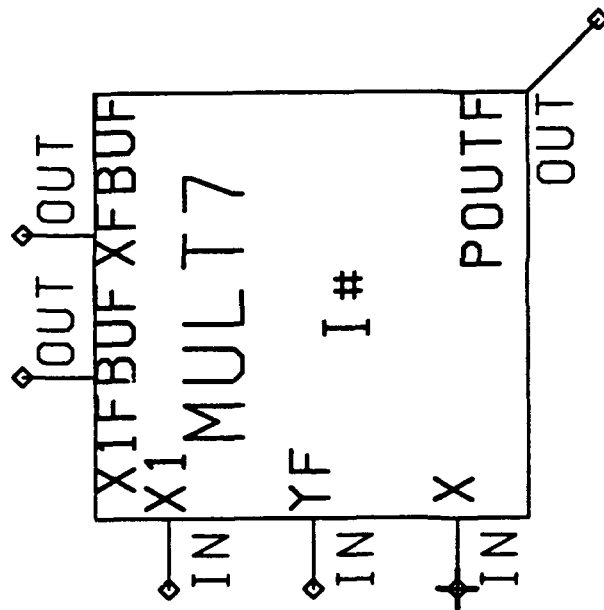
16 X 16 MULTIPLIER: MULT5



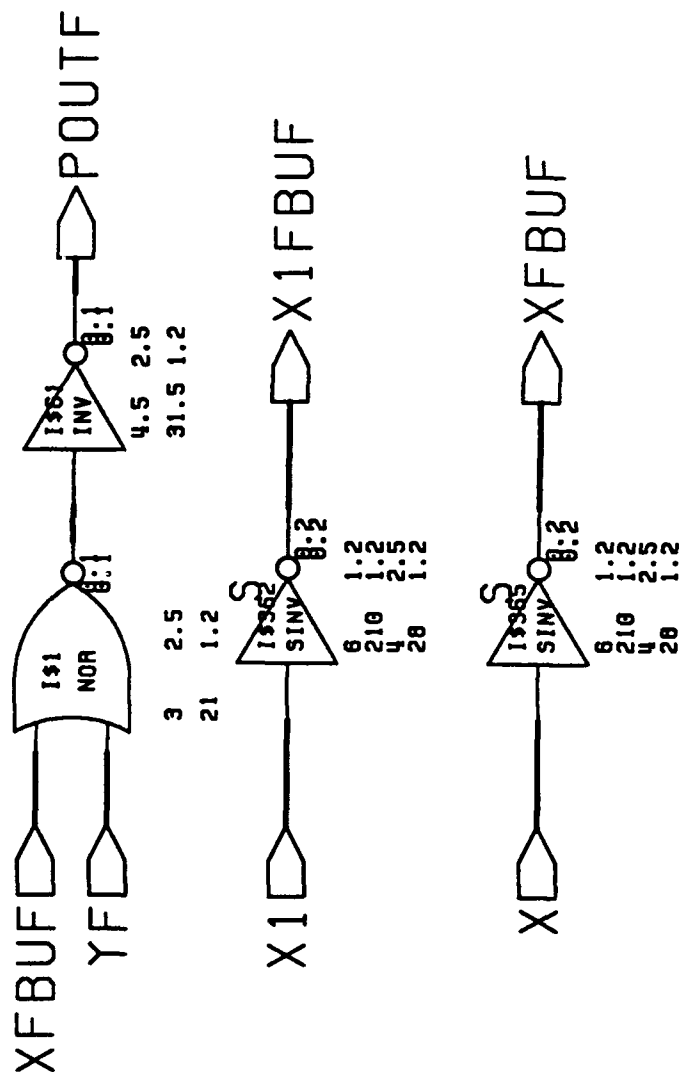


# 16 X 16 MULTIPLIER: MULT6

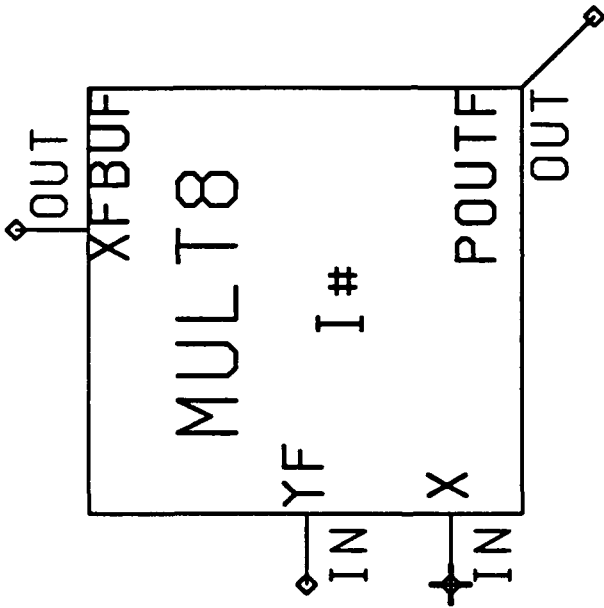




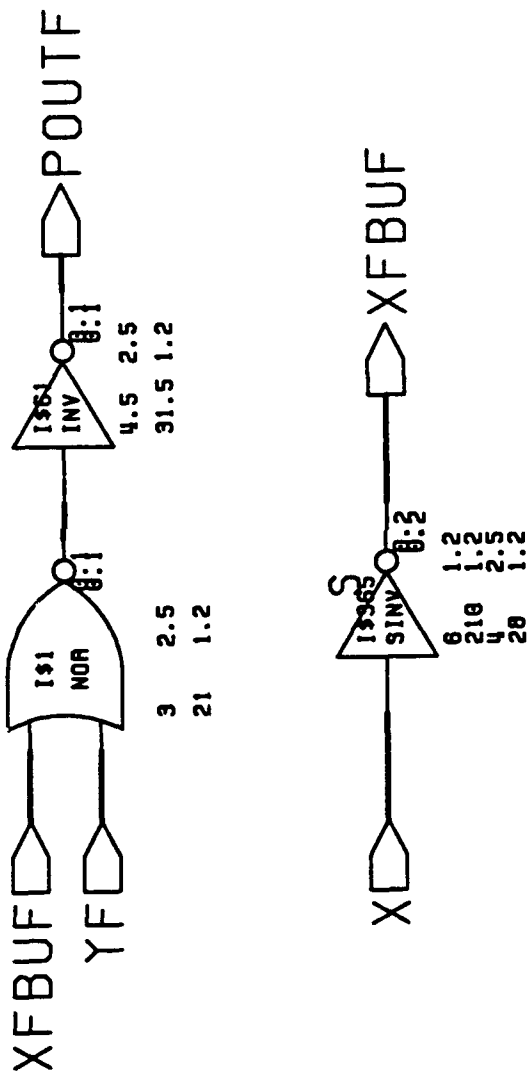
# 16 X 16 MULTIPLIER: MULT7

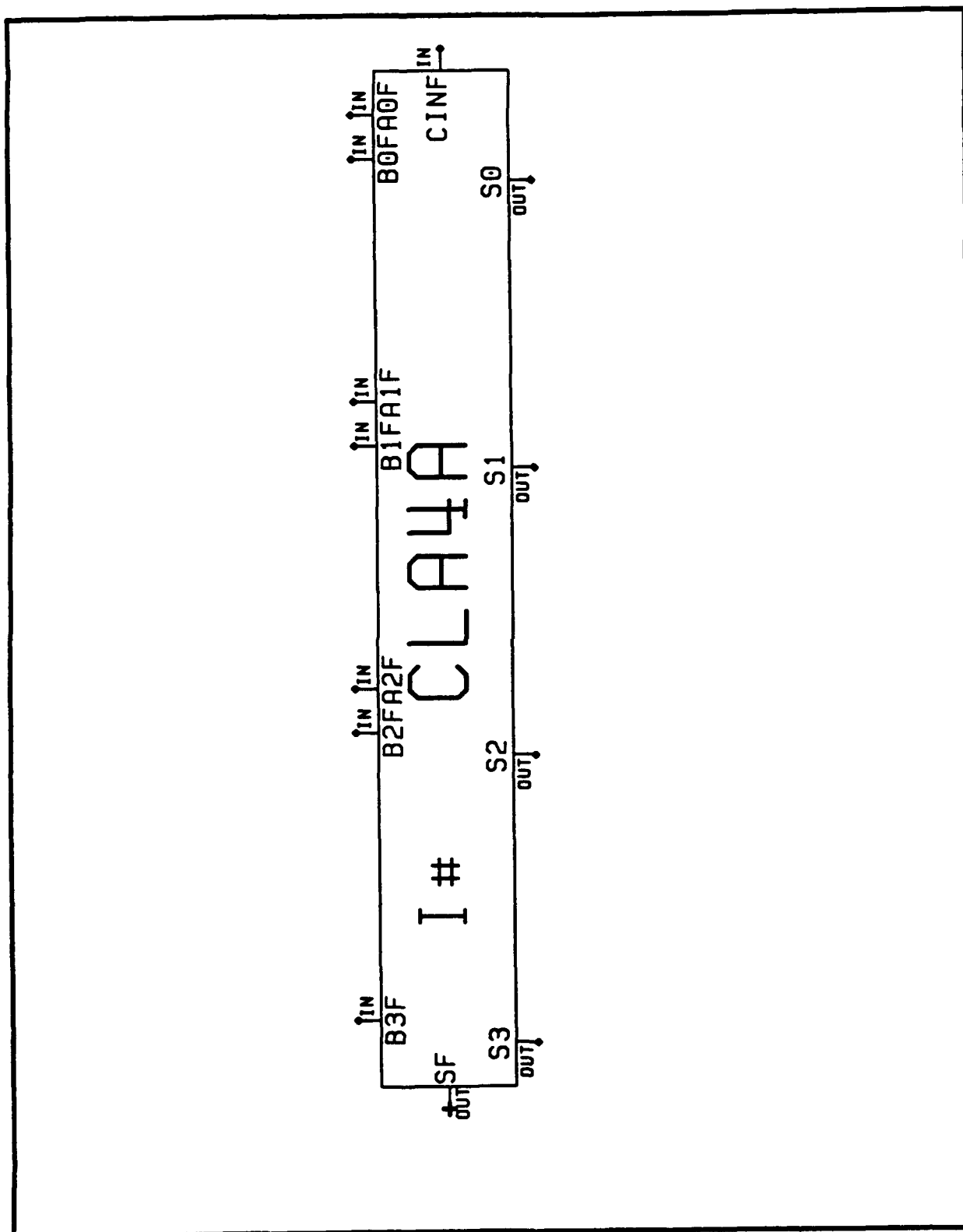


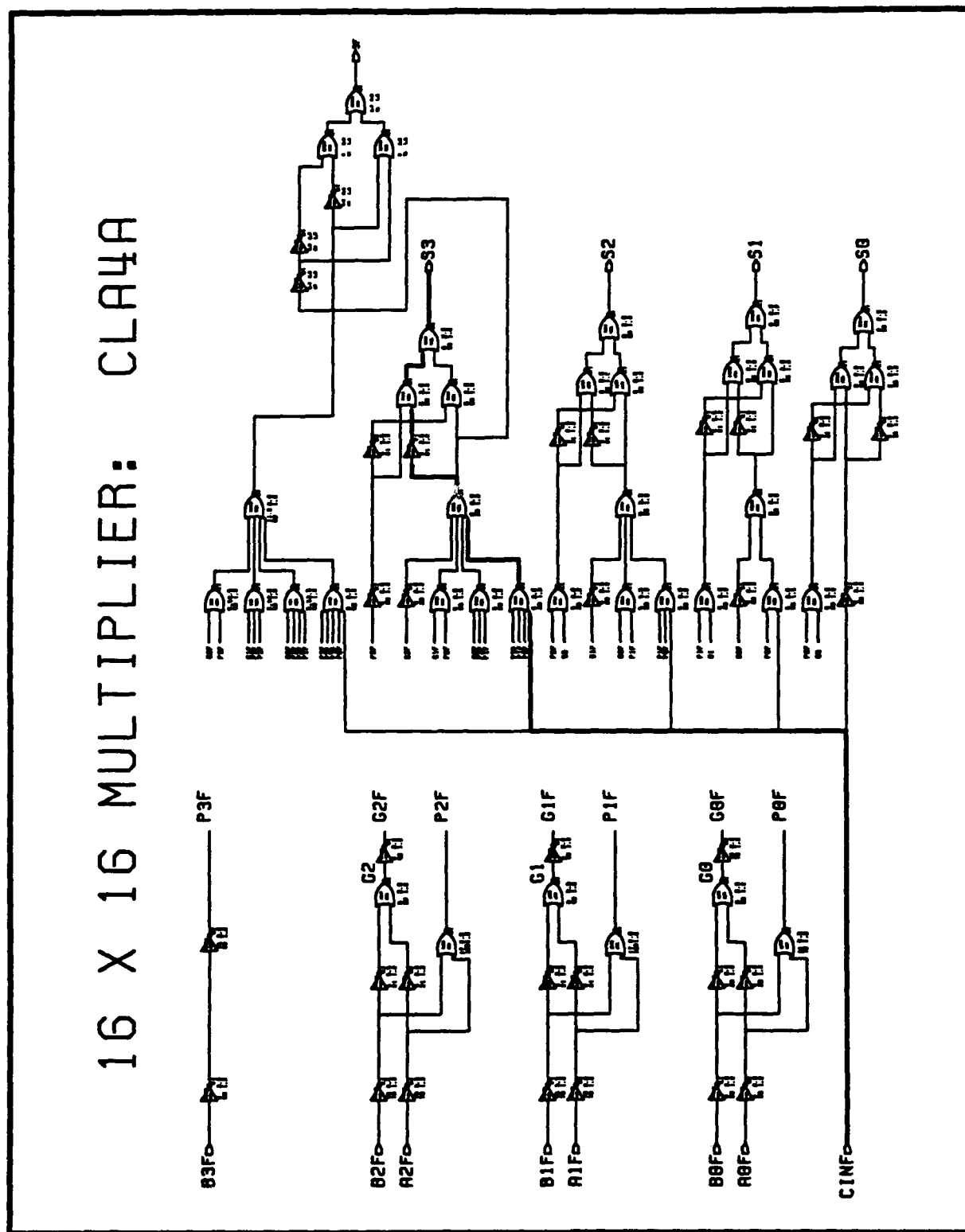


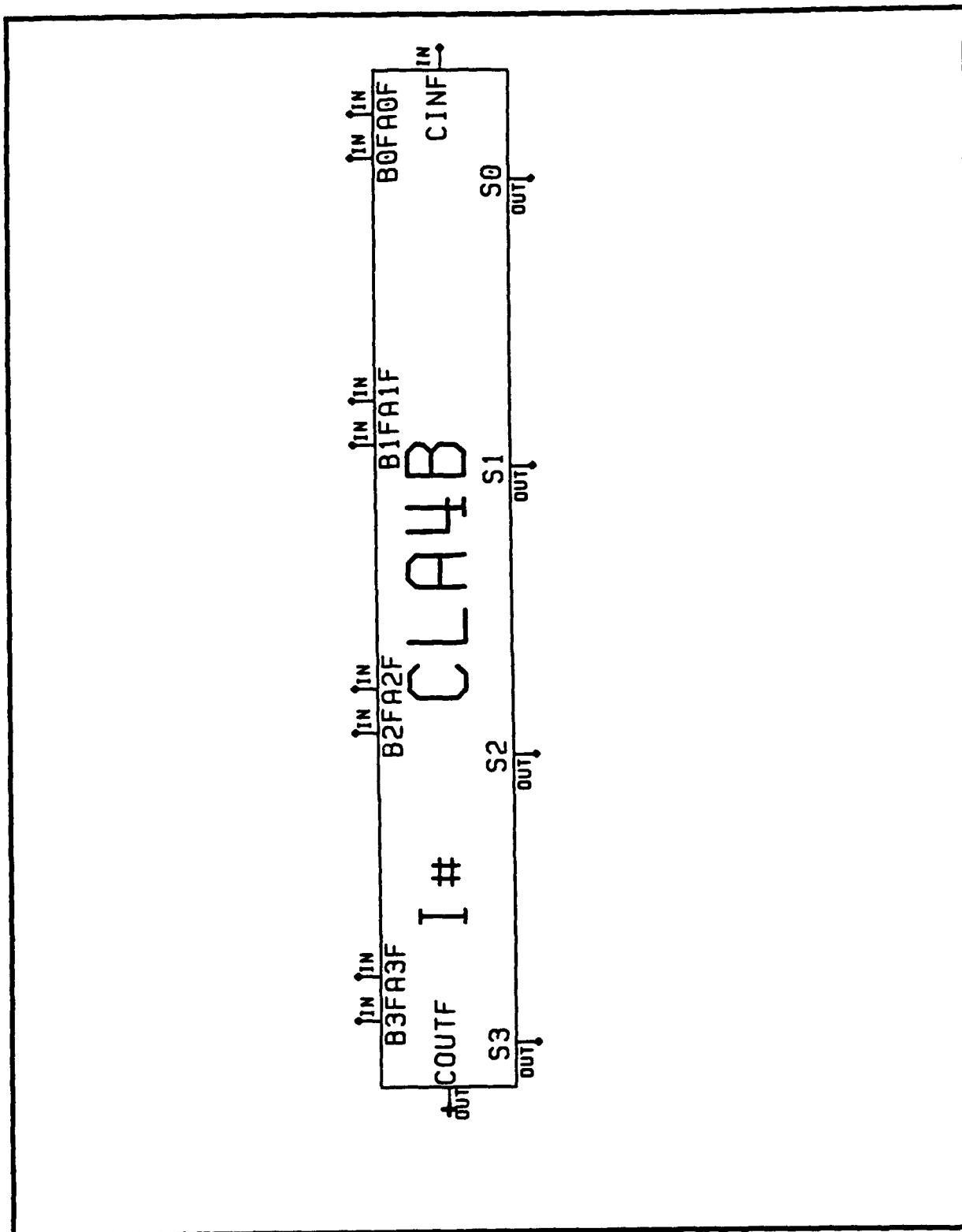


# 16 X 16 MULTIPLIER: MULT8

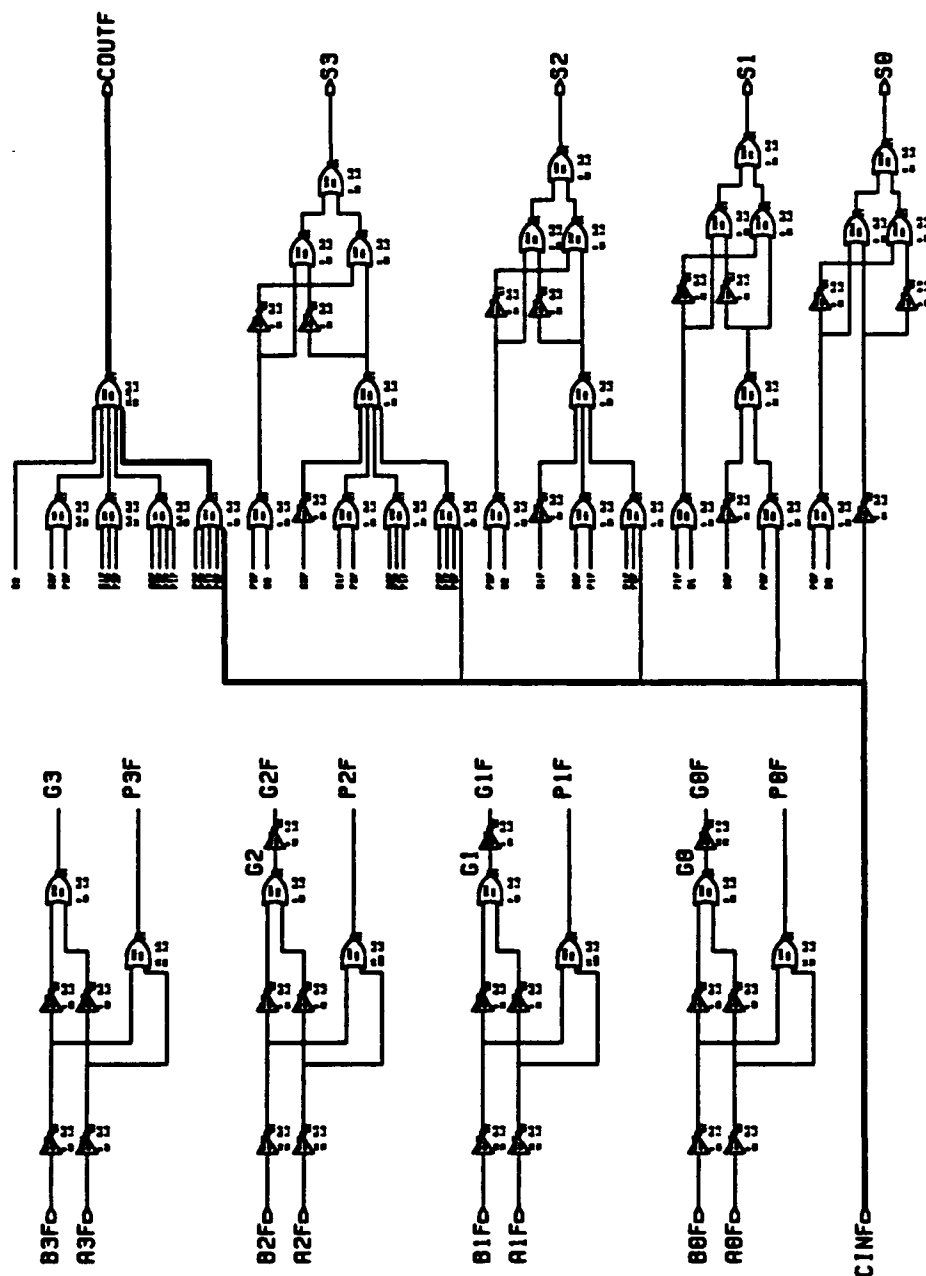


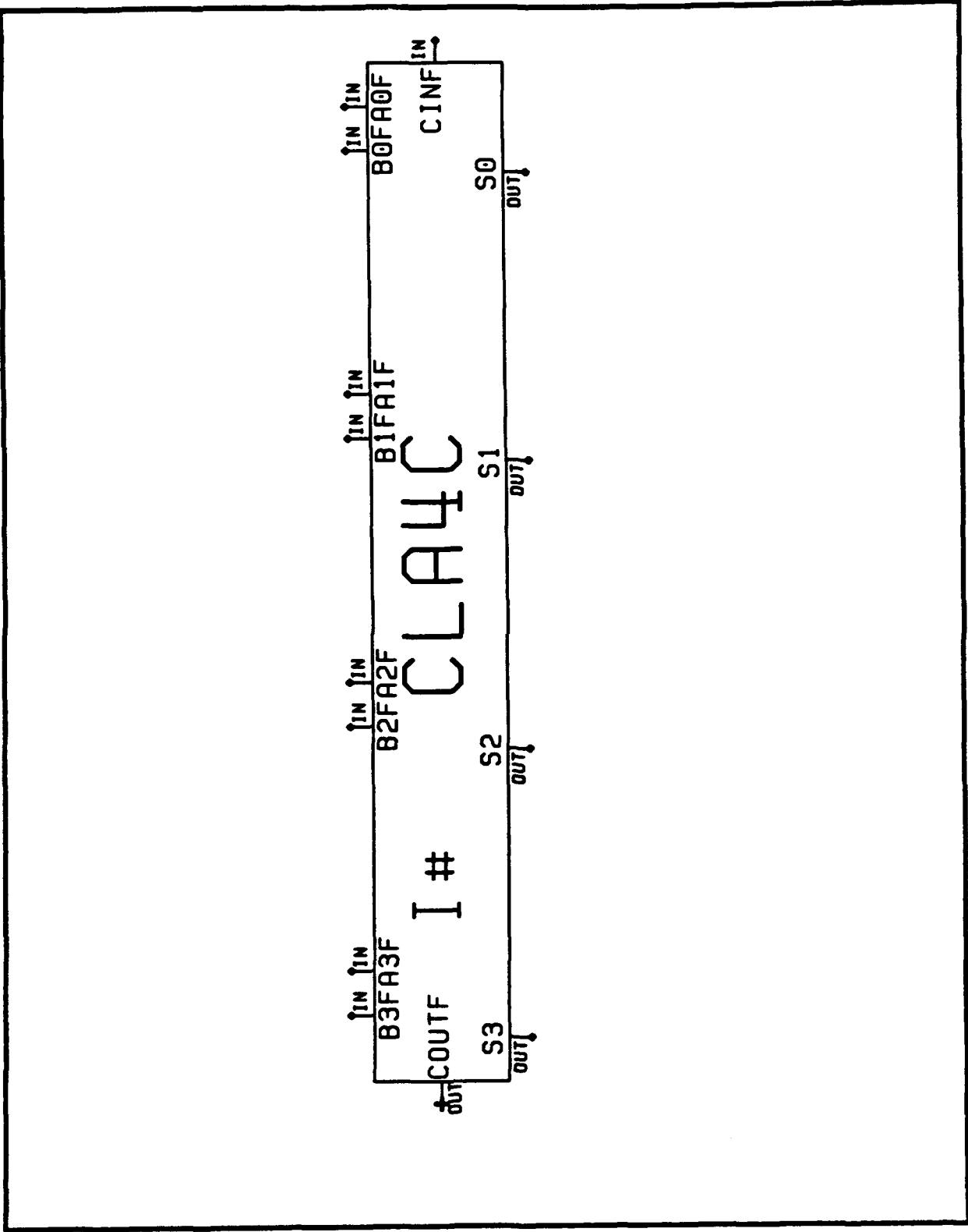


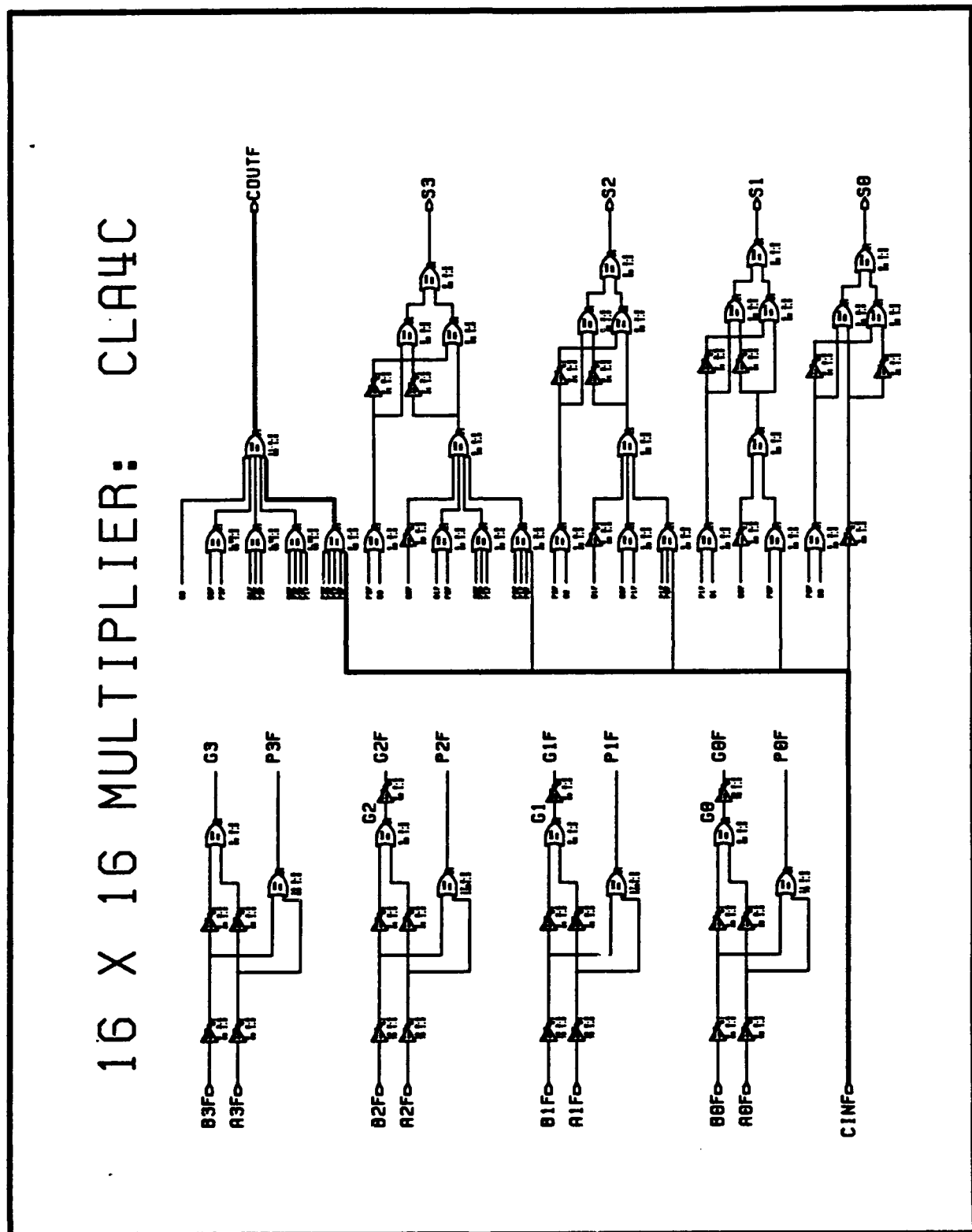




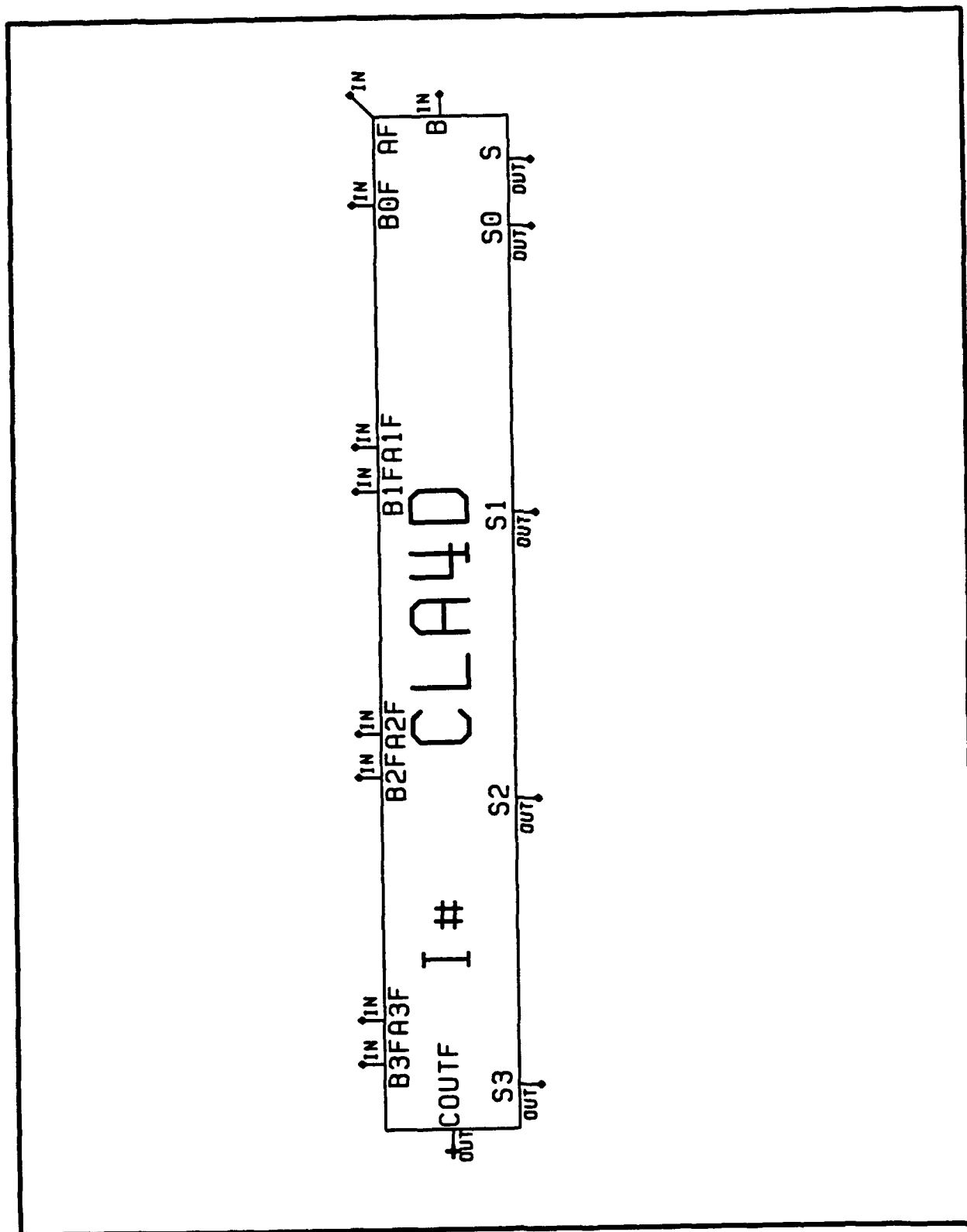
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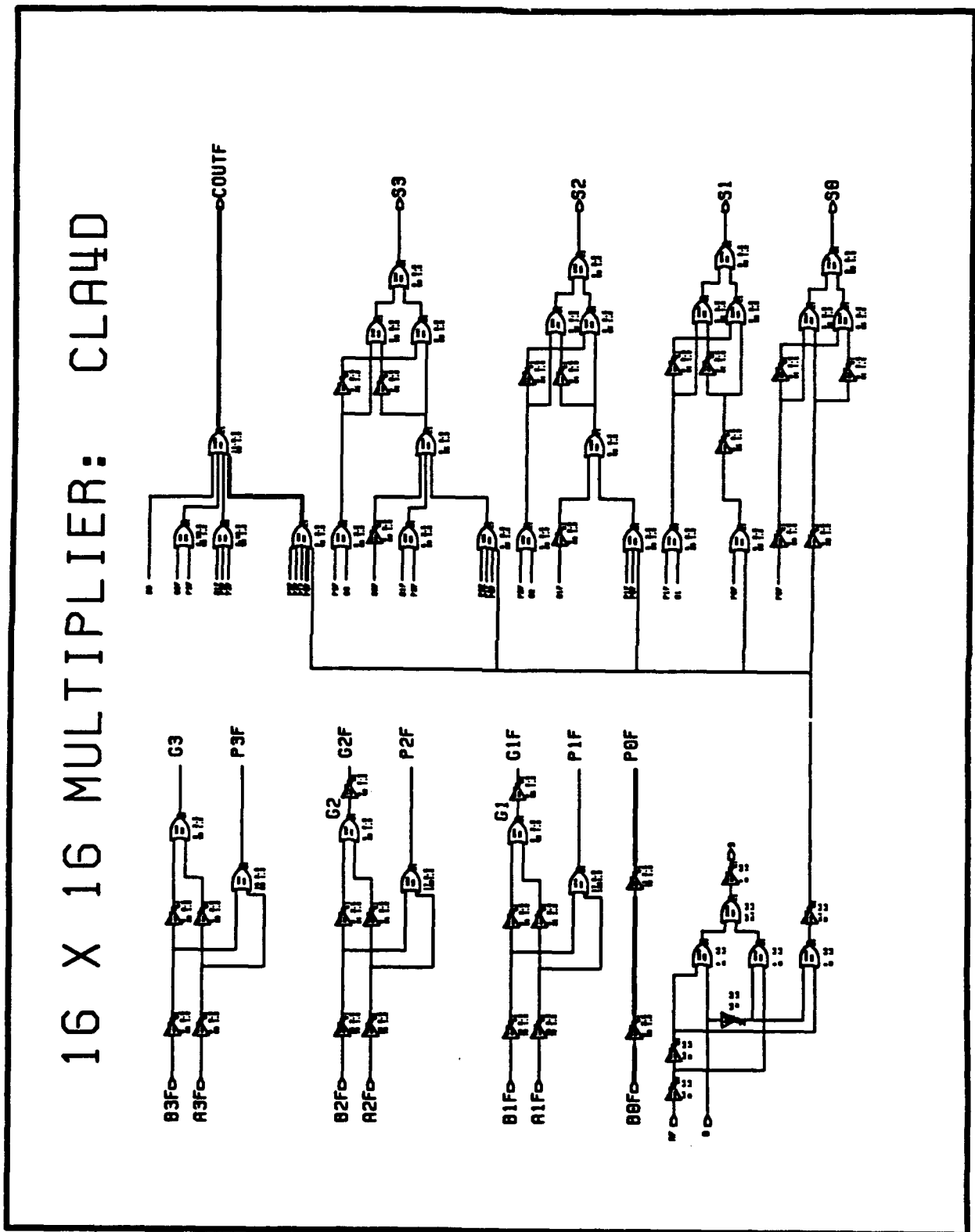


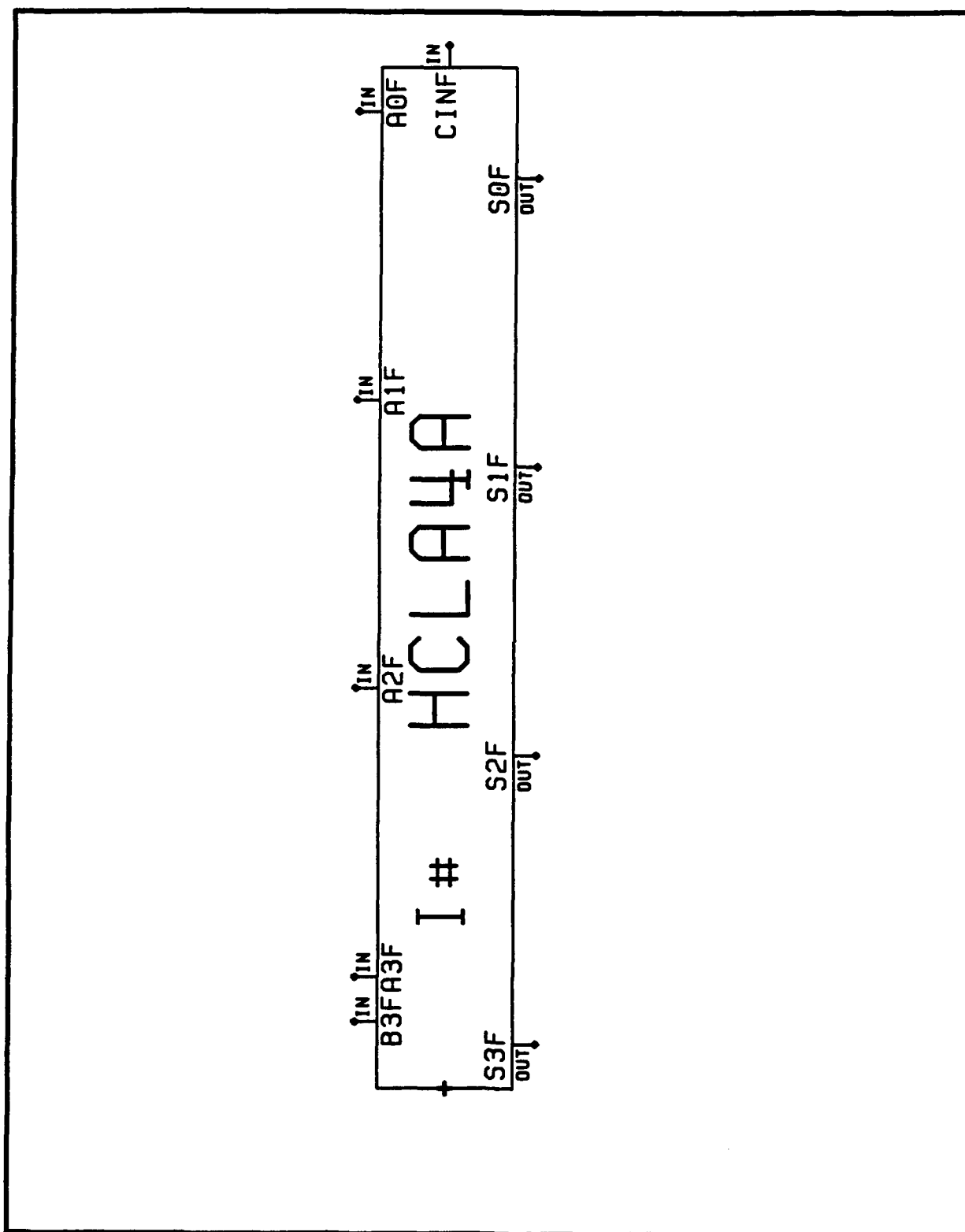


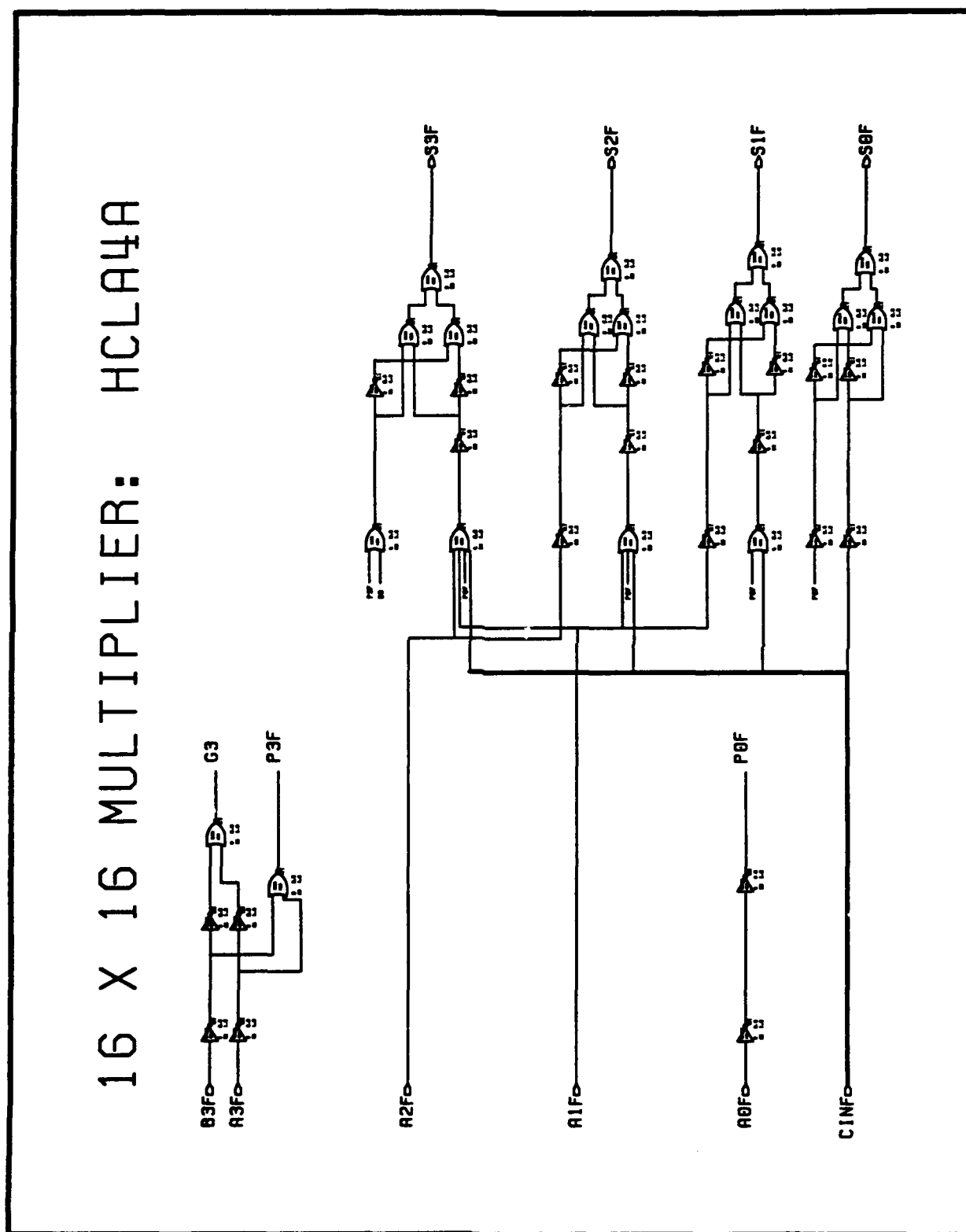


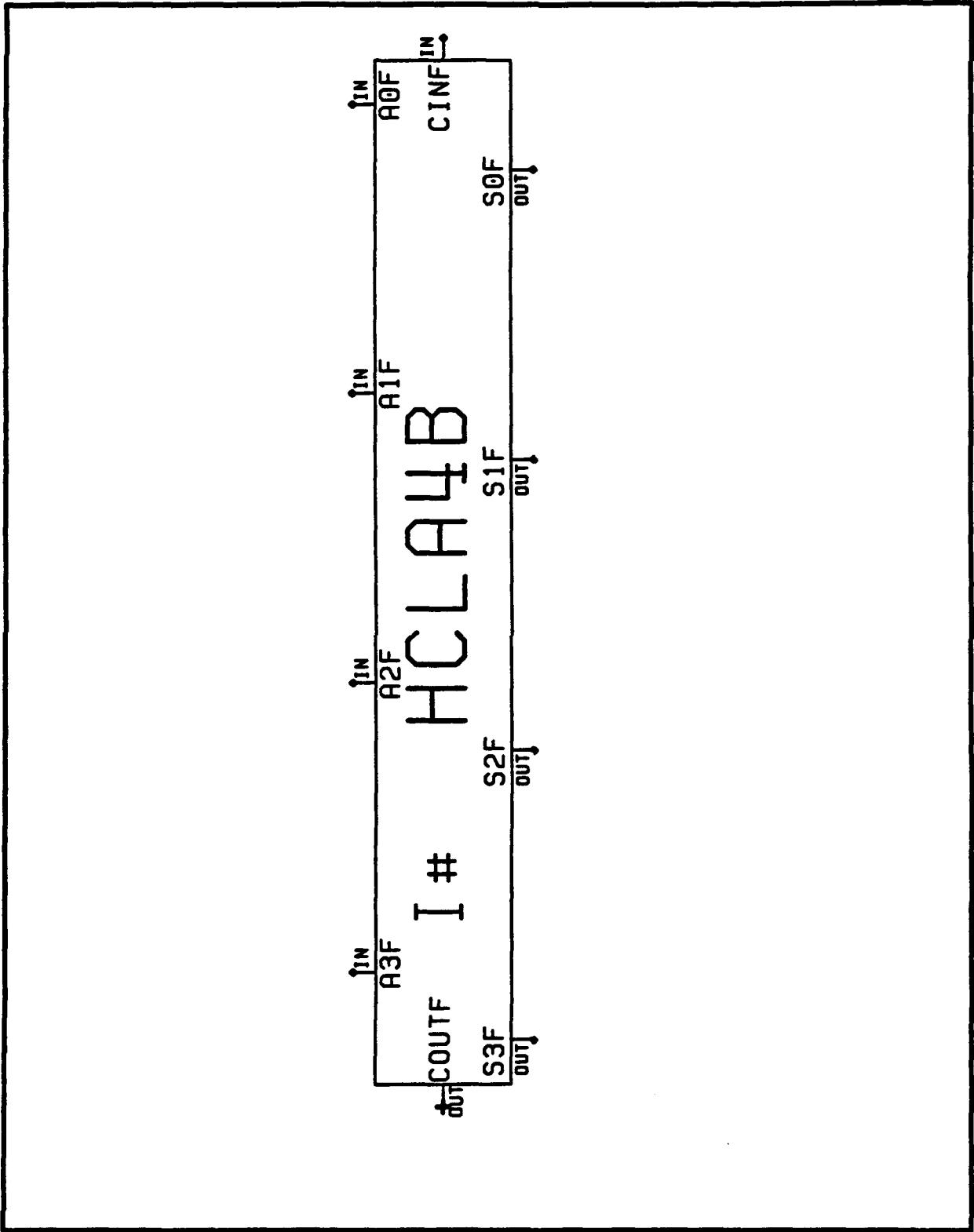


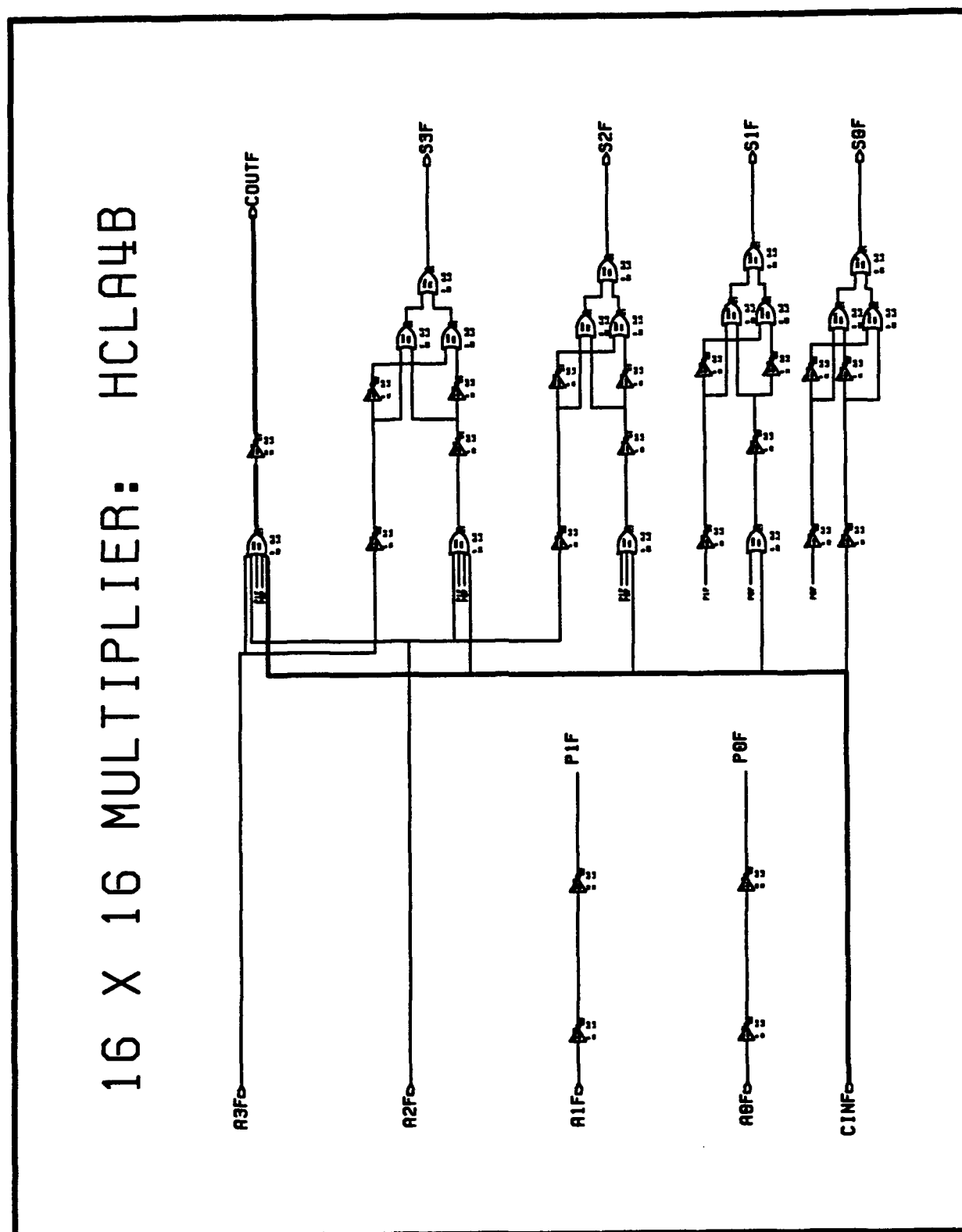


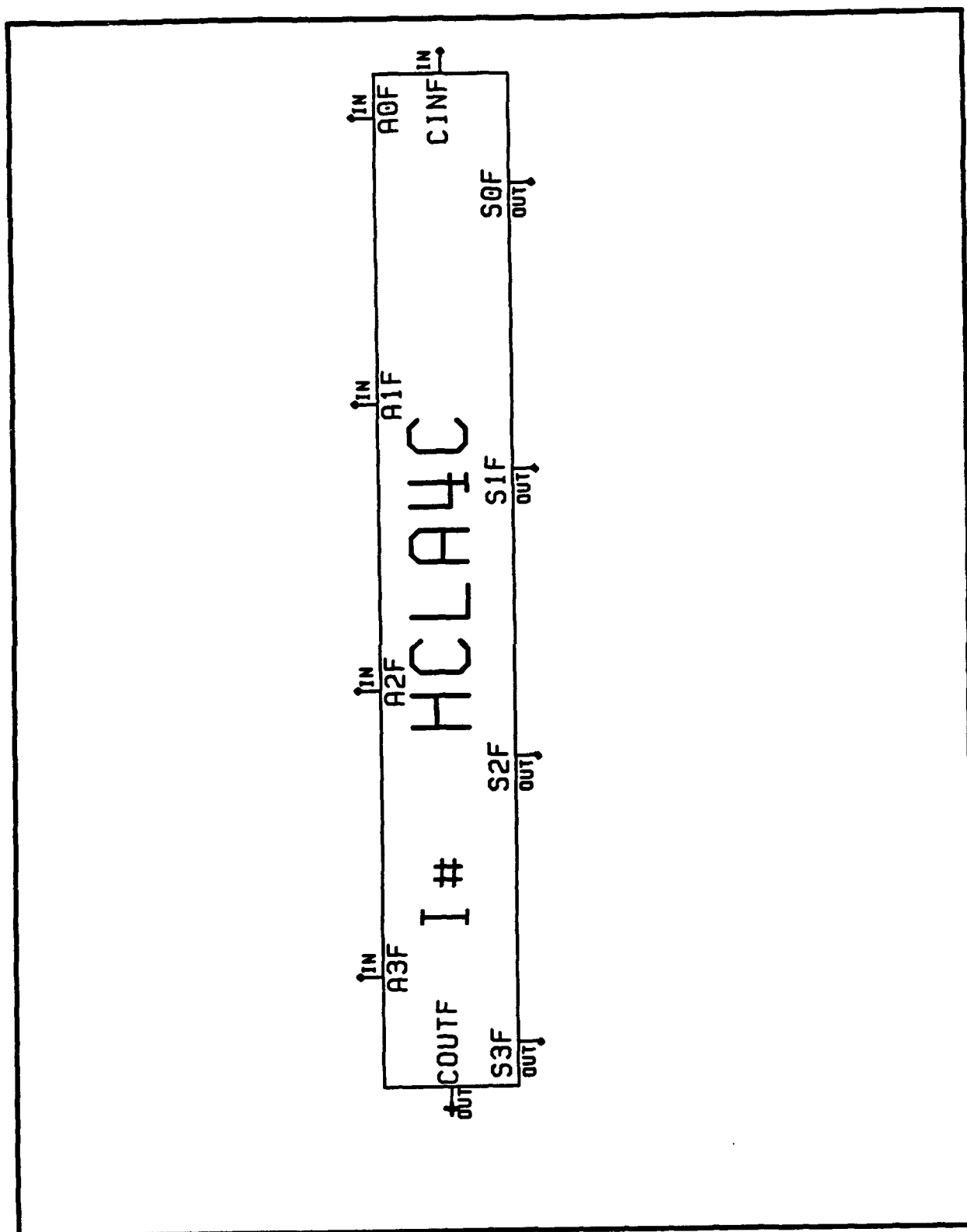


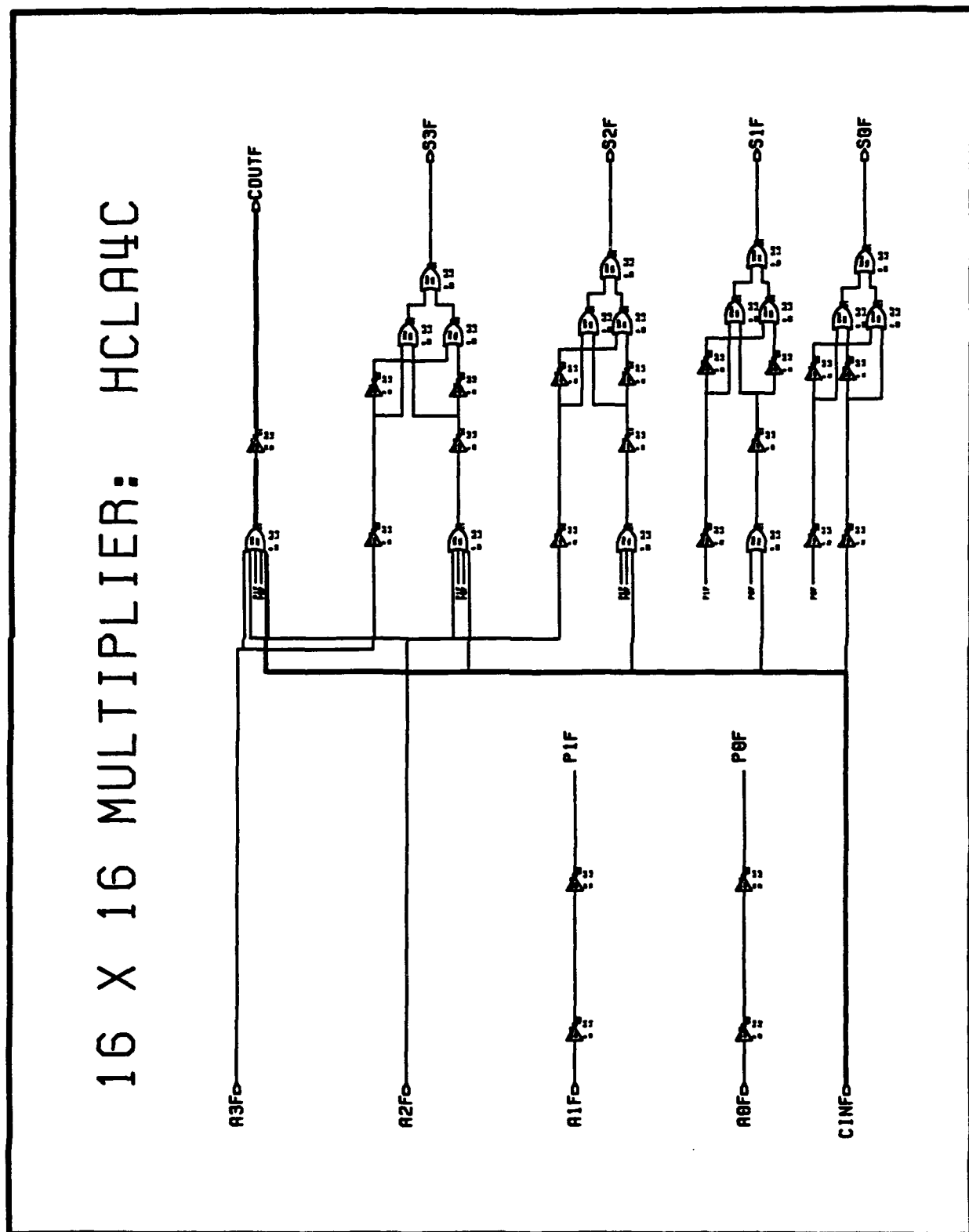




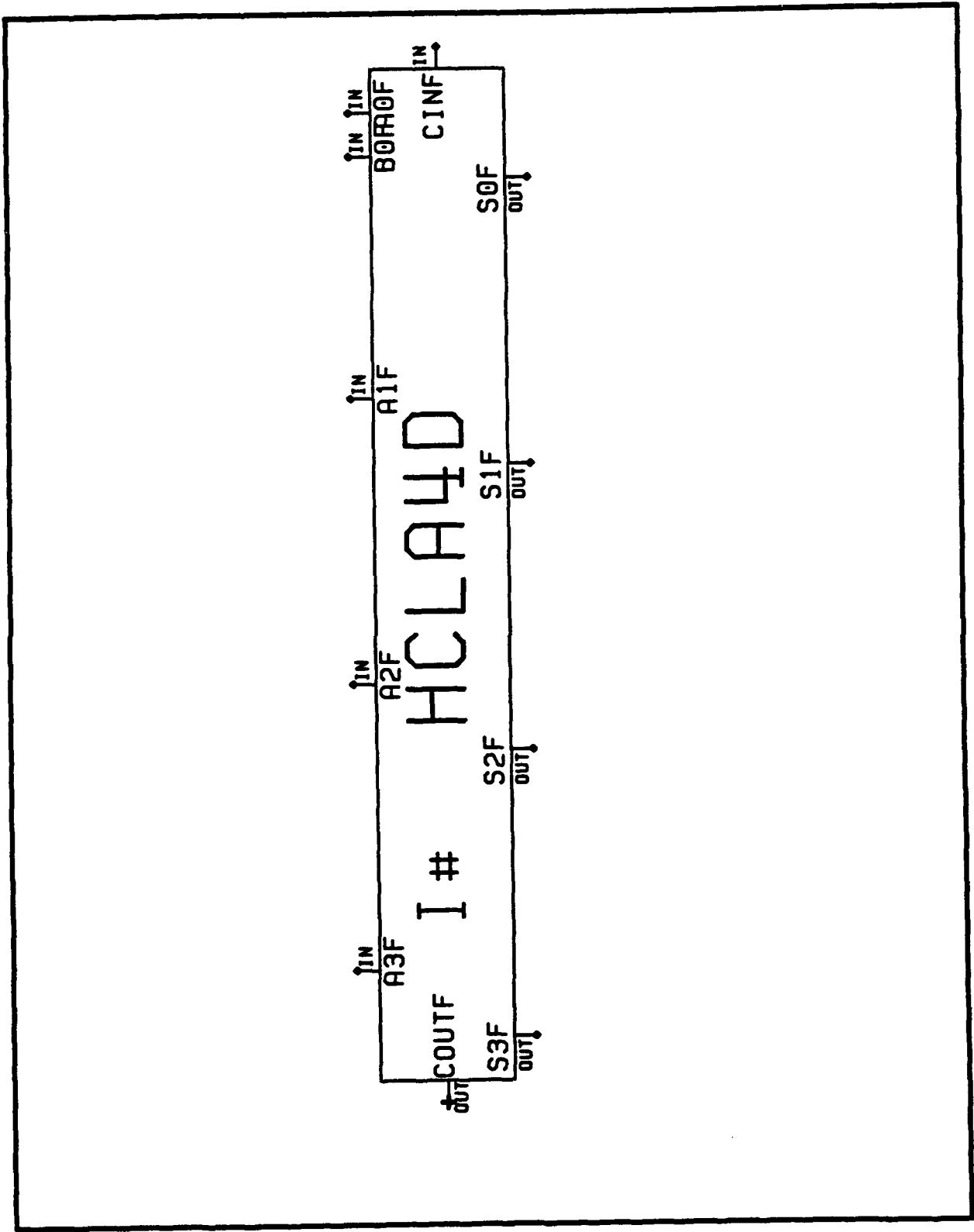




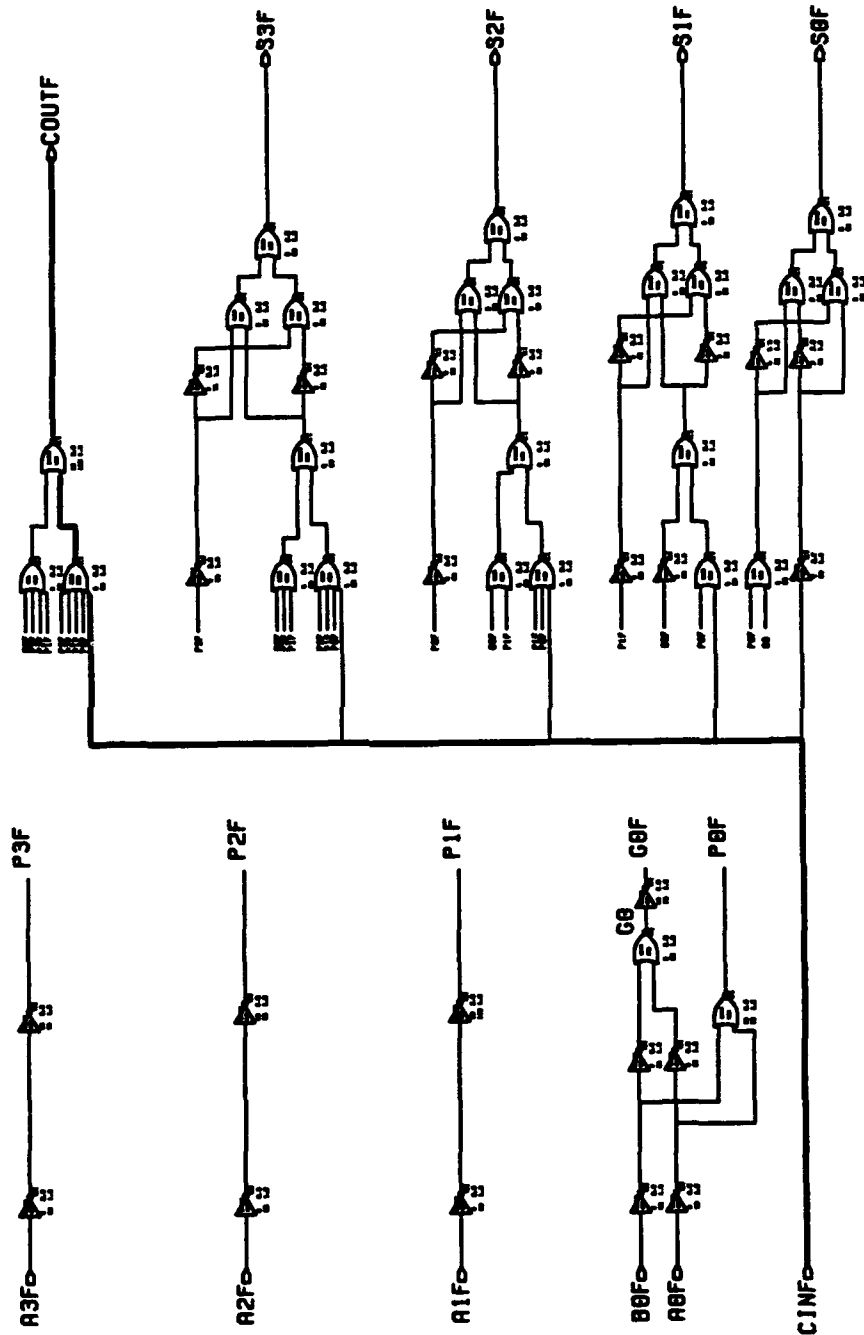


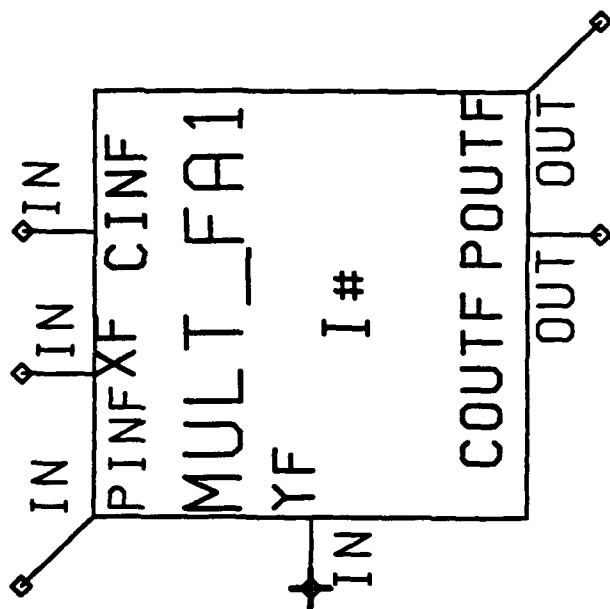


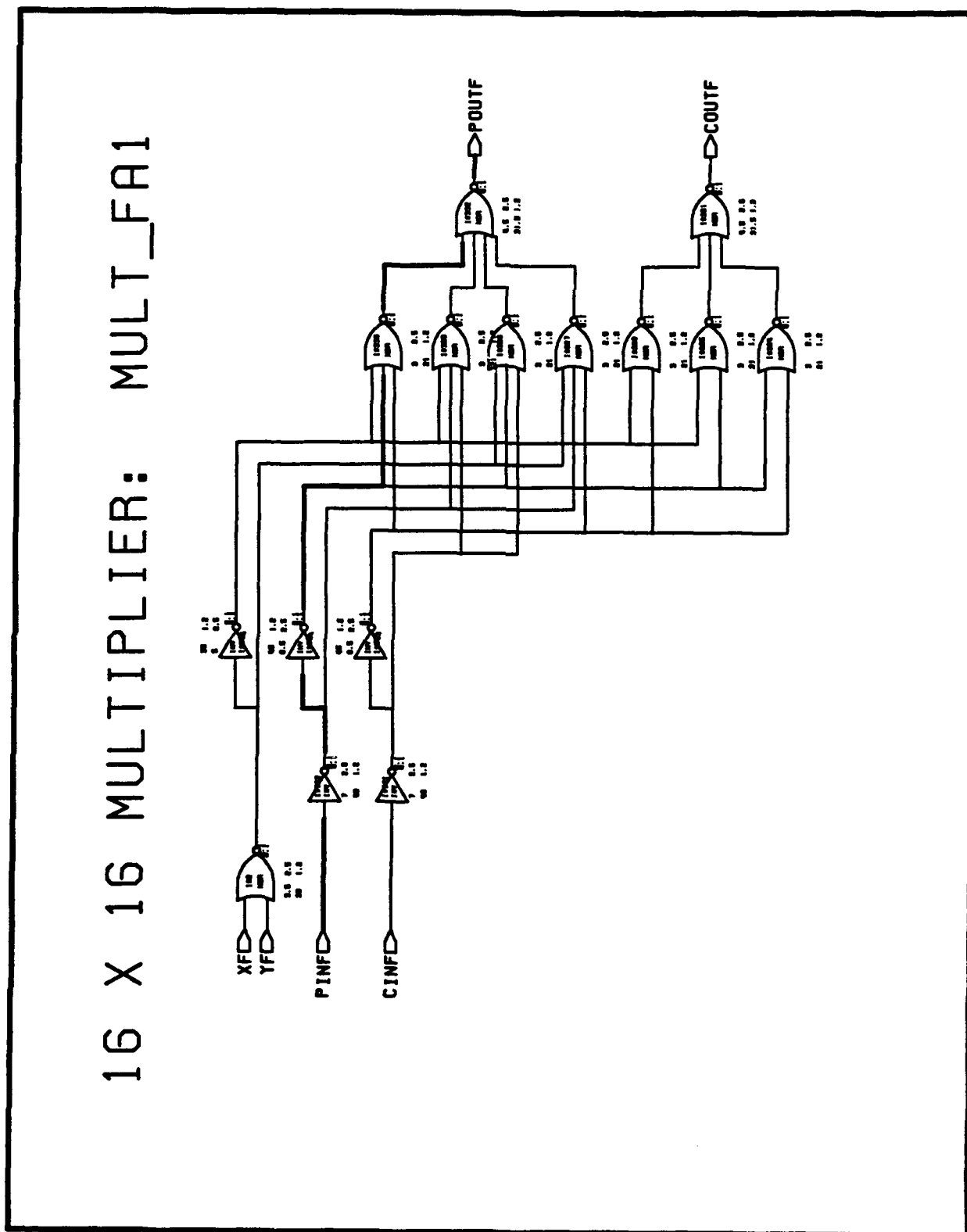


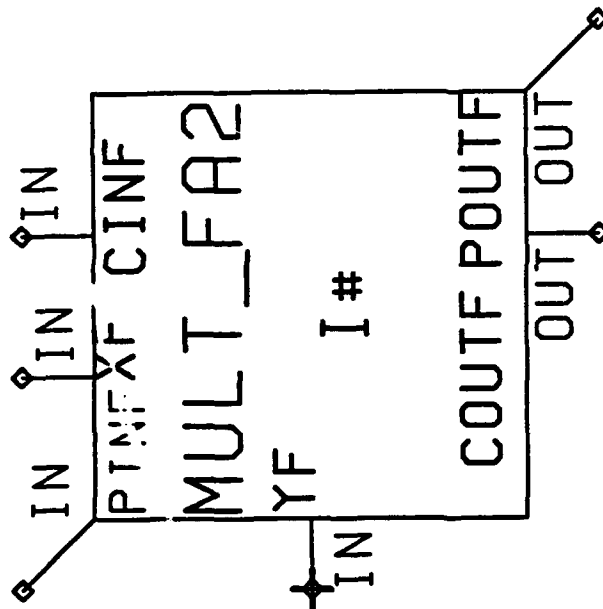


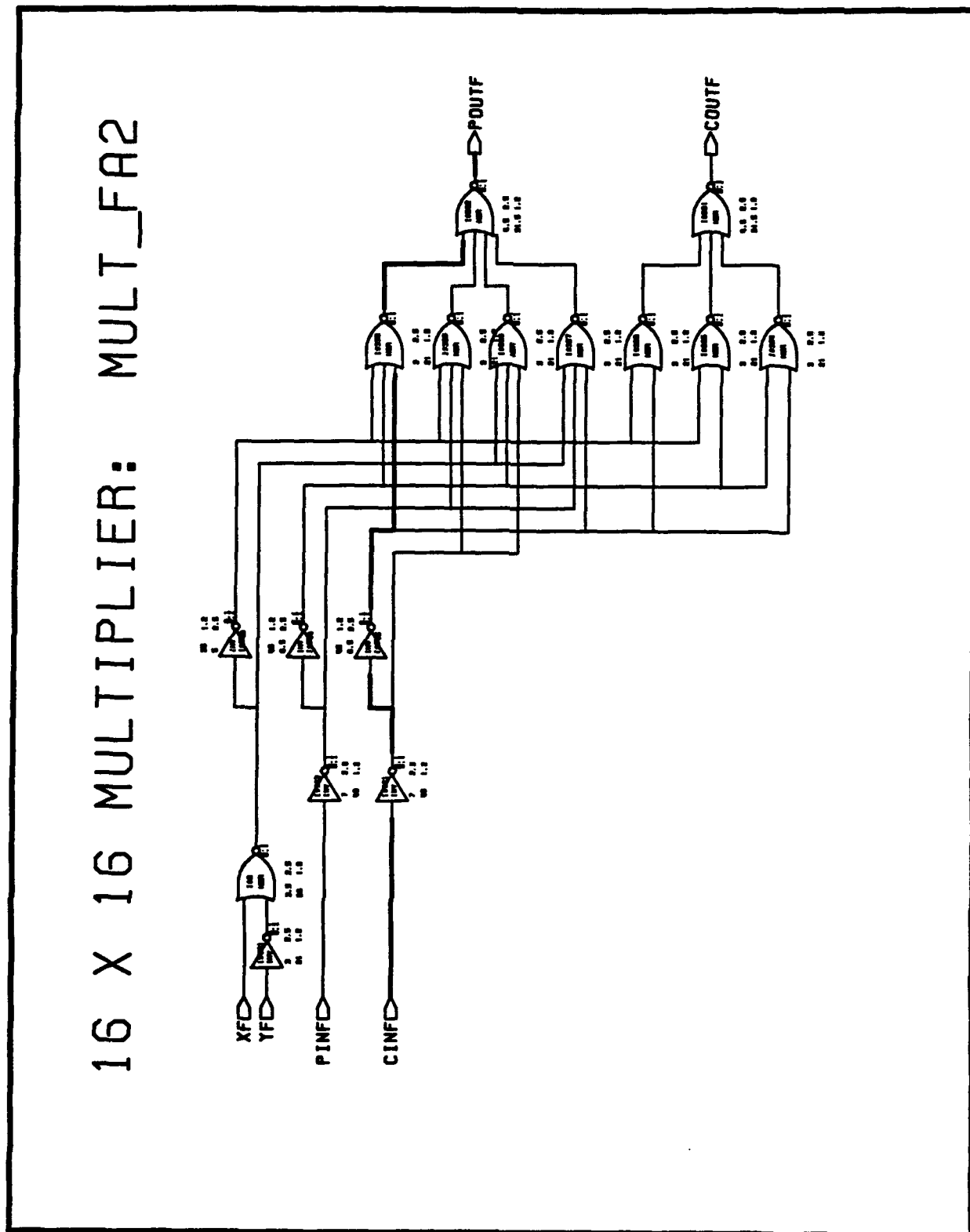
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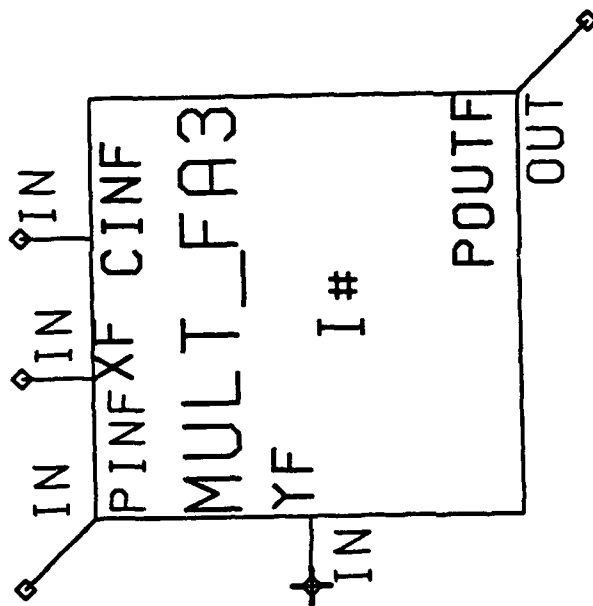




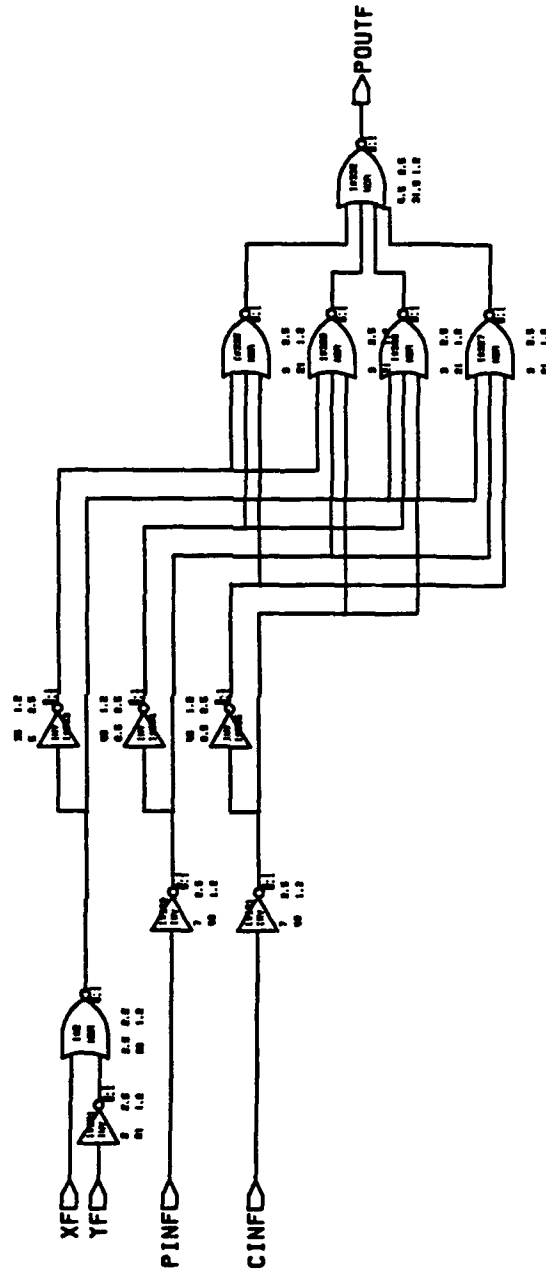




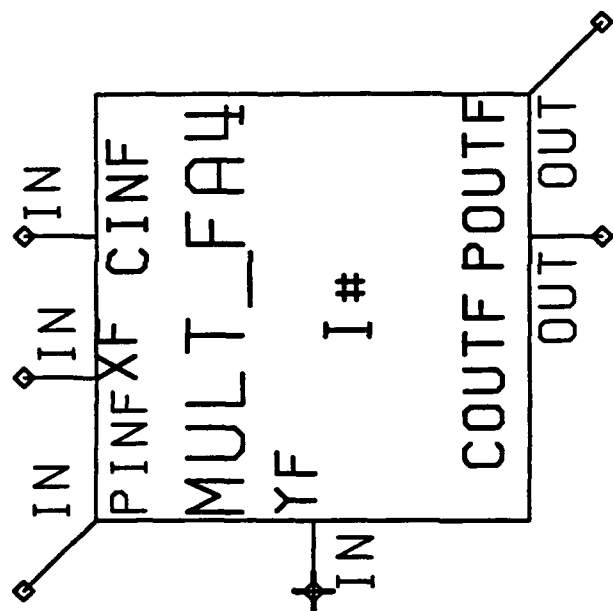


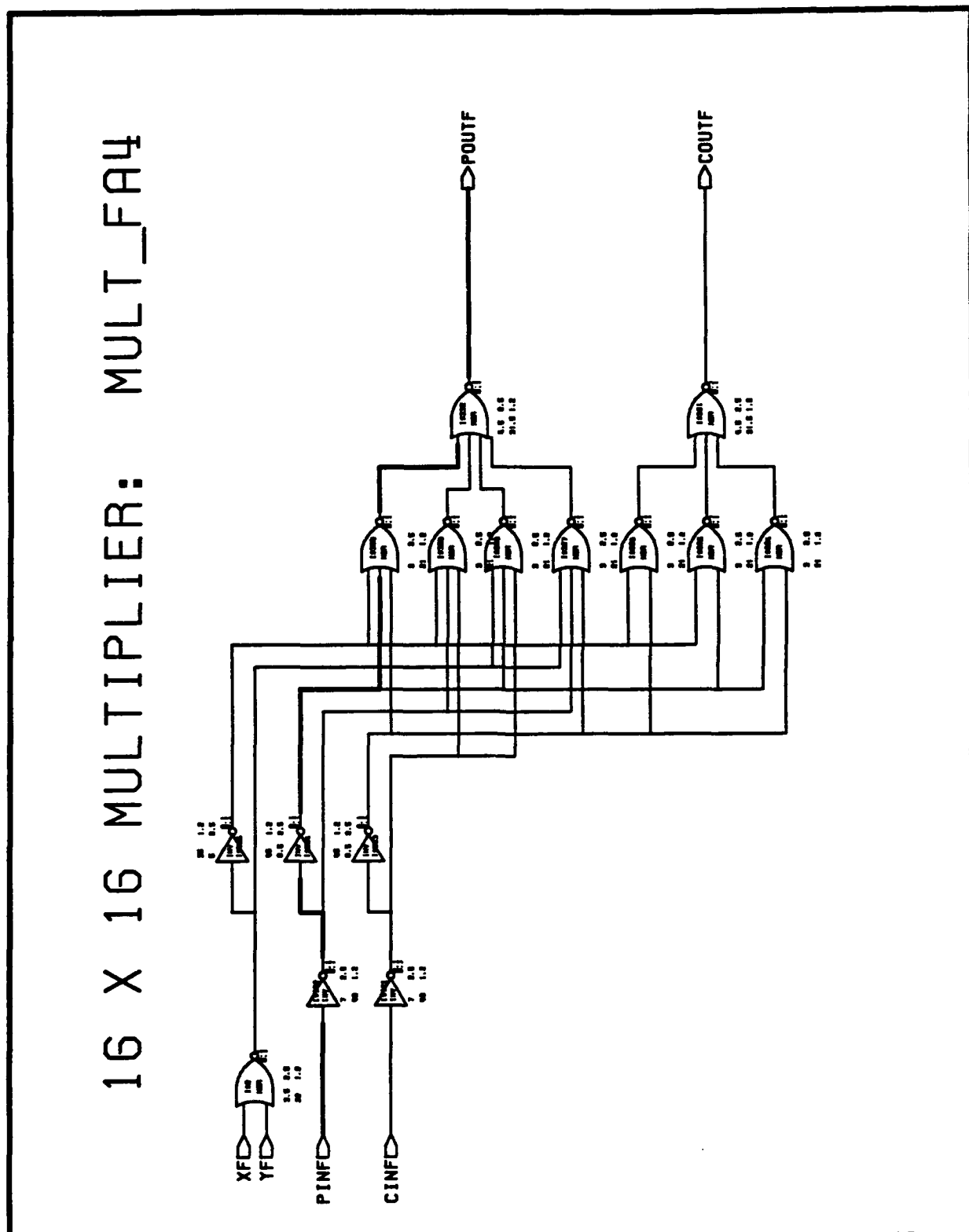


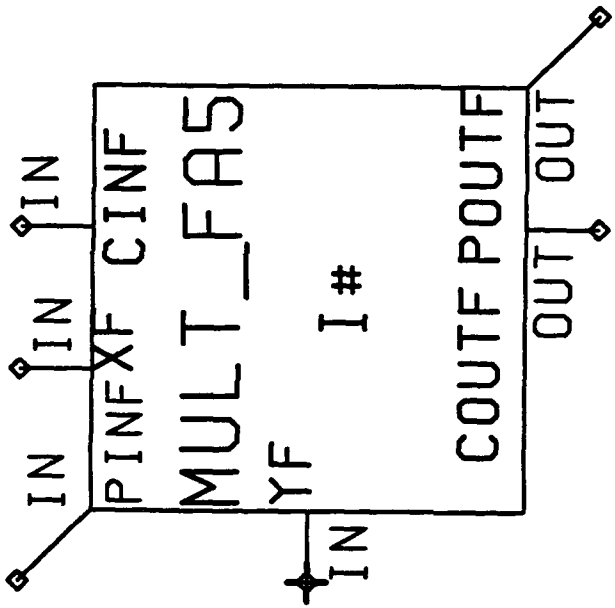
16 X 16 MULTIPLIER: MULT\_FA3

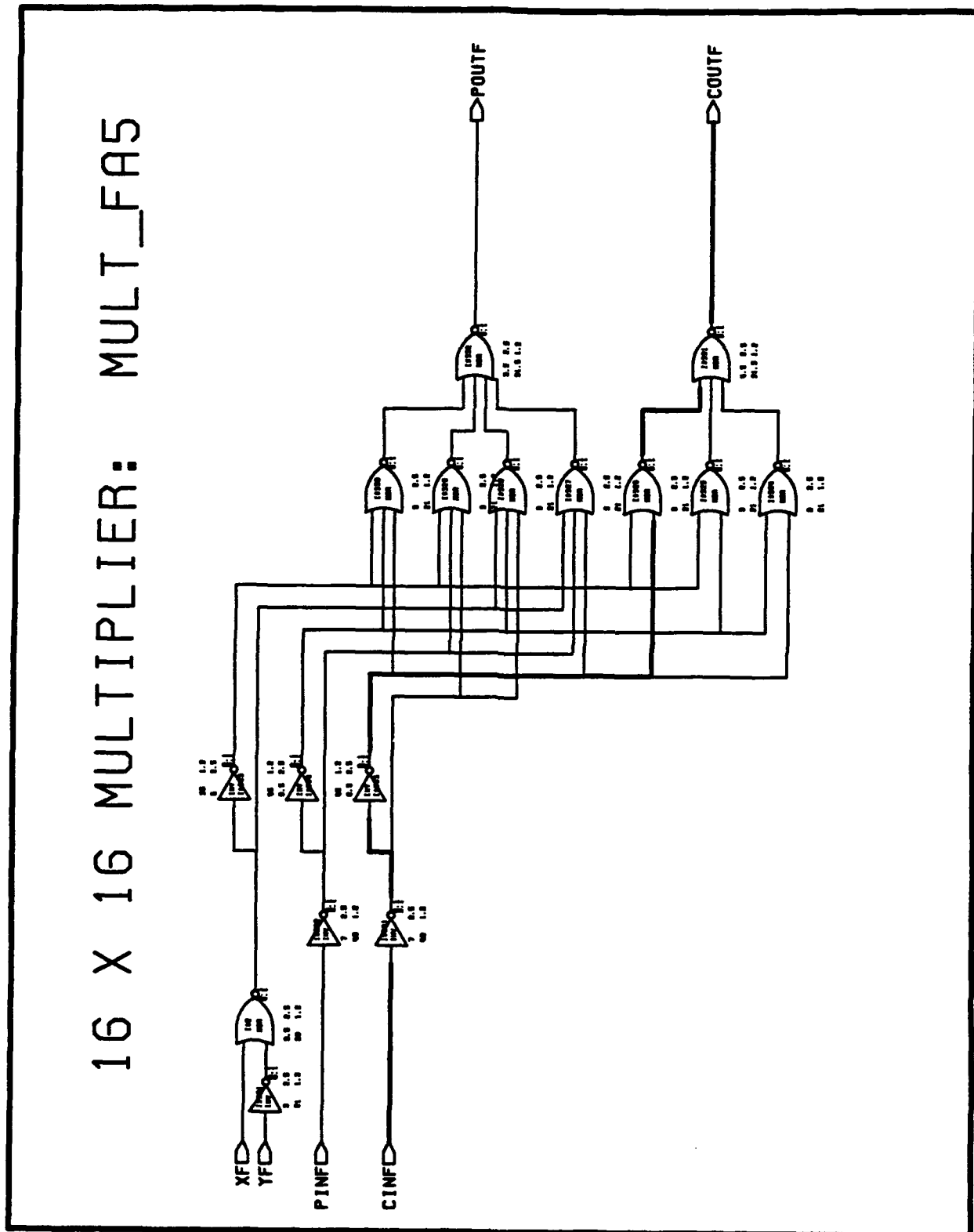


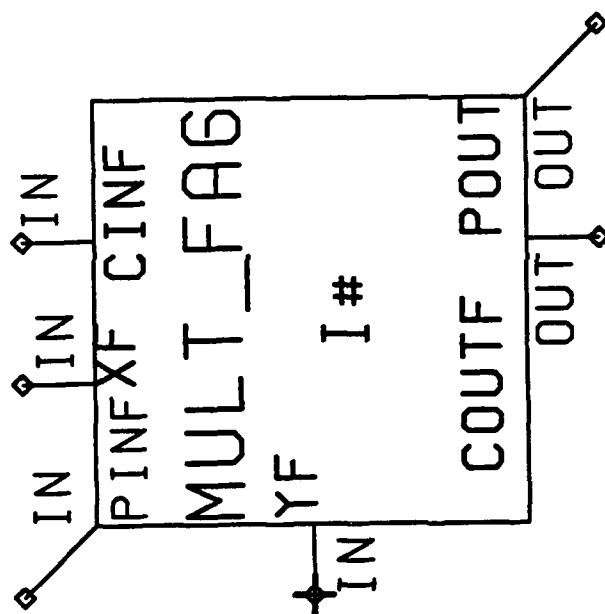


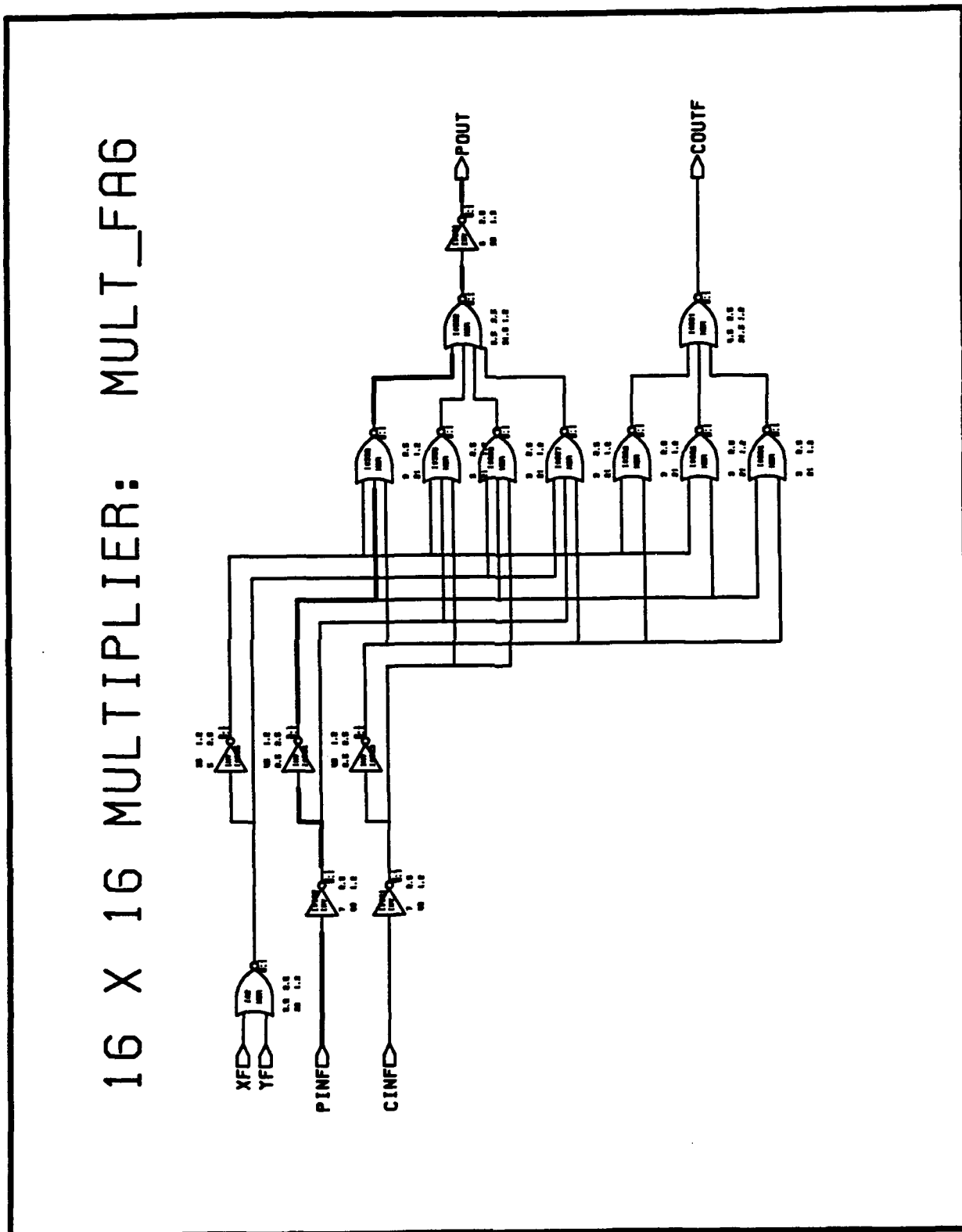


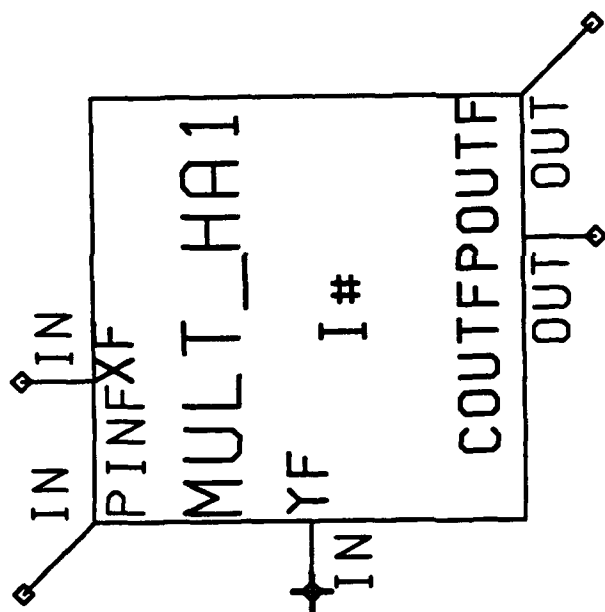


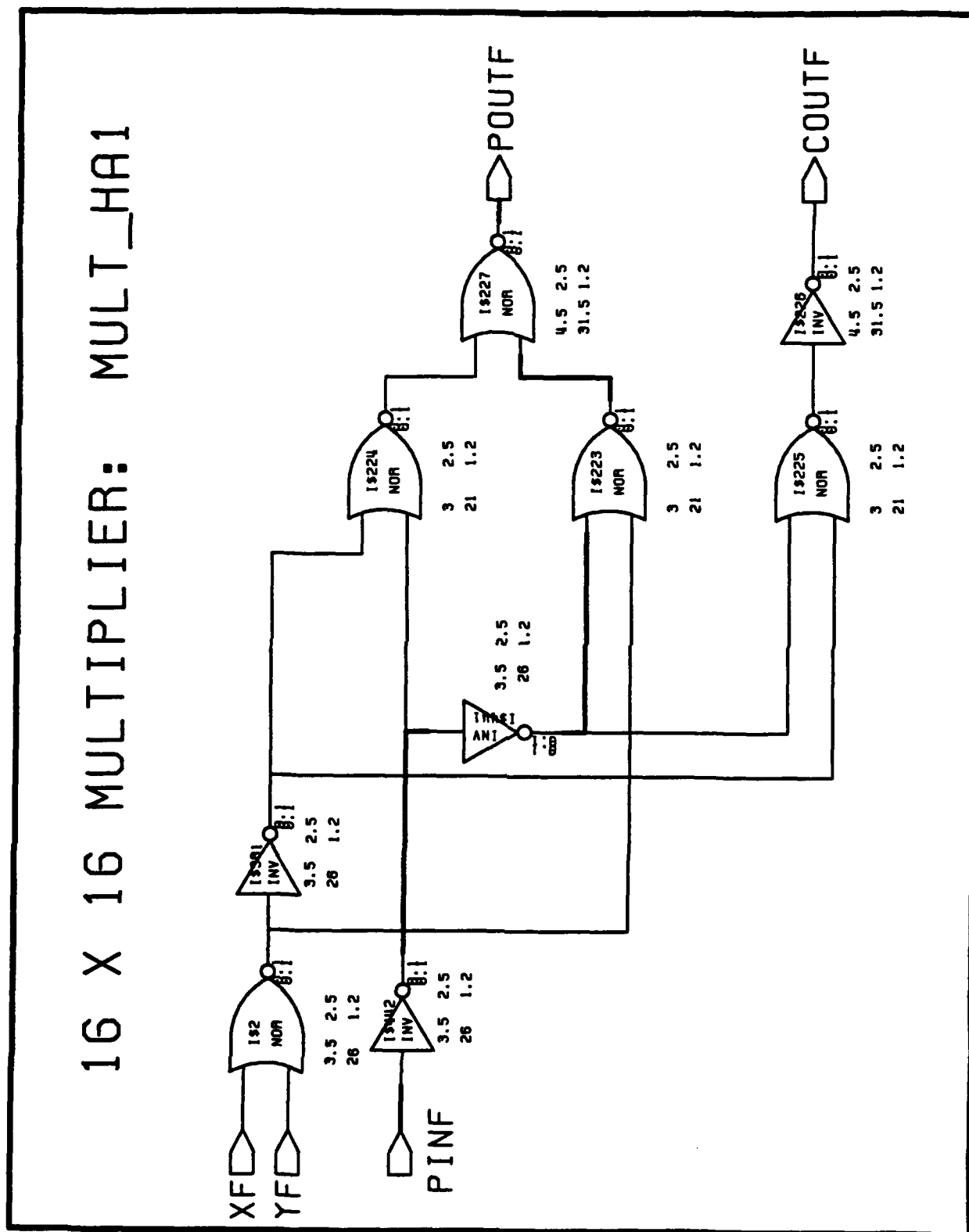




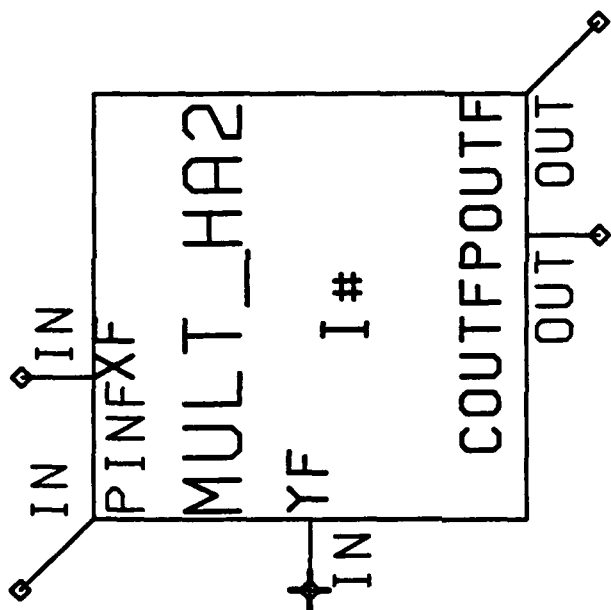


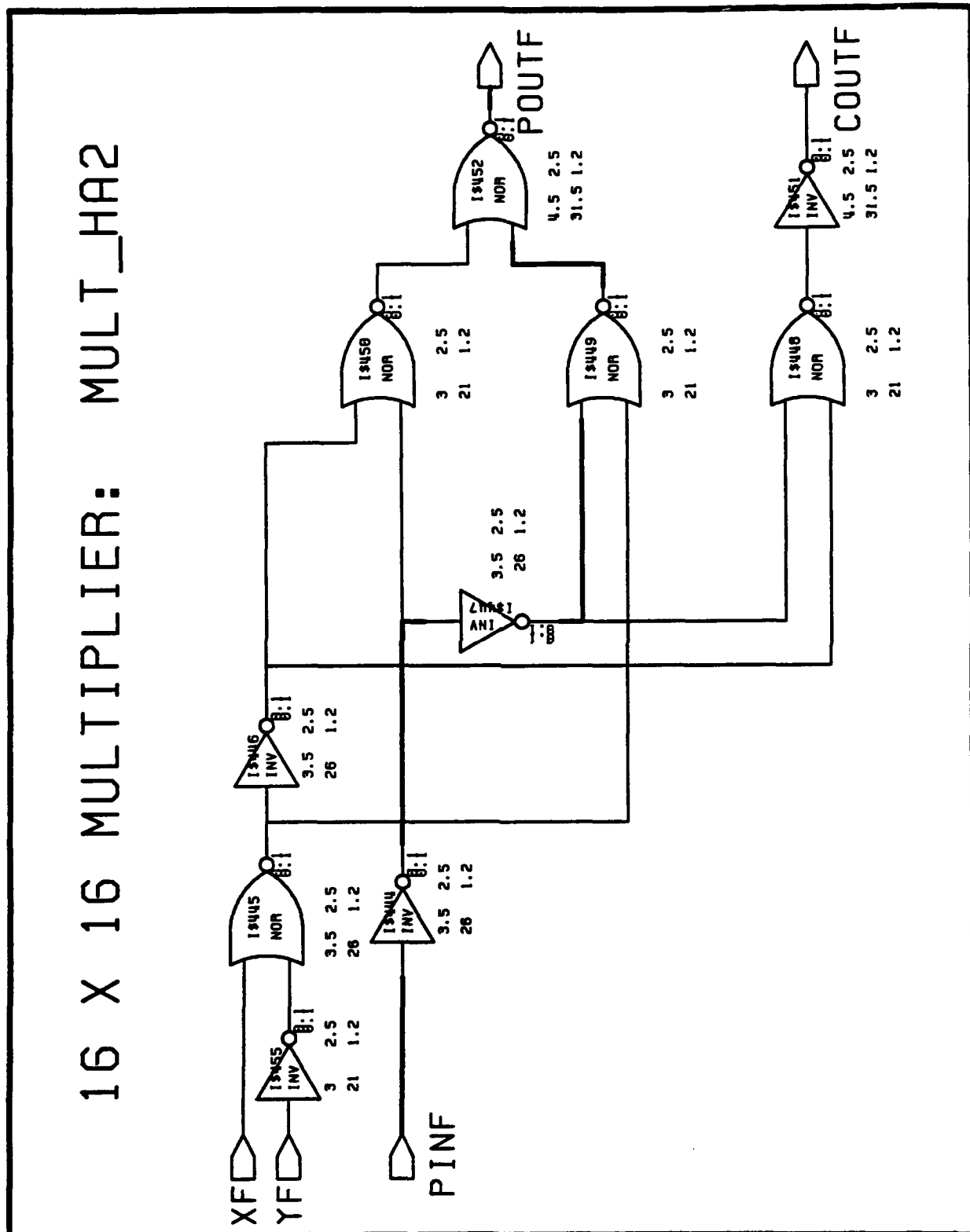


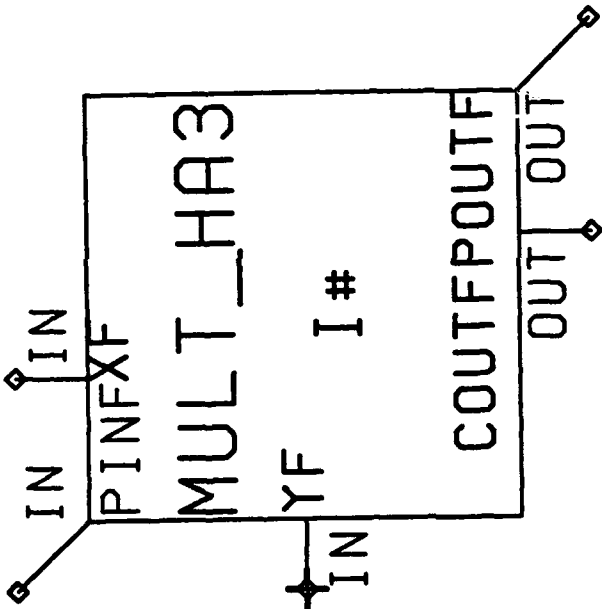


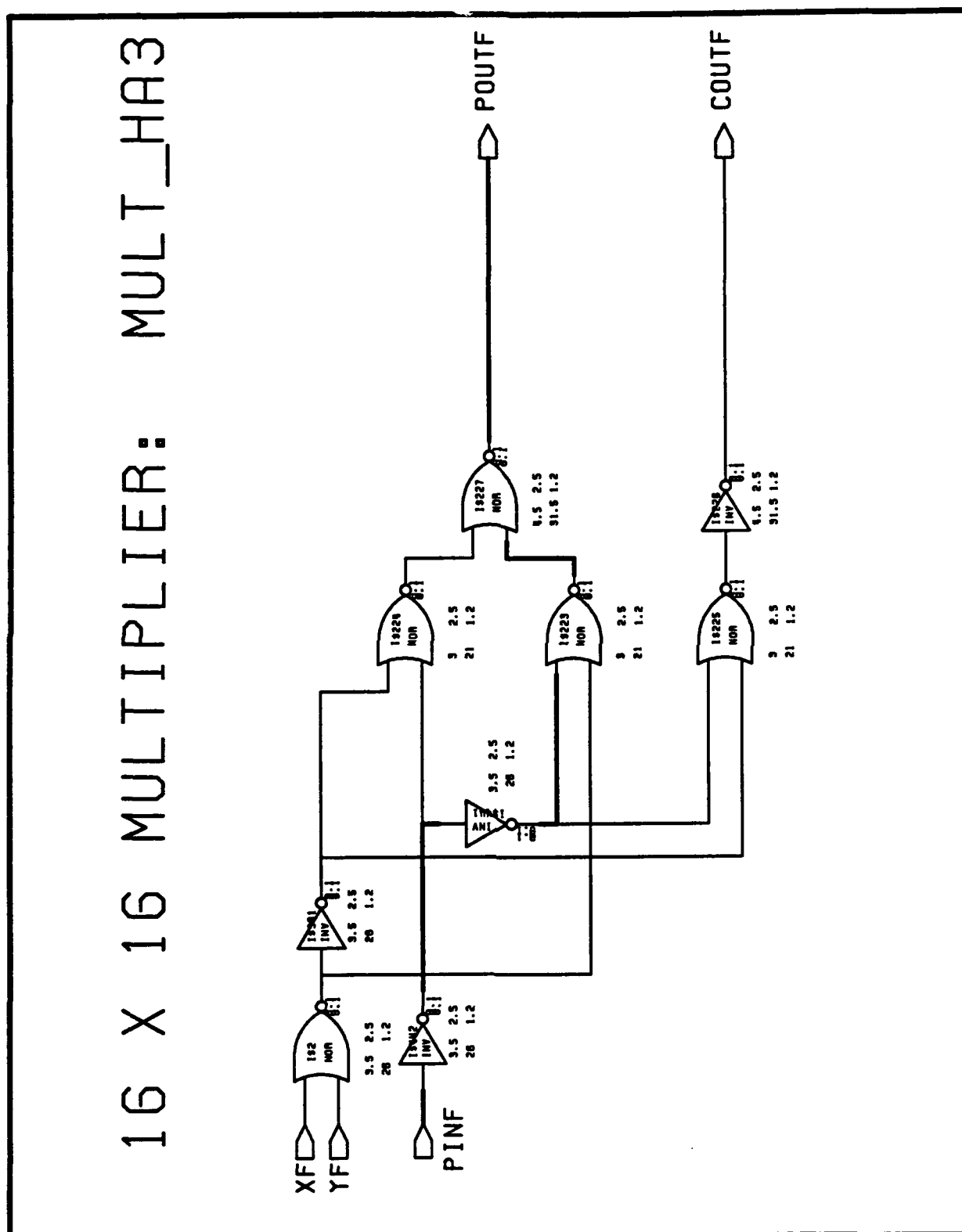


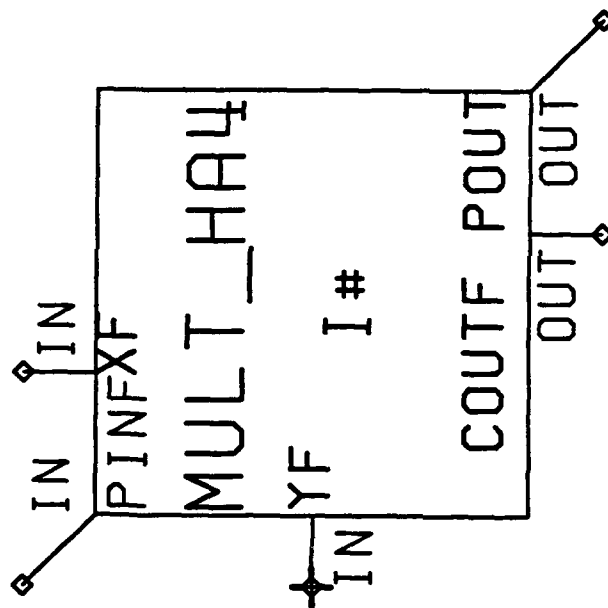


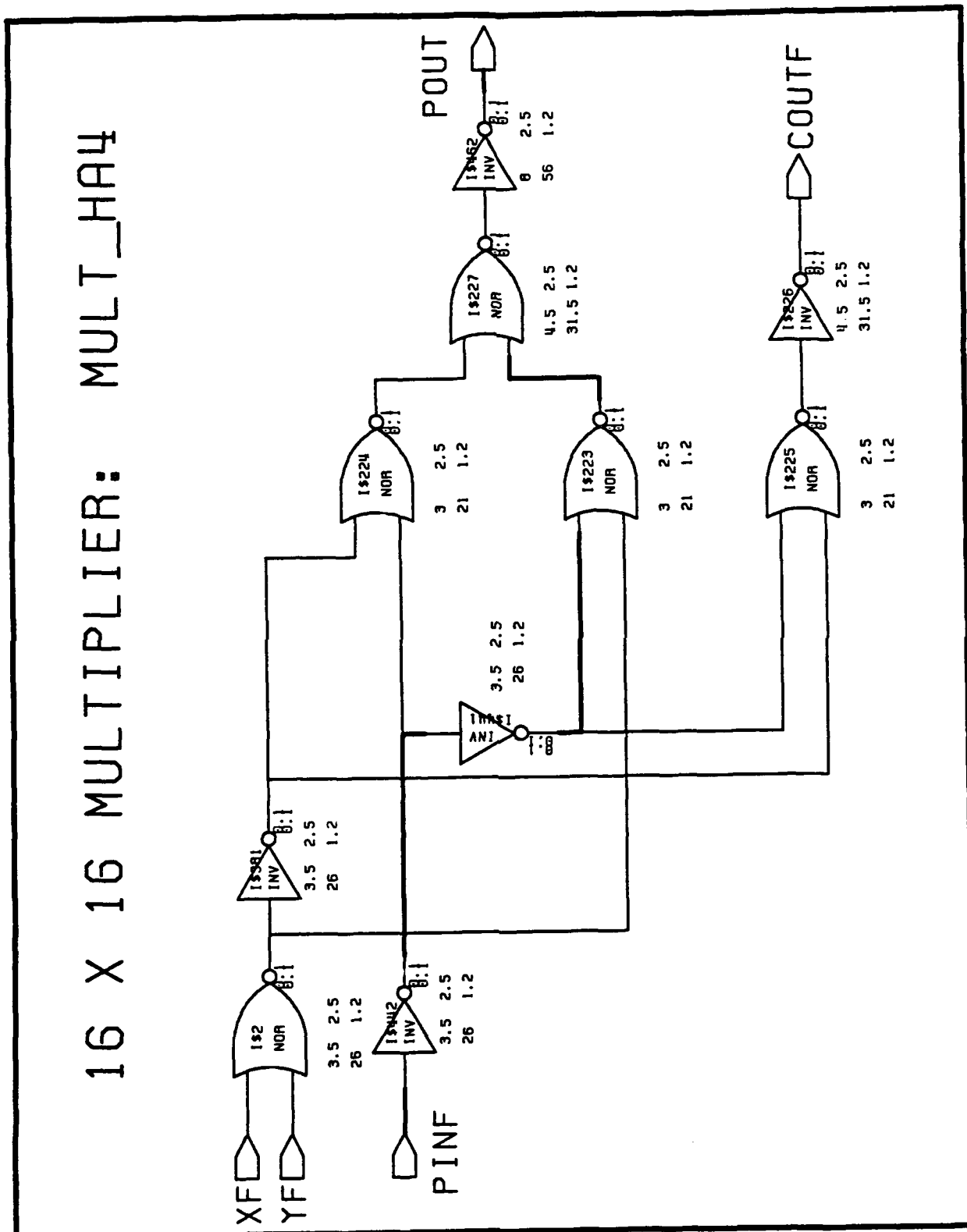


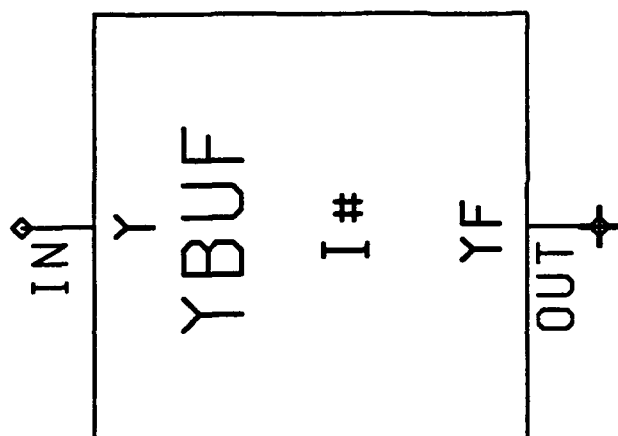




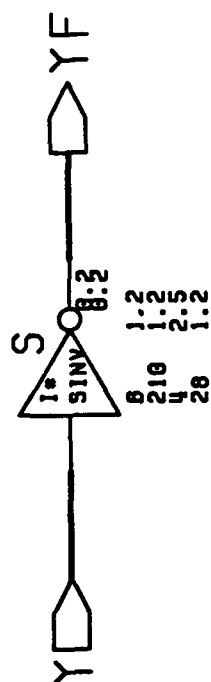




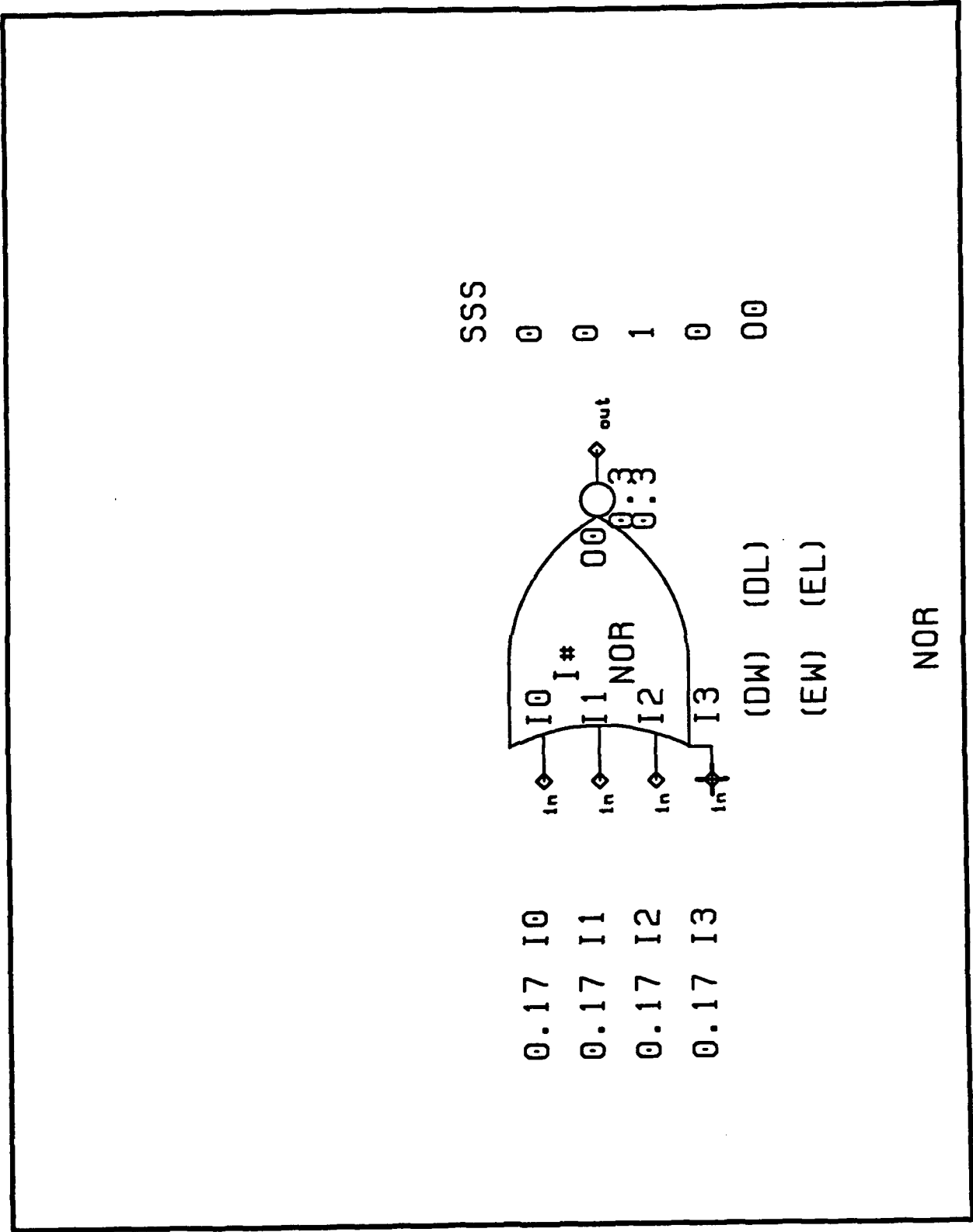


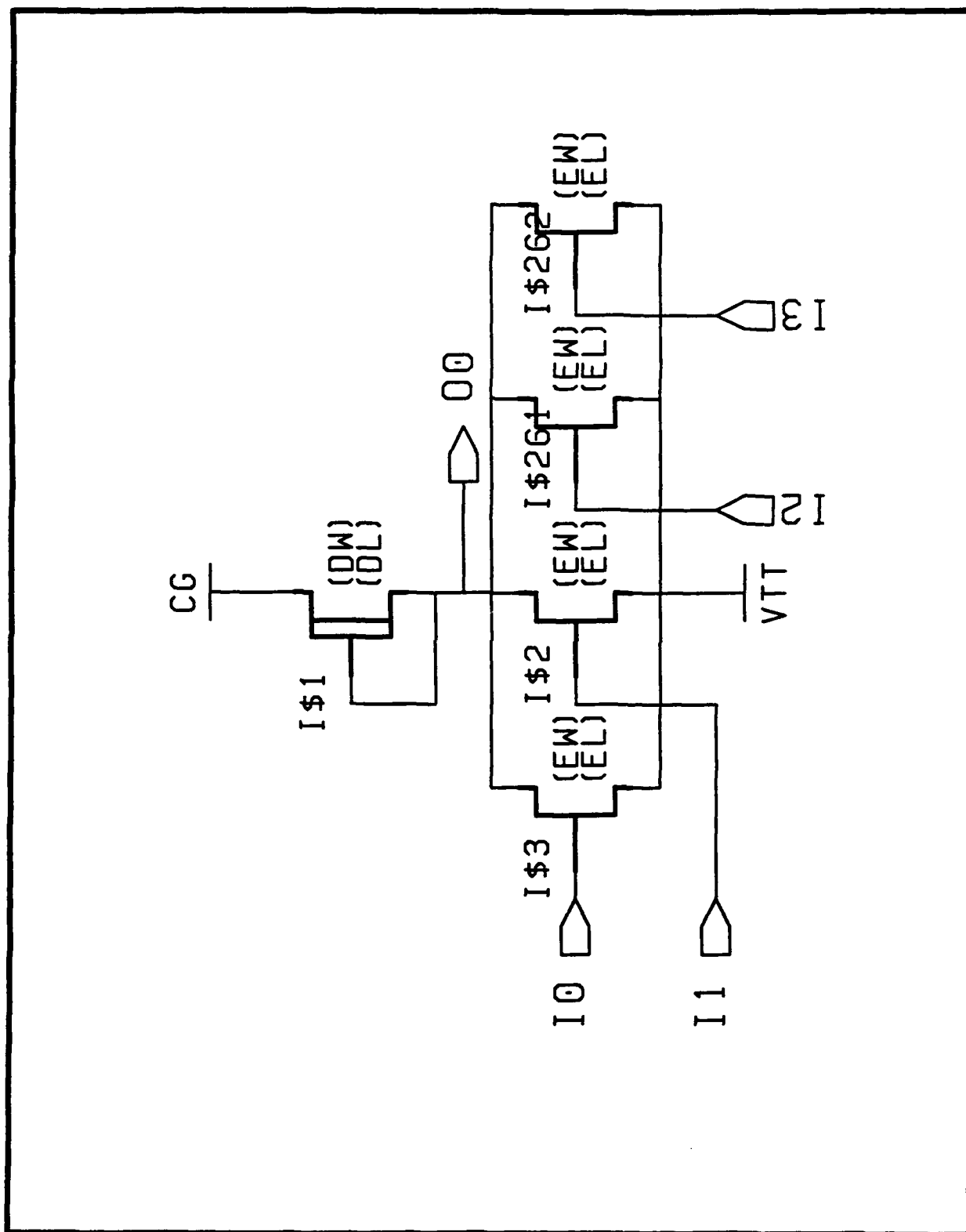


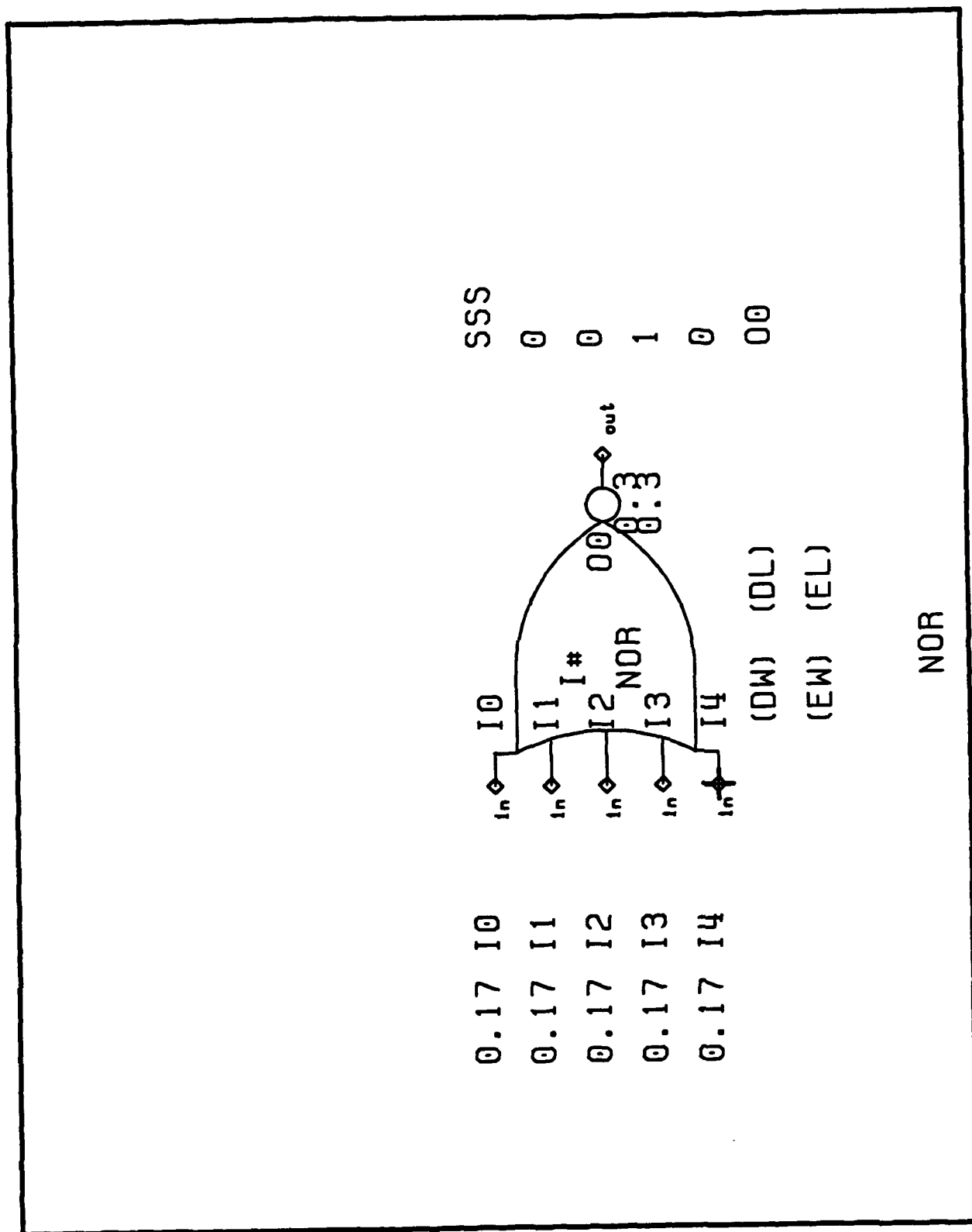
# 16 X 16 MULTIPLIER: YBUF

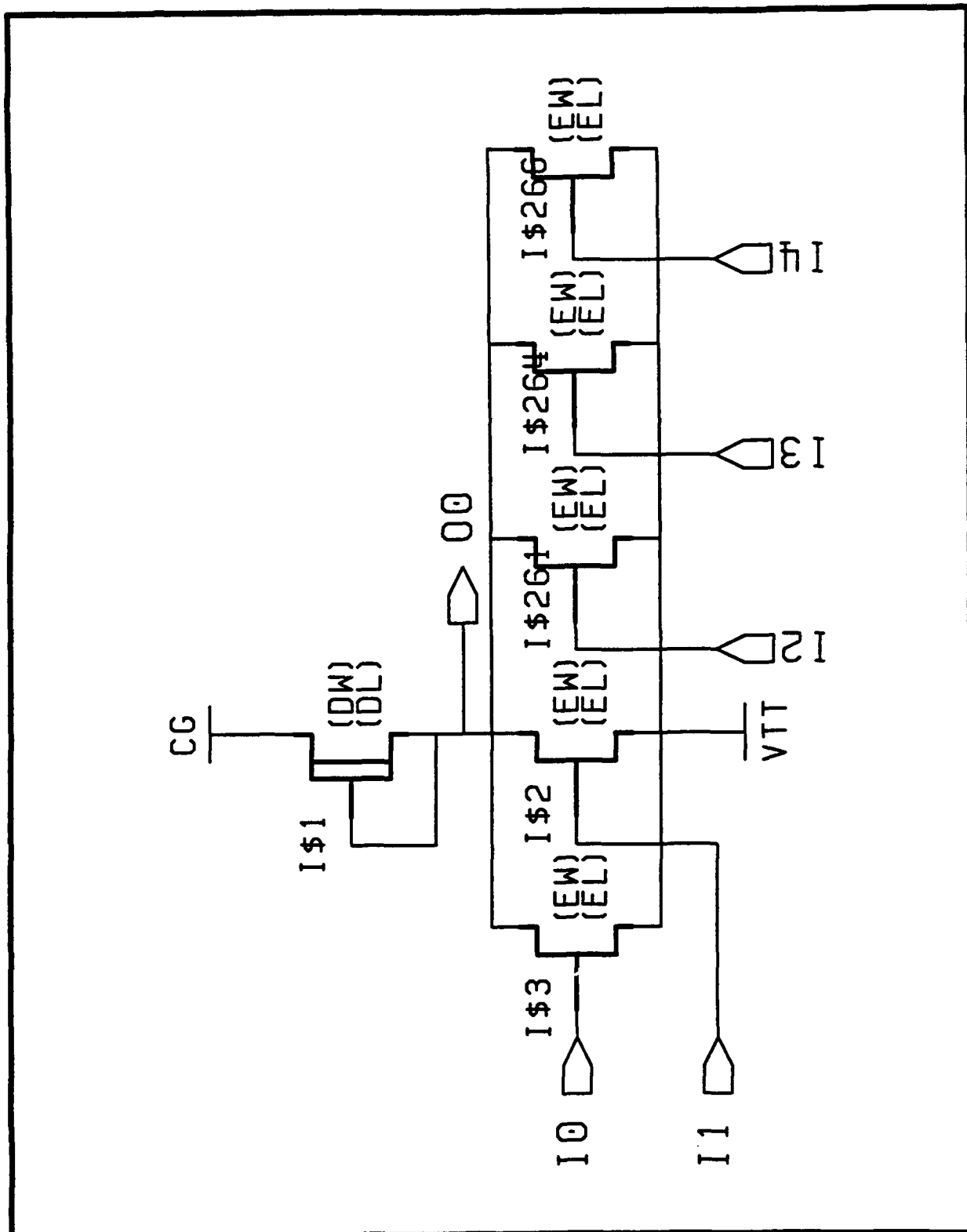


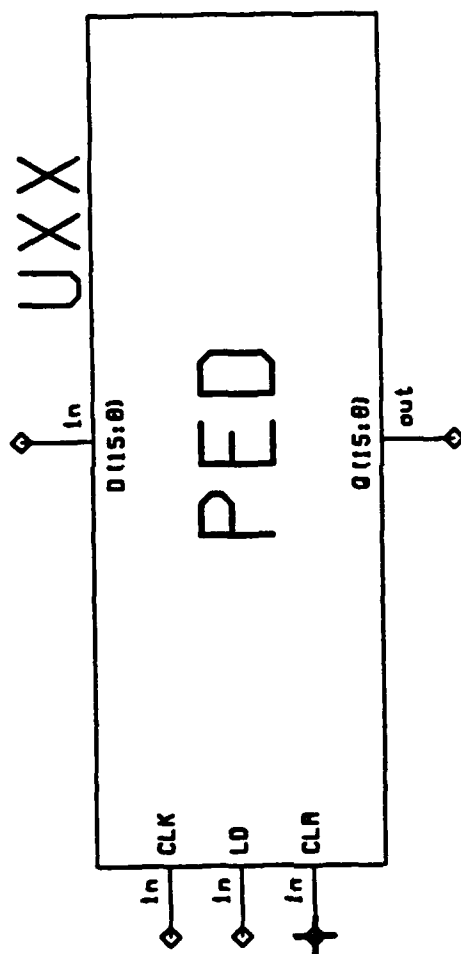


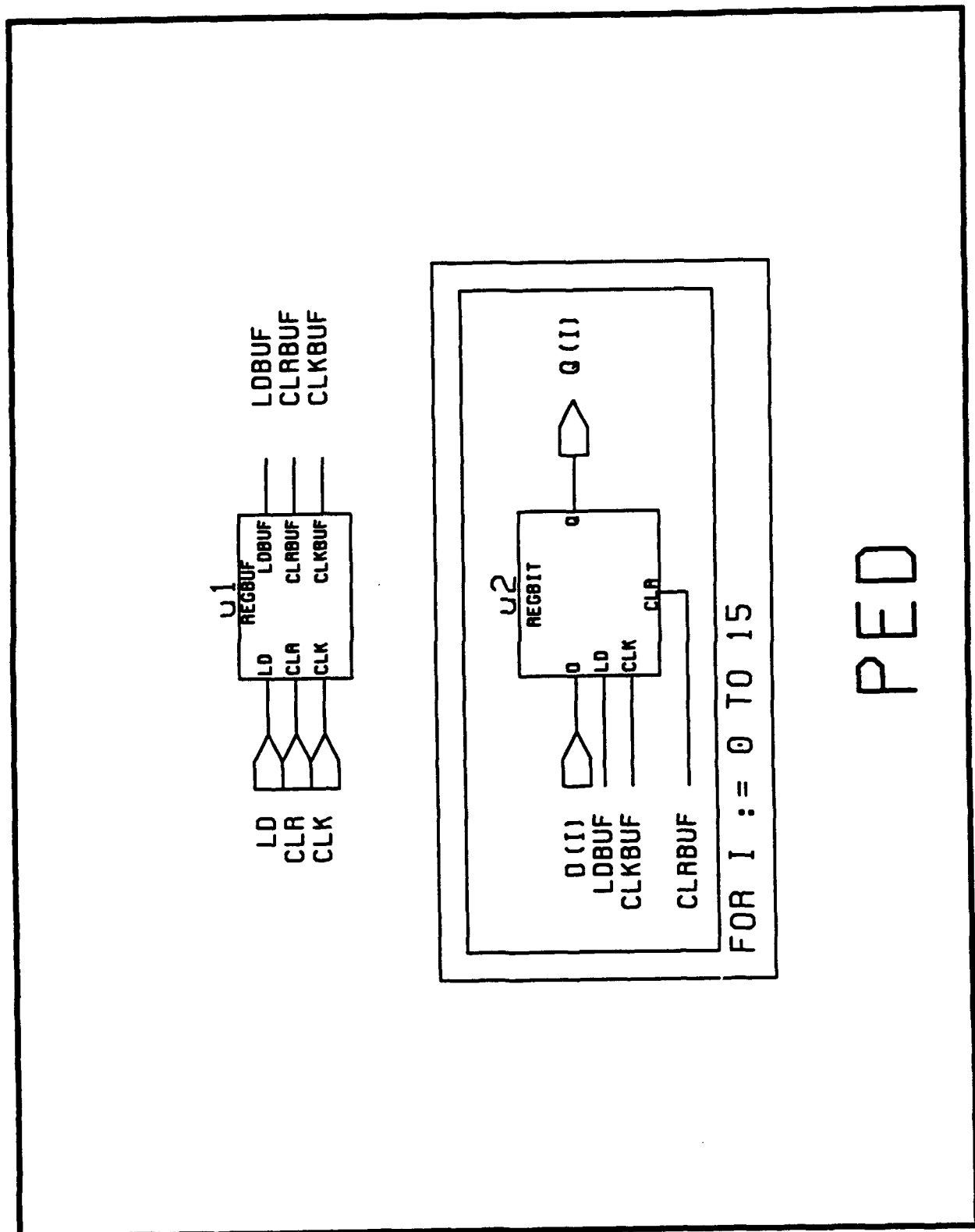




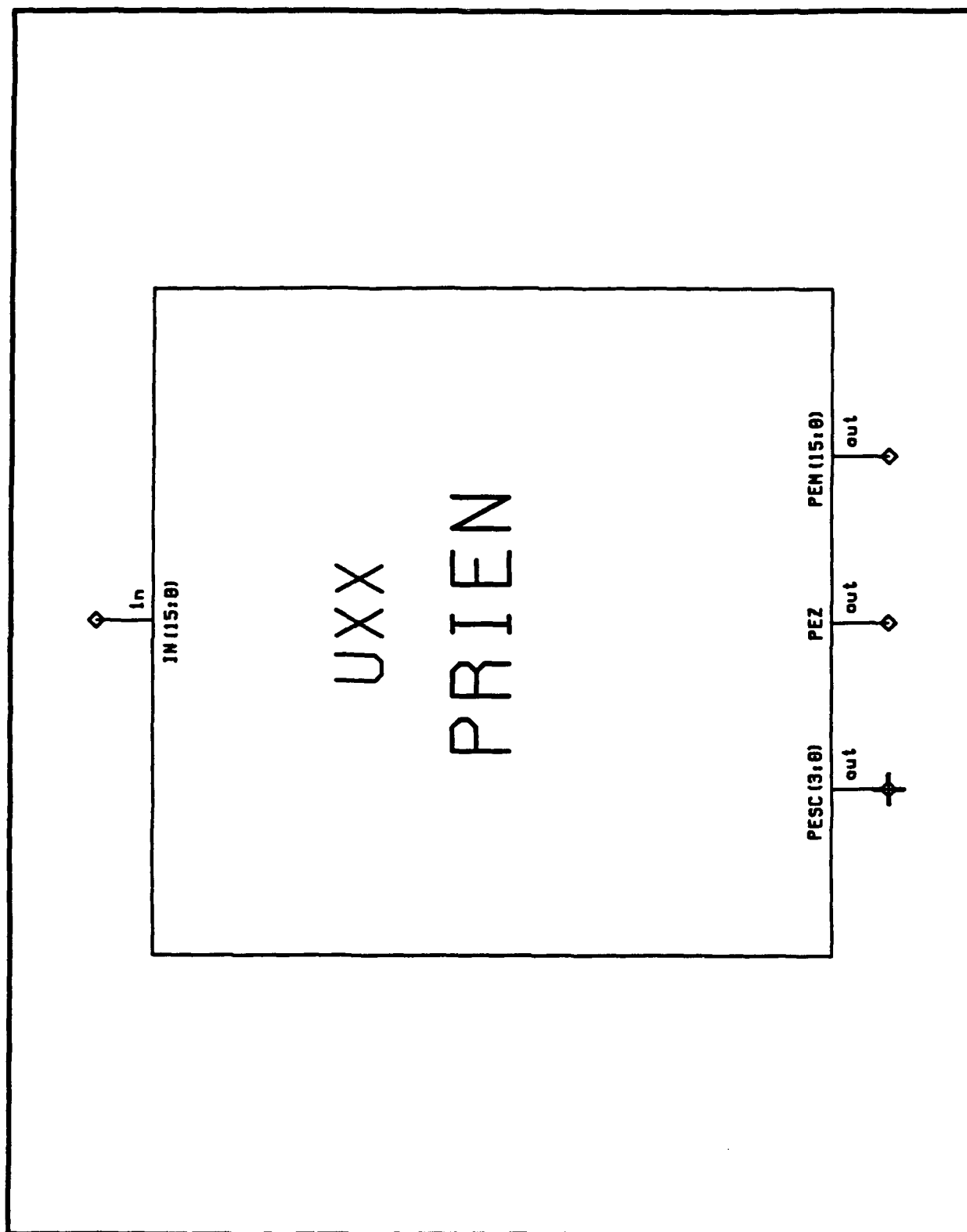


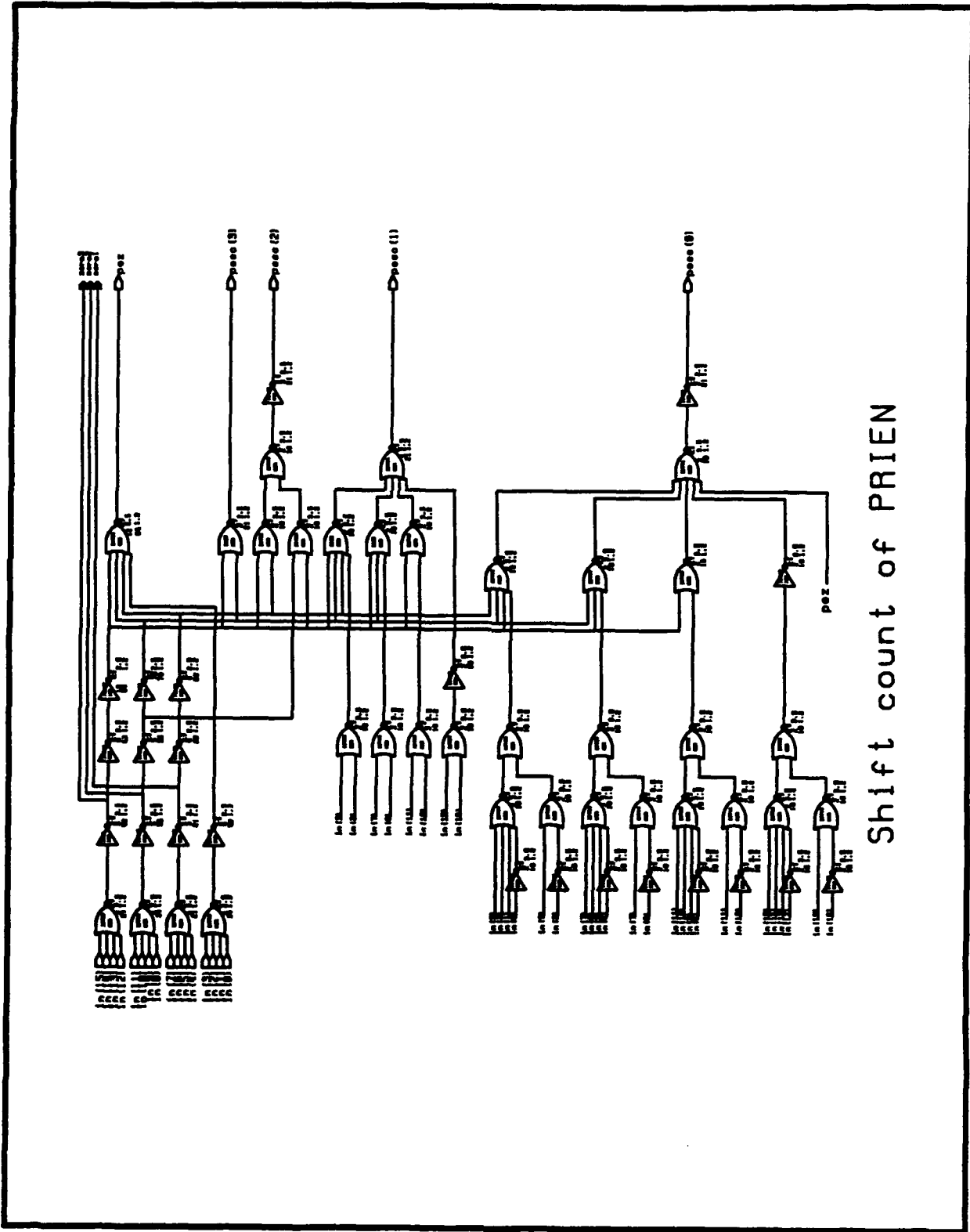




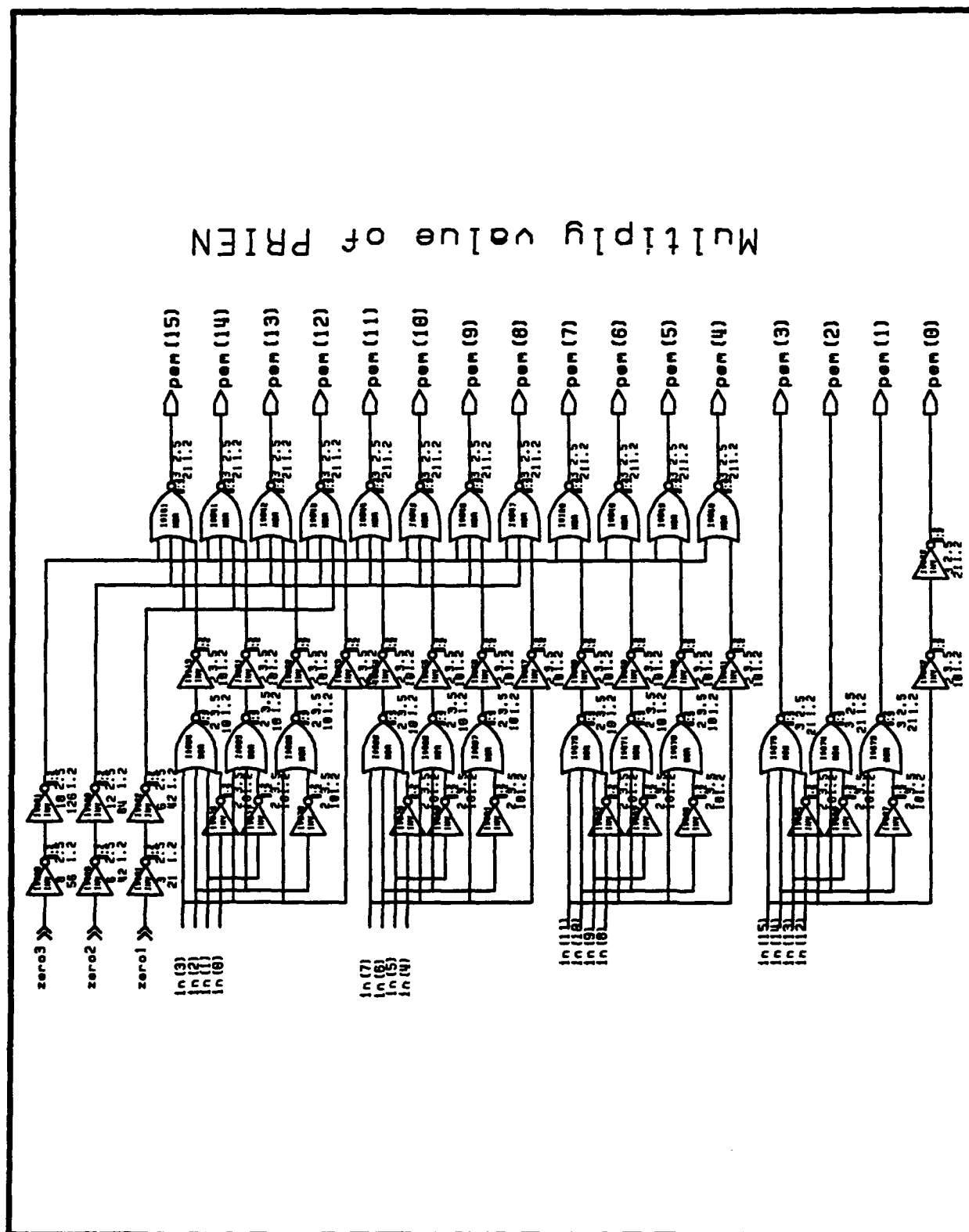


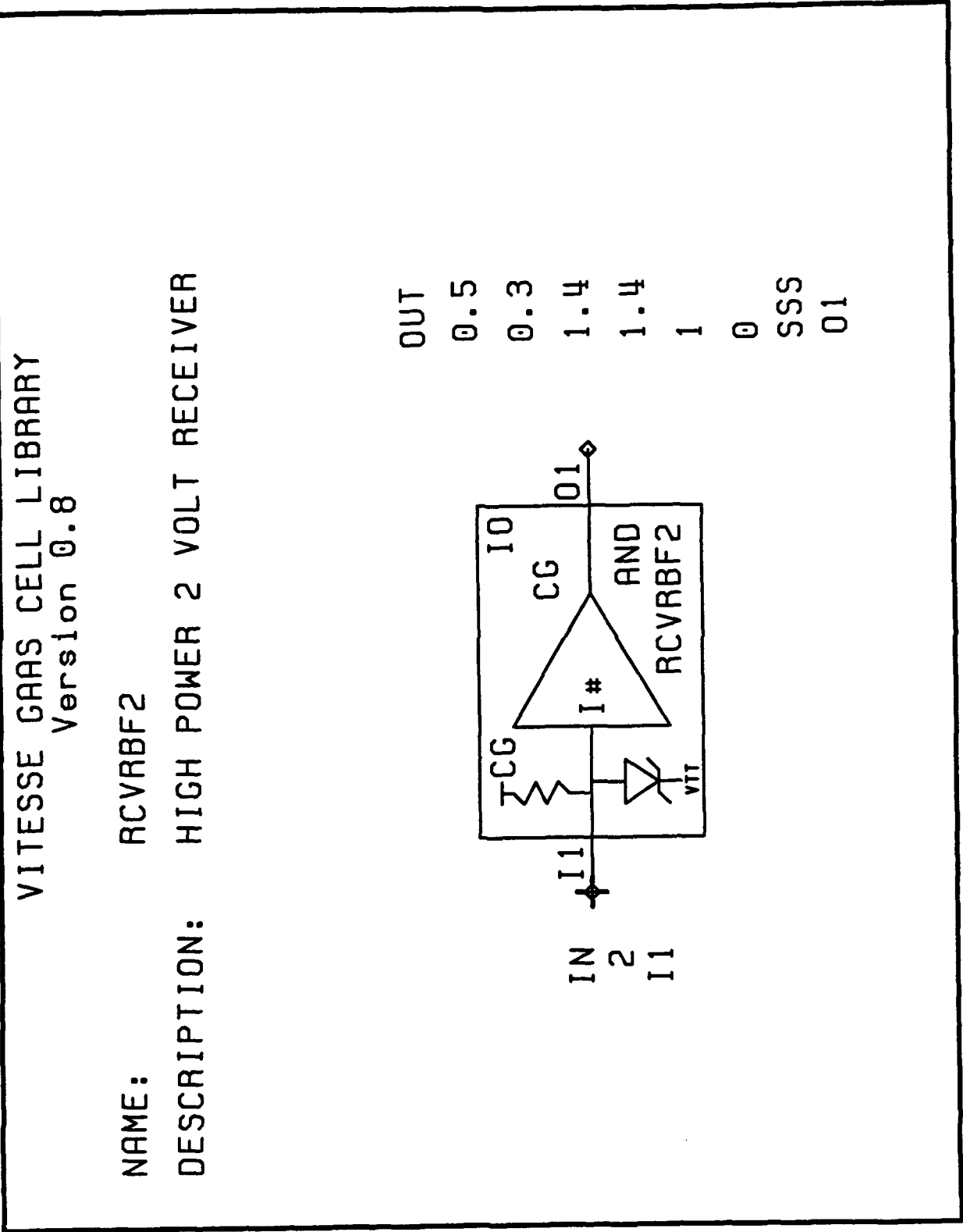
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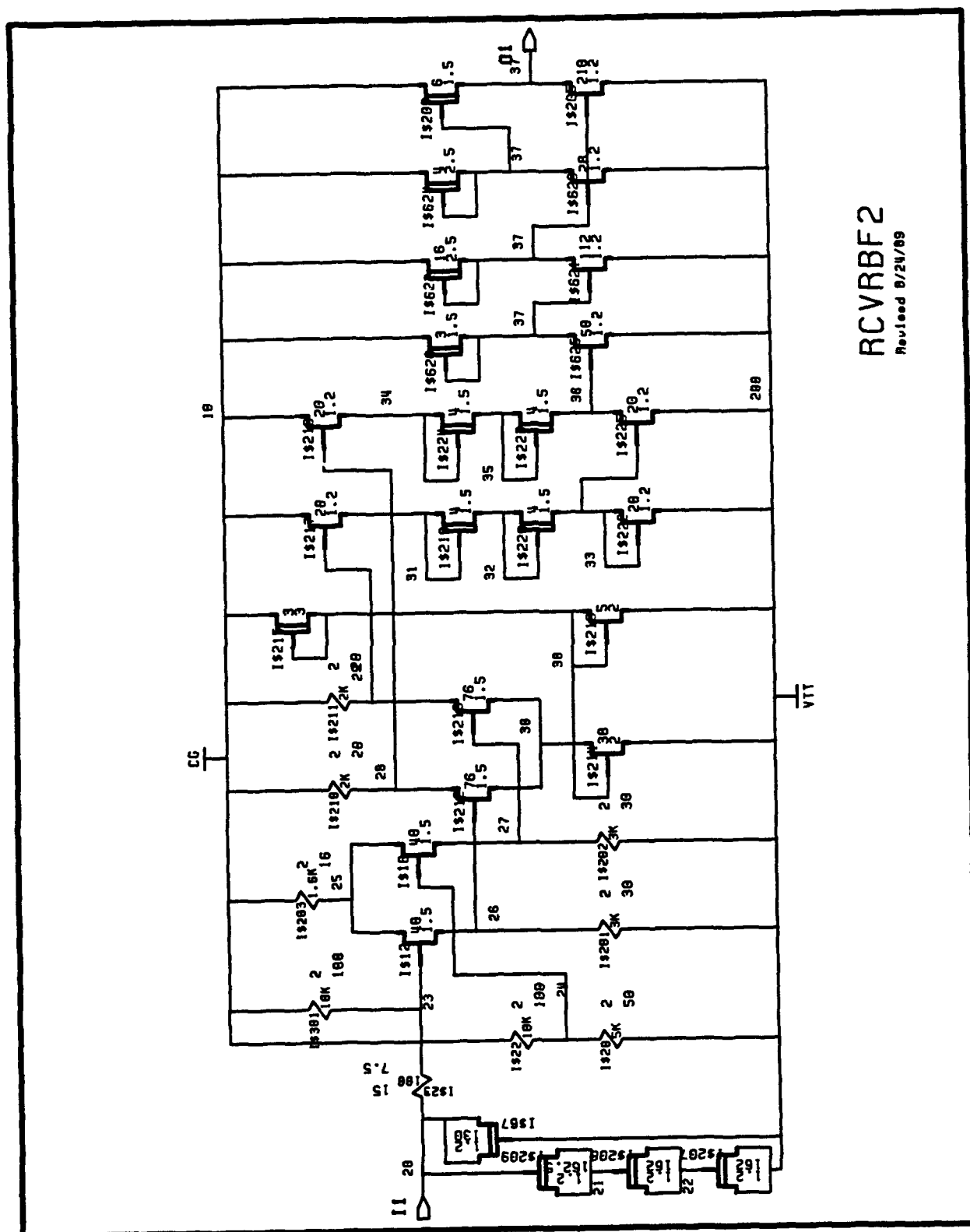








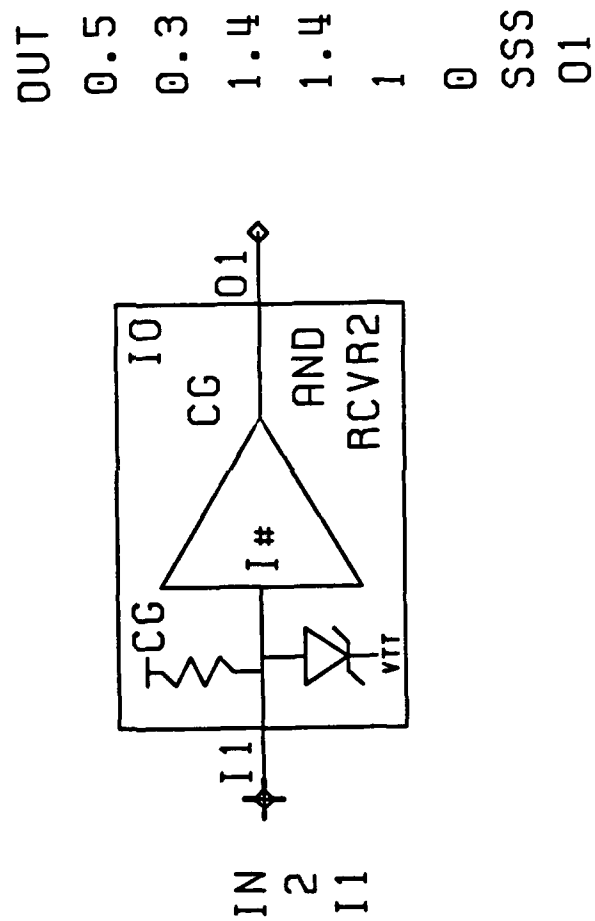


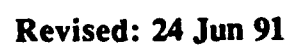


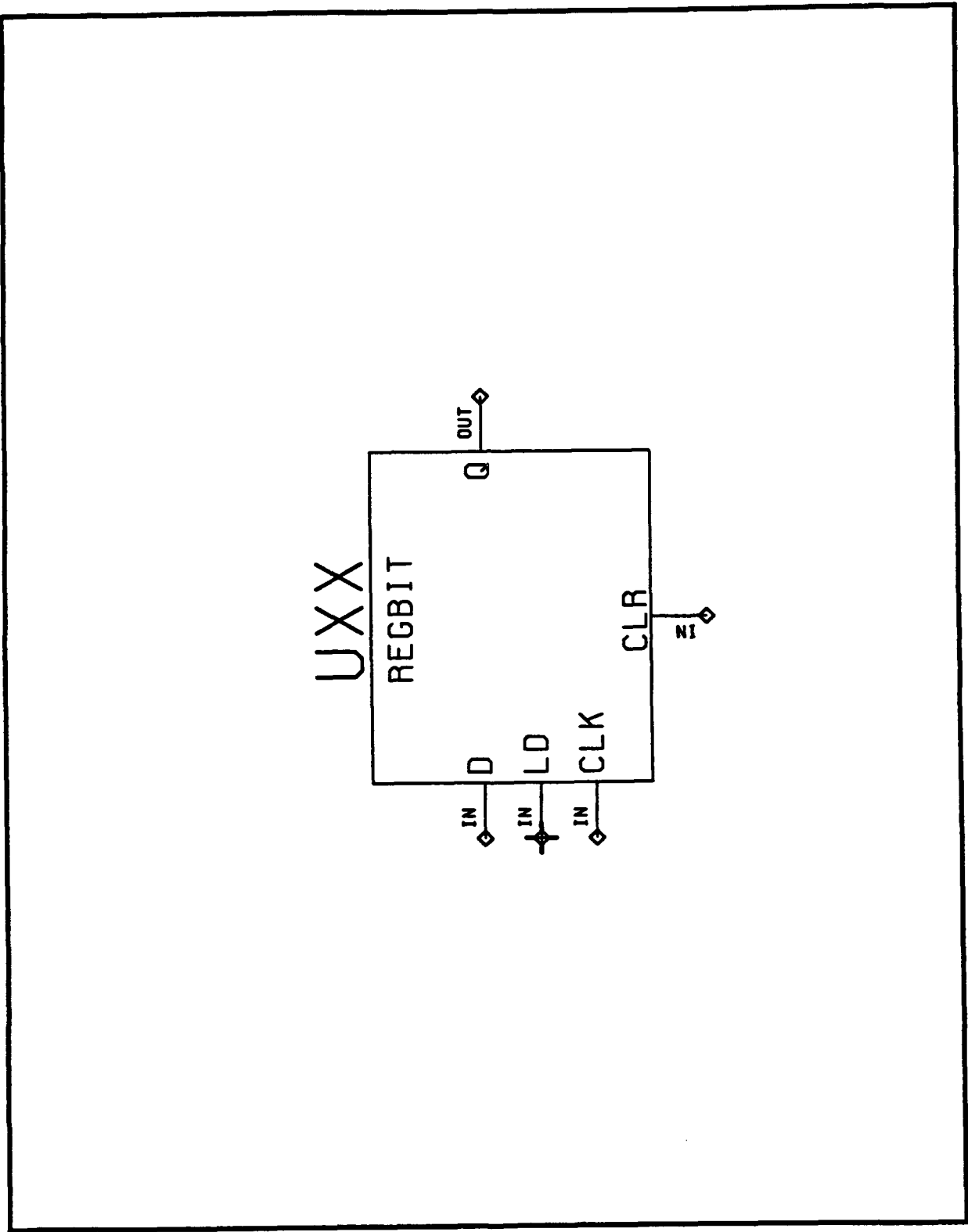
VITESSE GAAS CELL LIBRARY  
Version 0.8

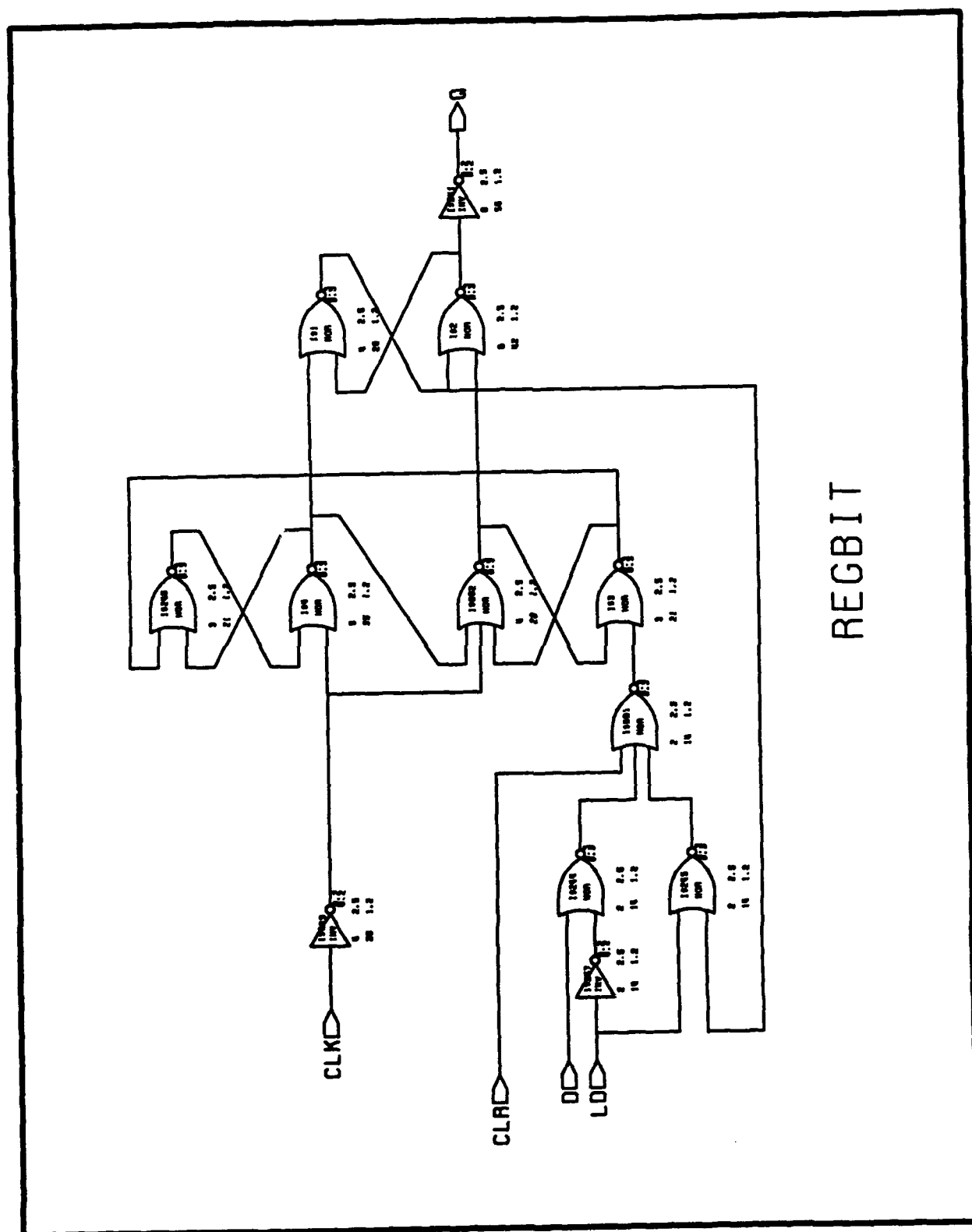
NAME: RCVR2

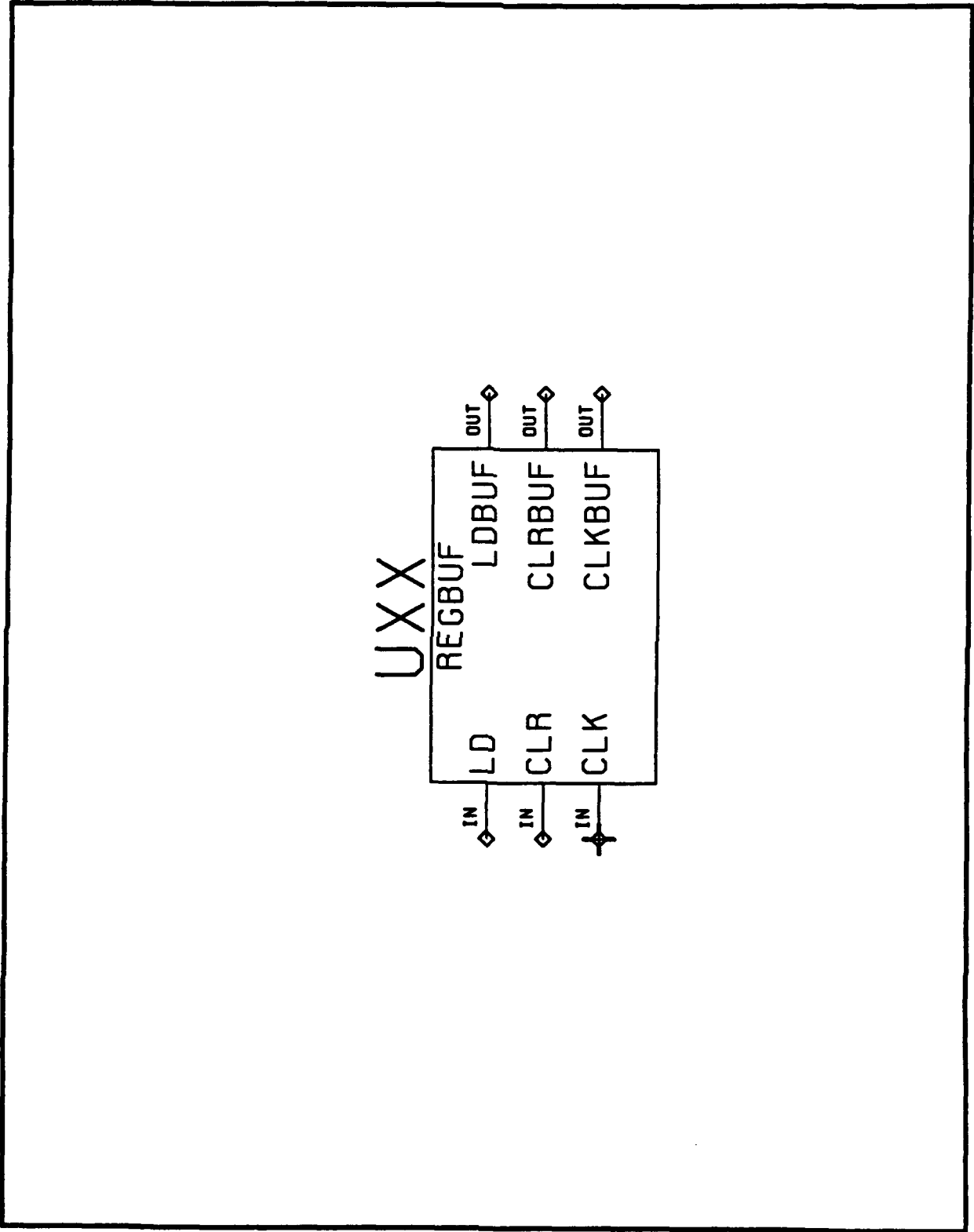
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD



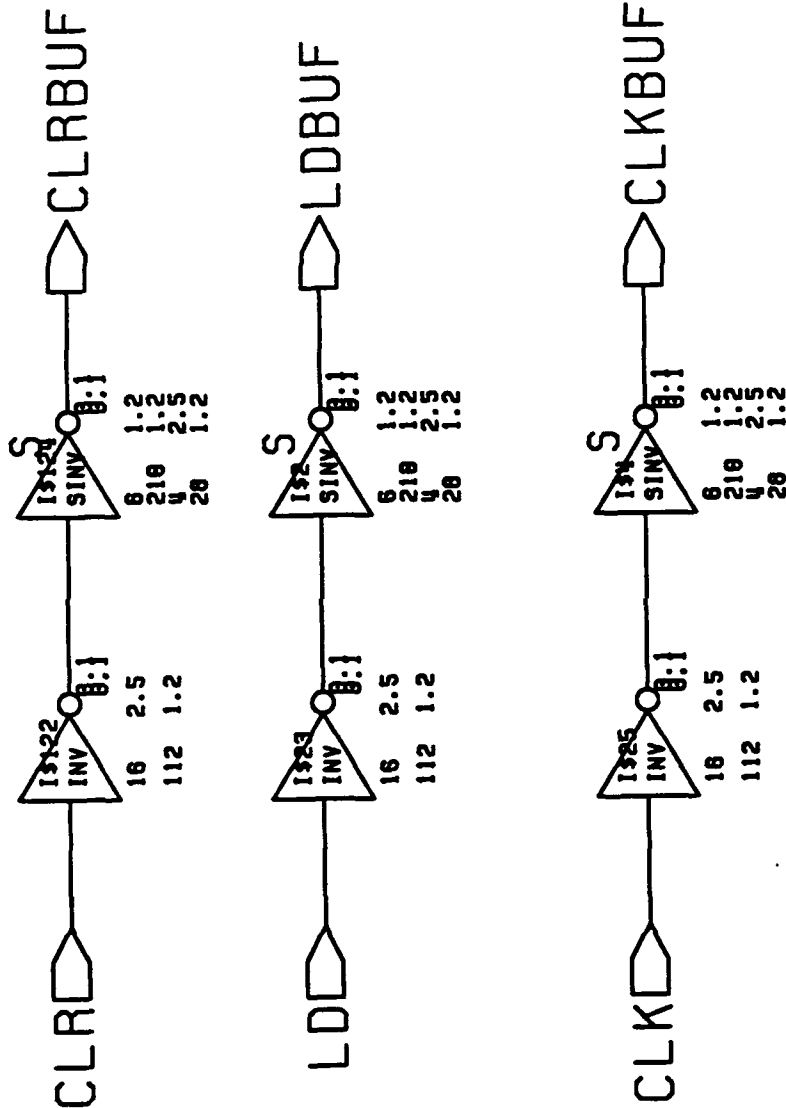


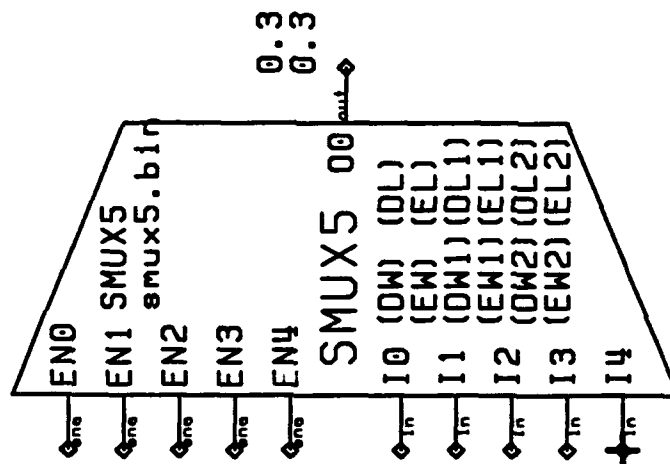


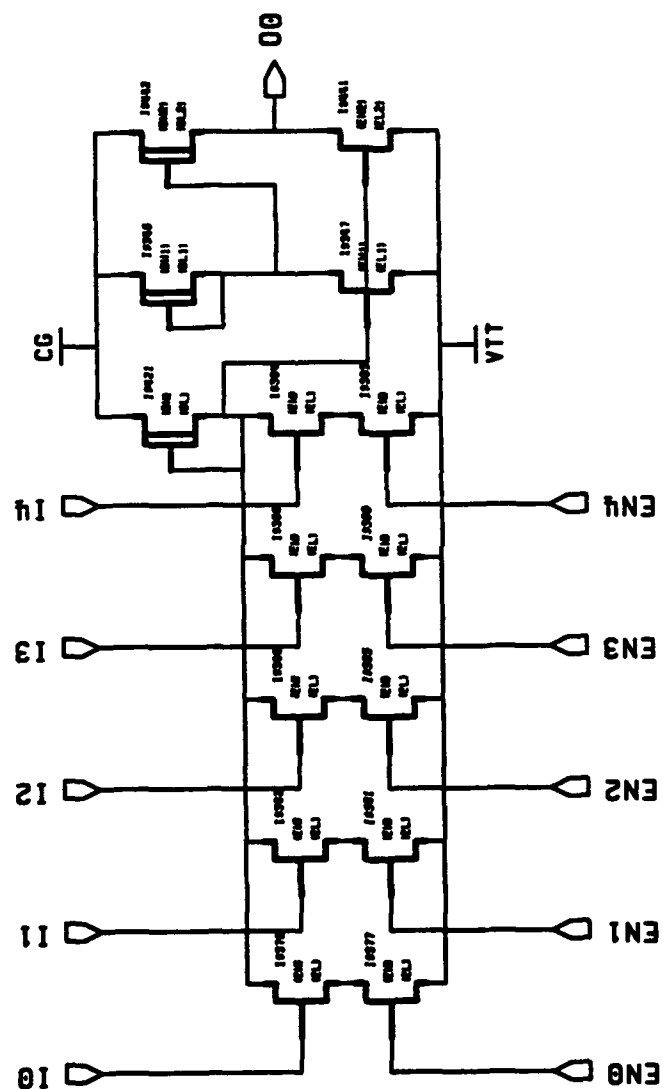




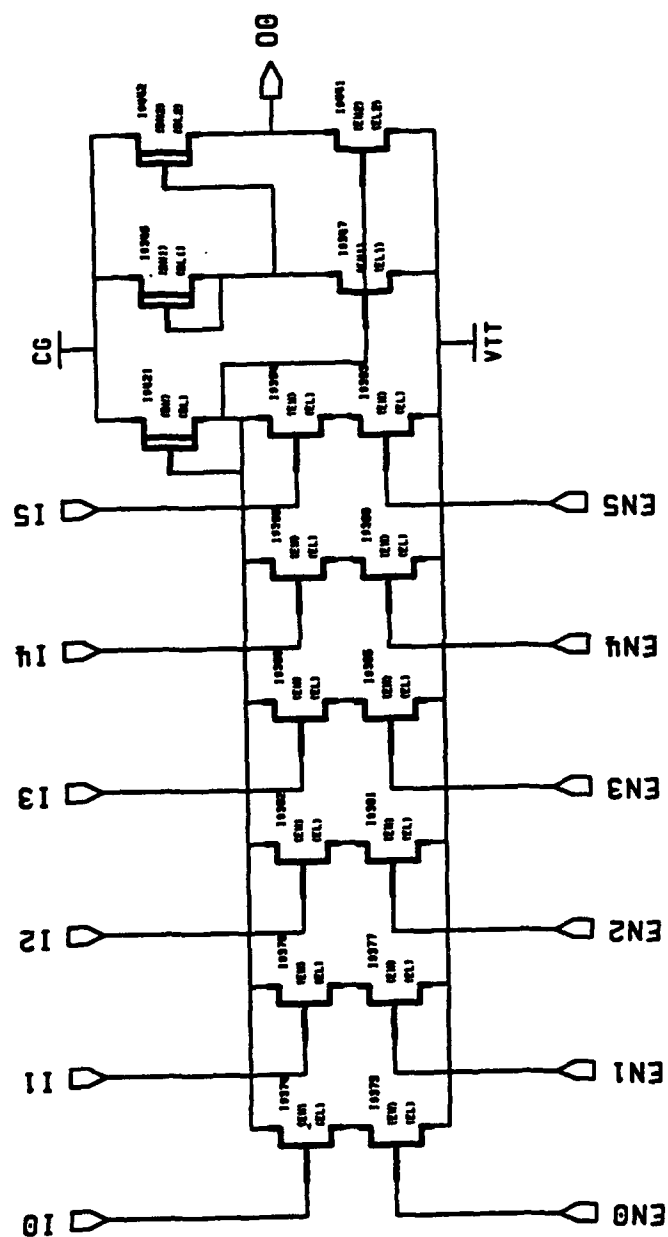


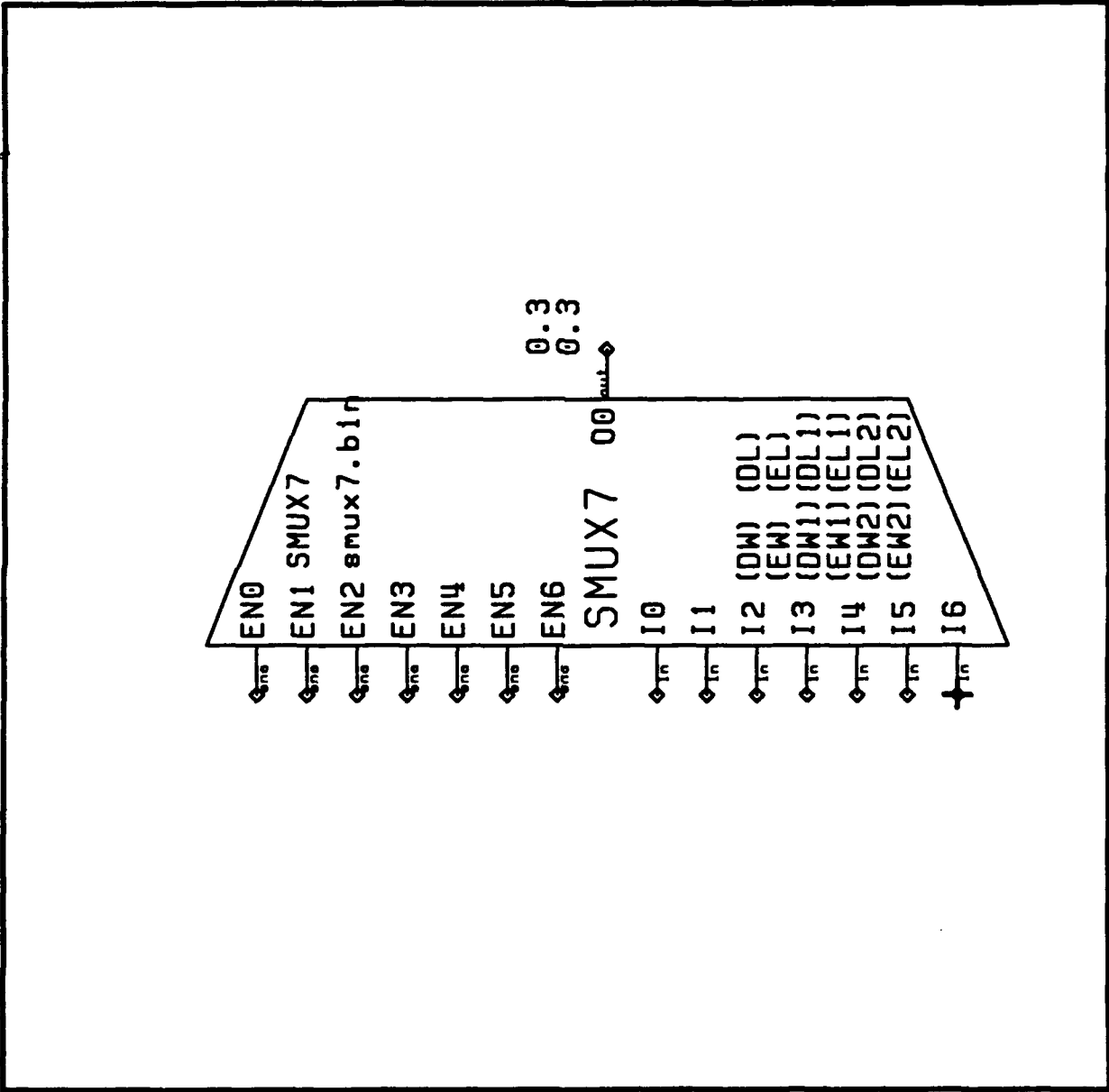


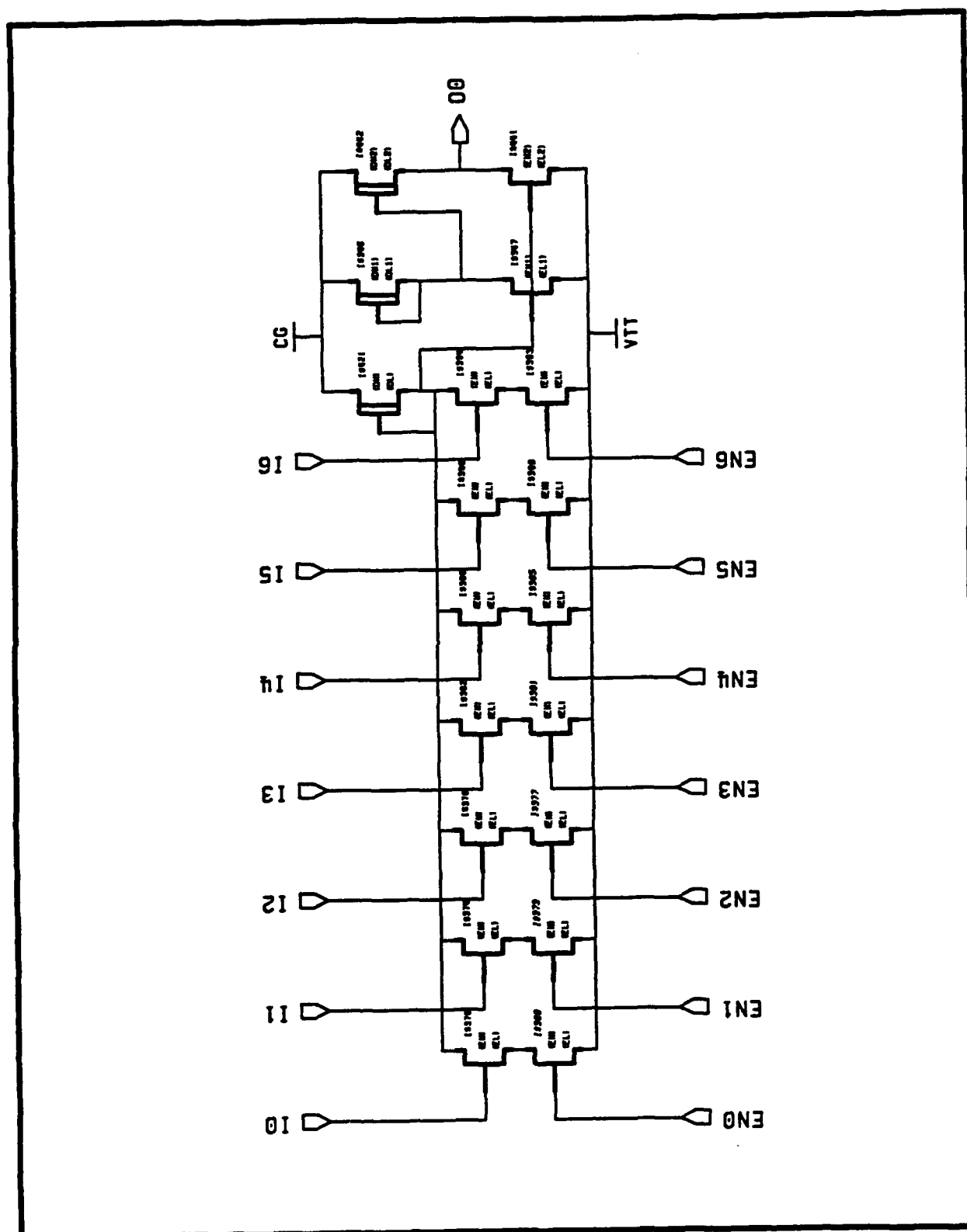


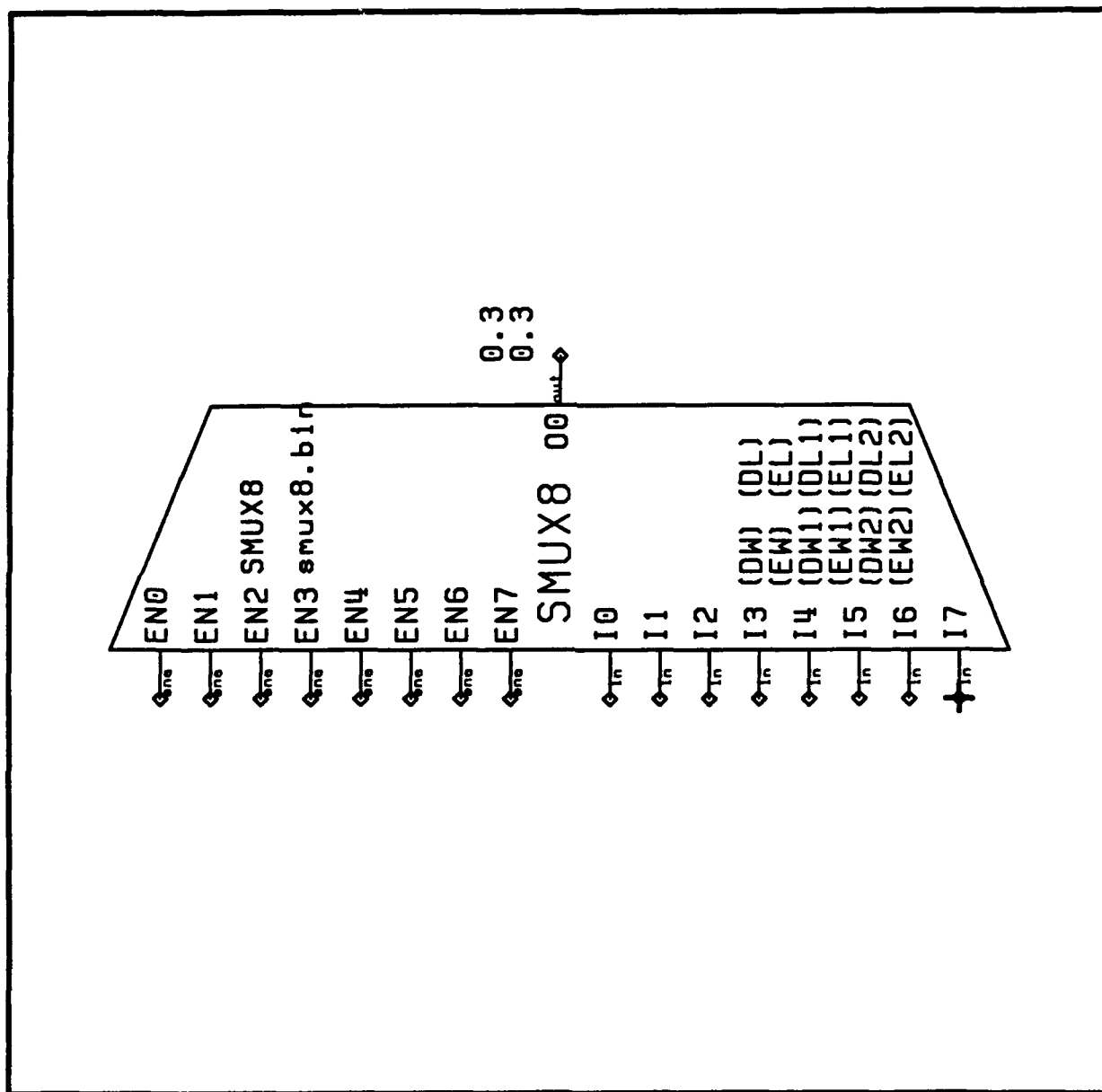




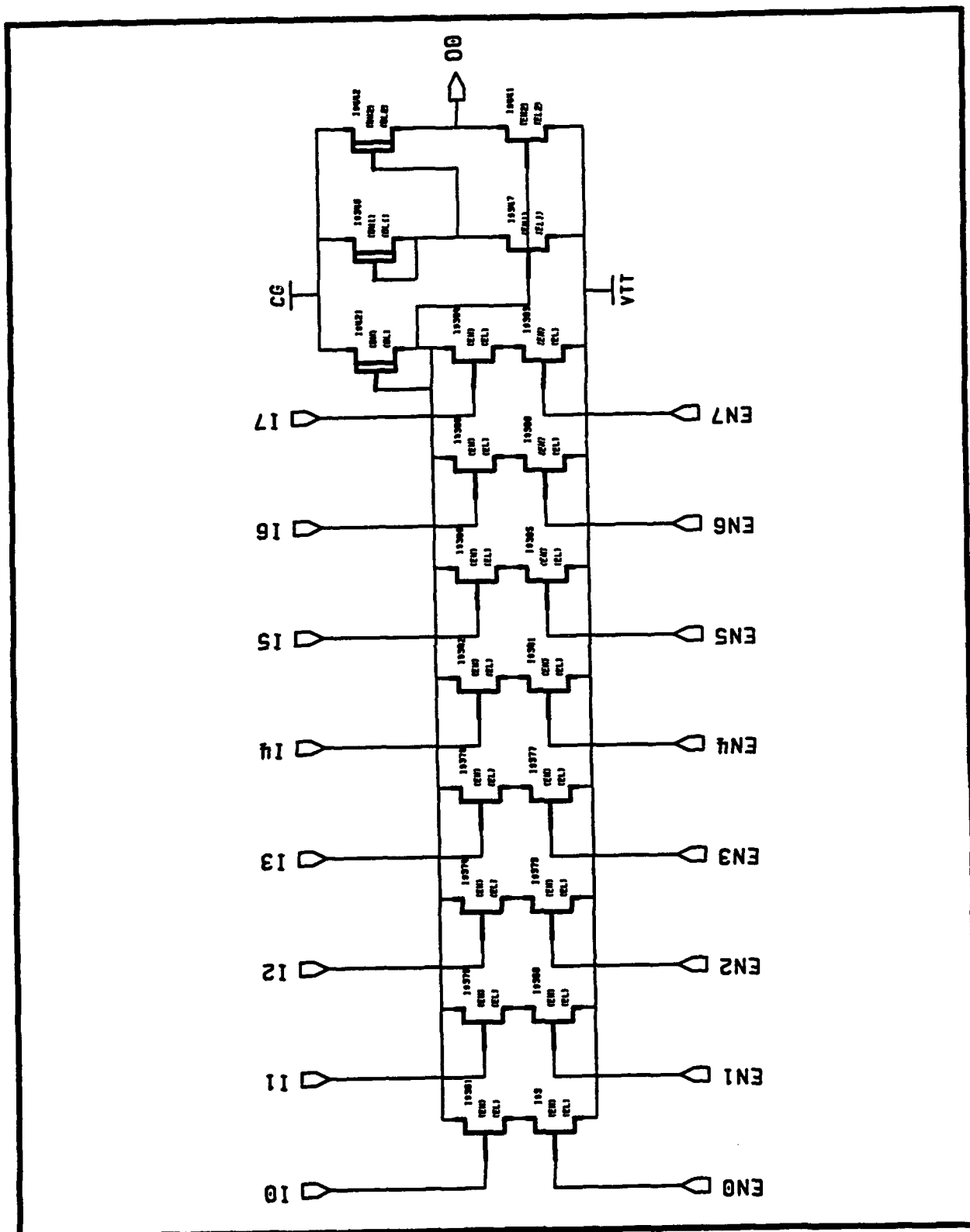


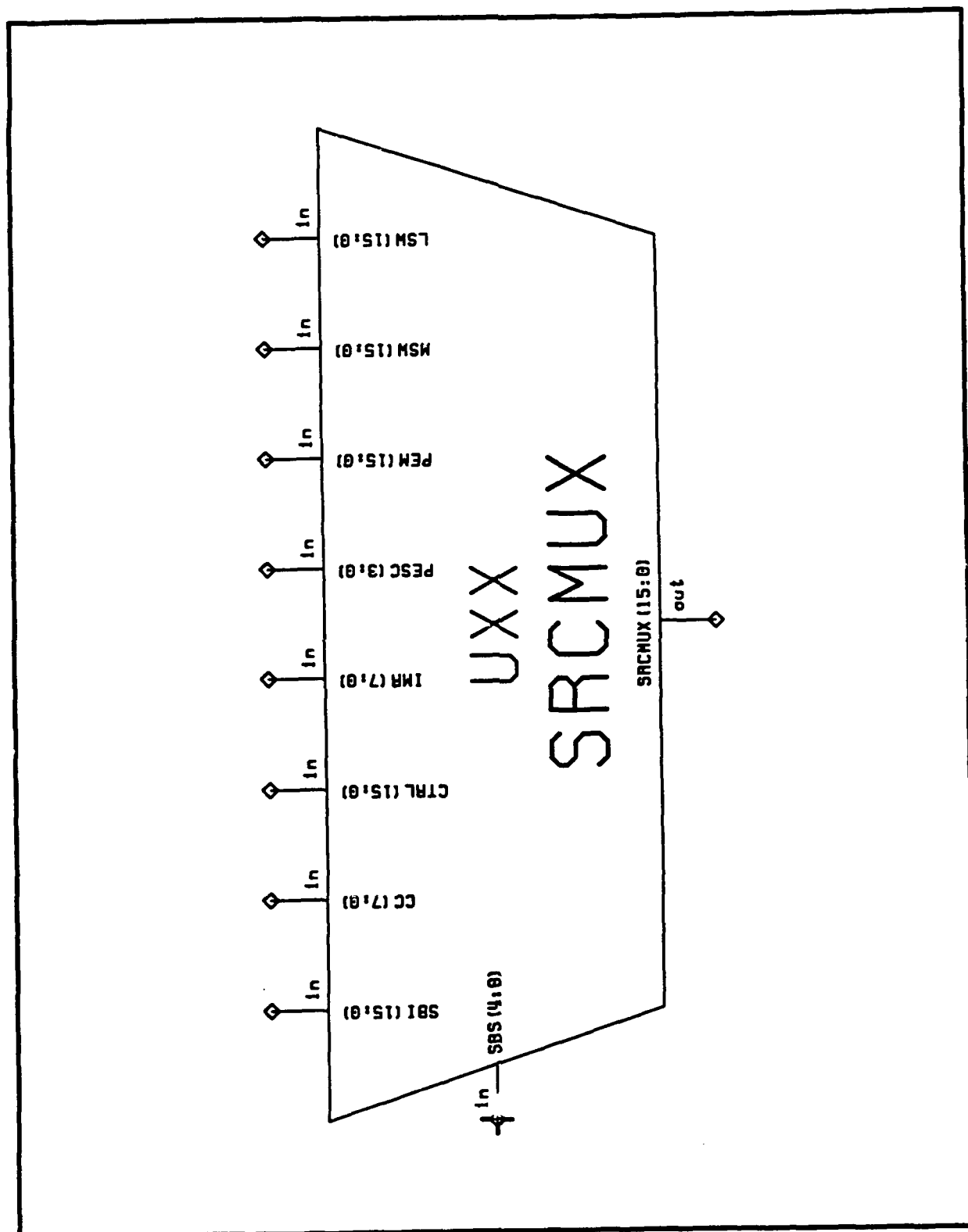


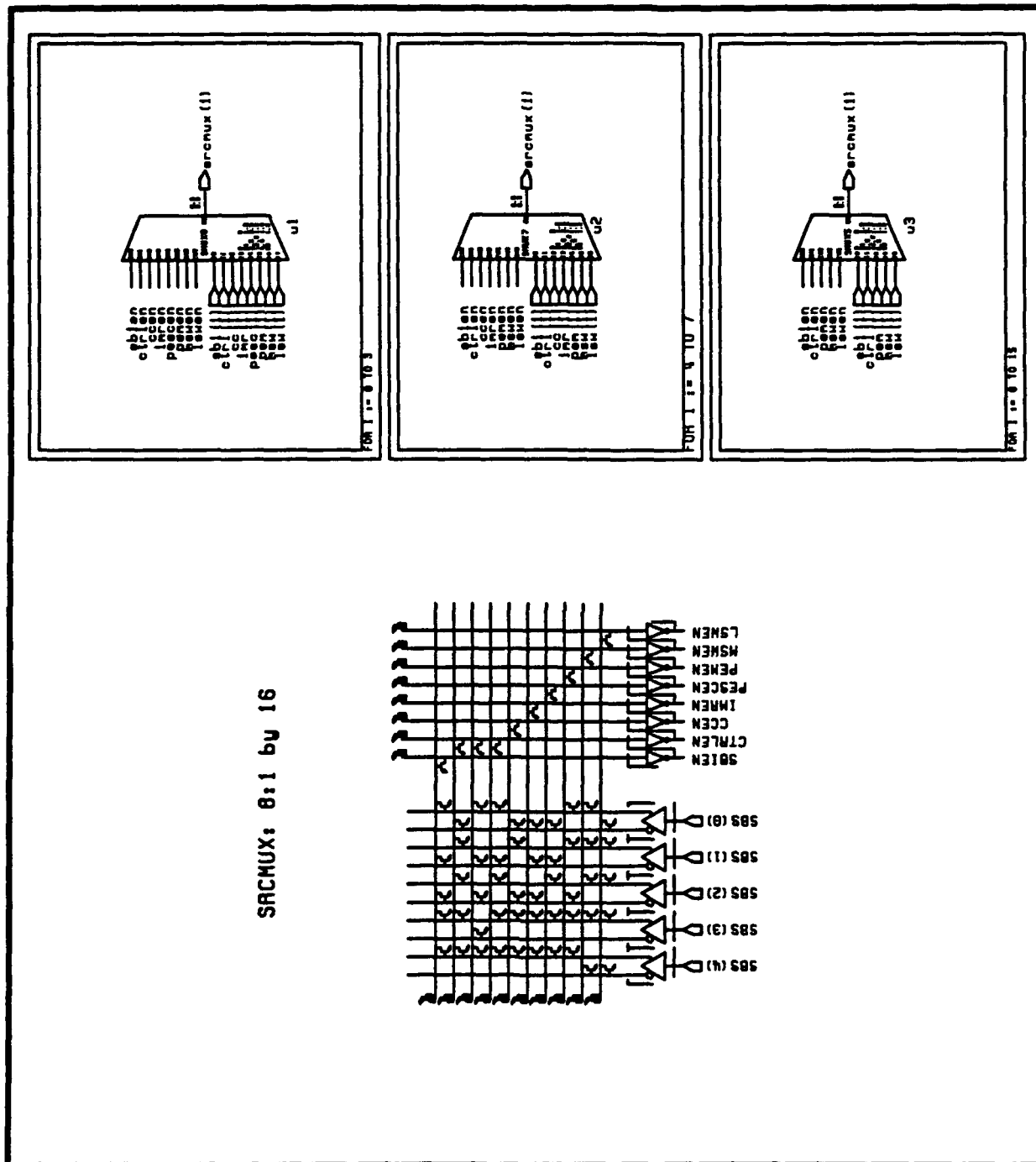


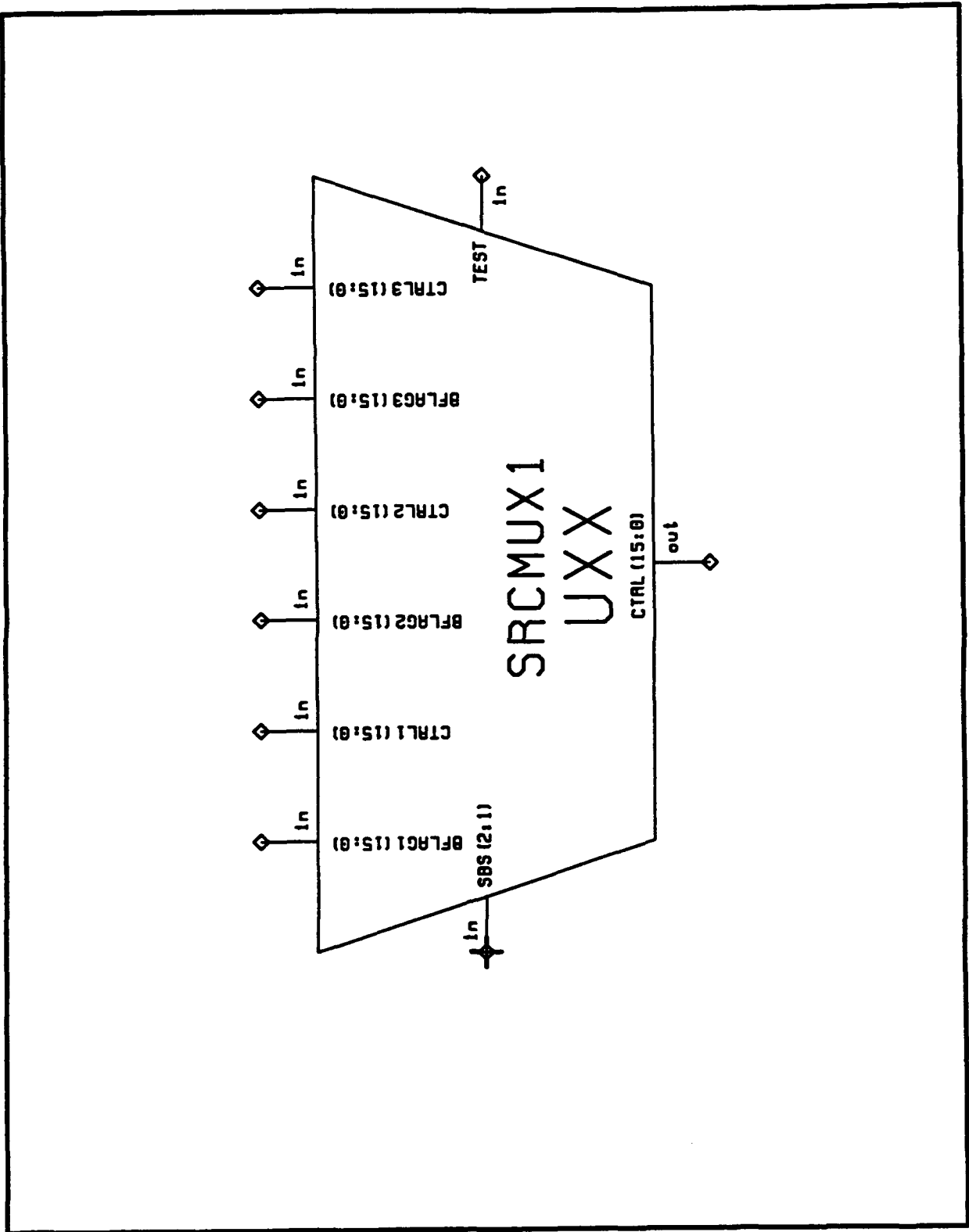


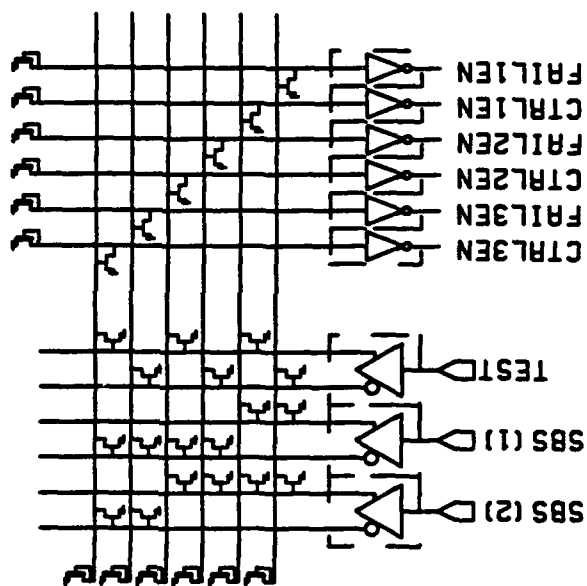
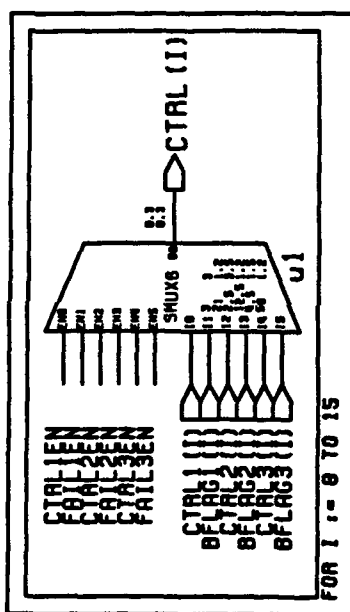




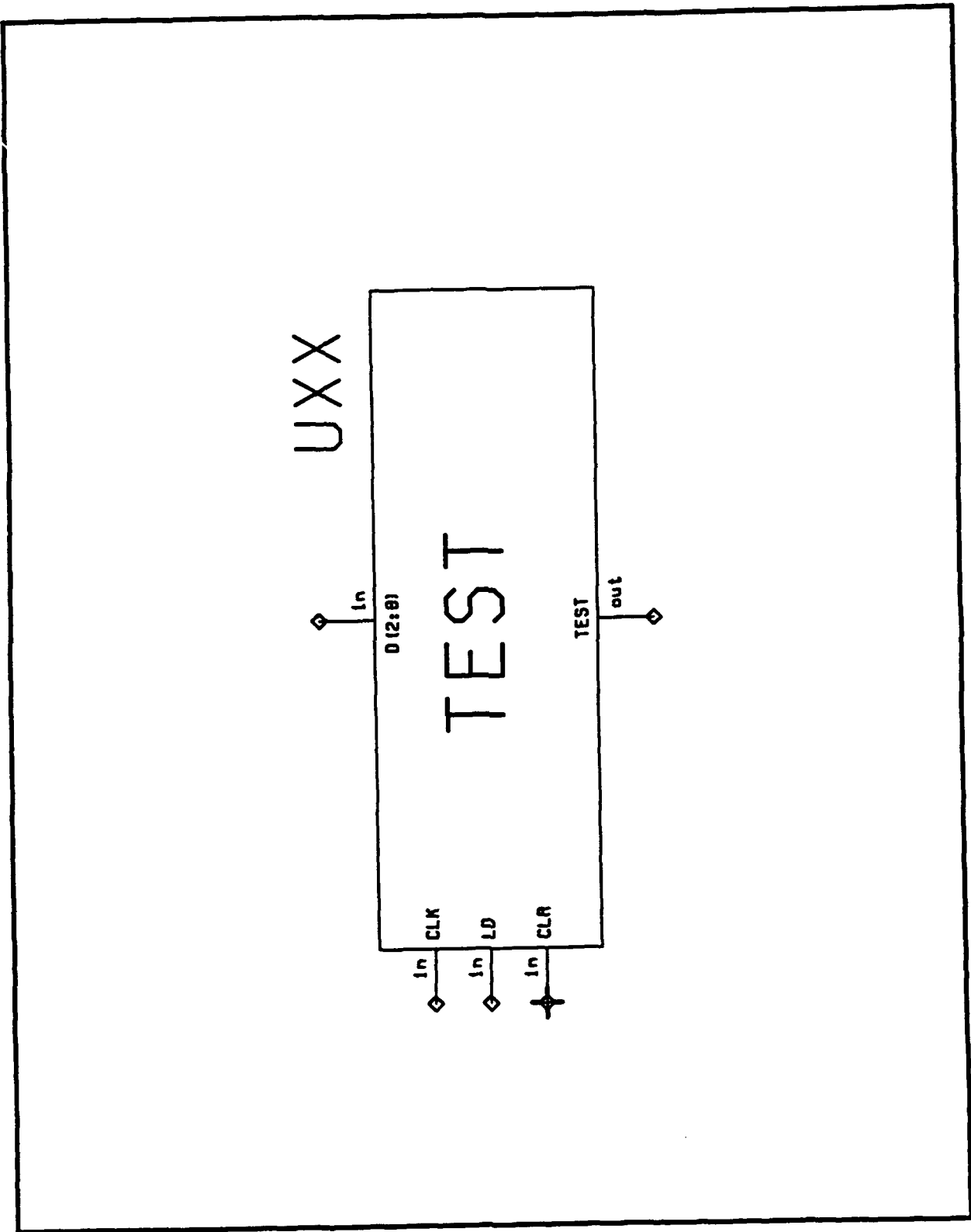


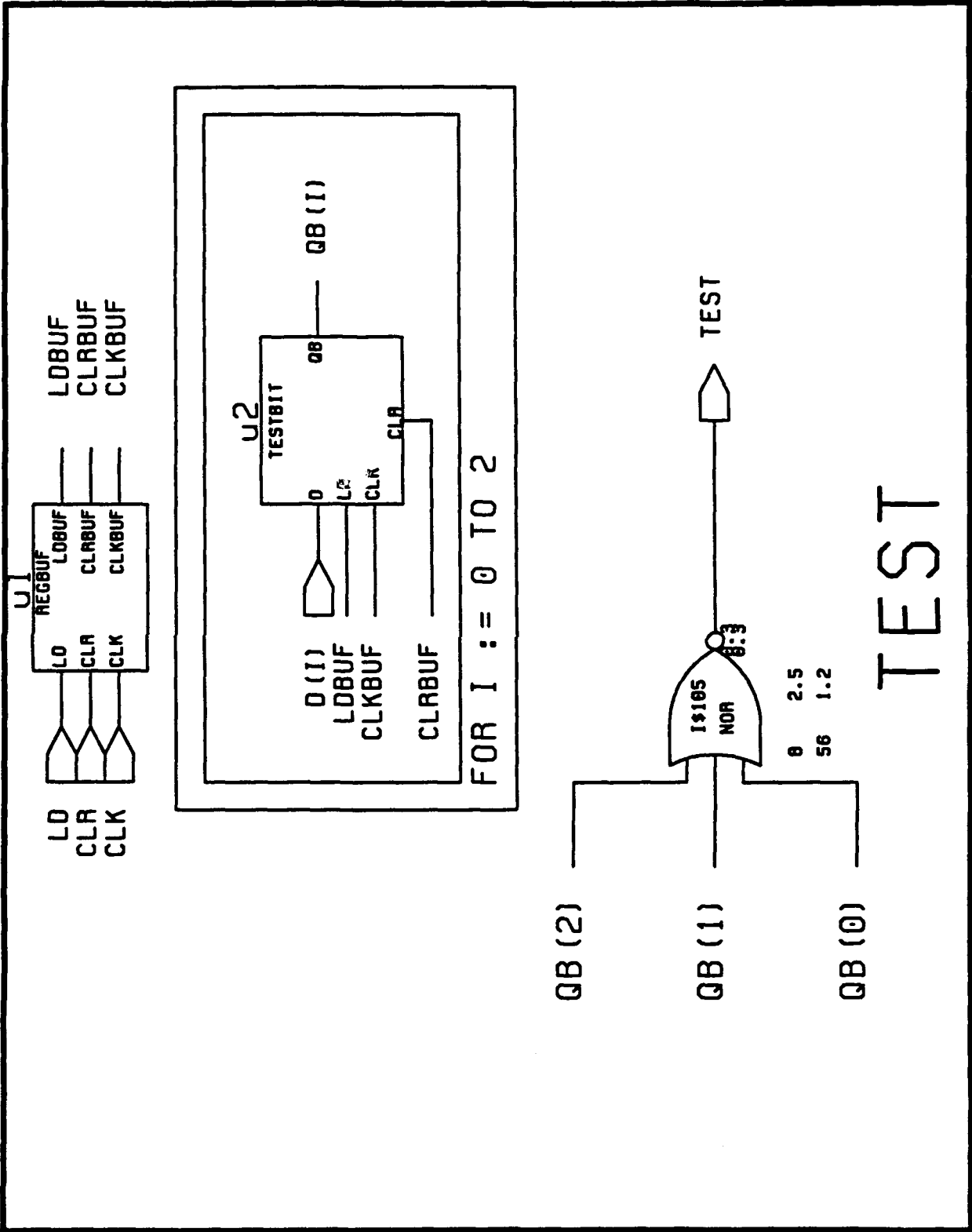


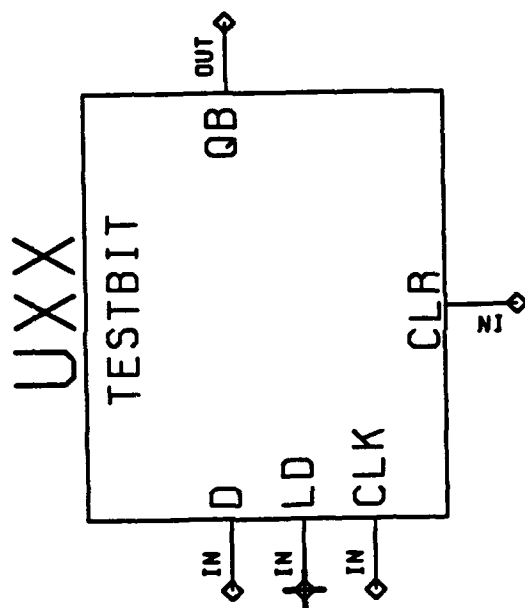




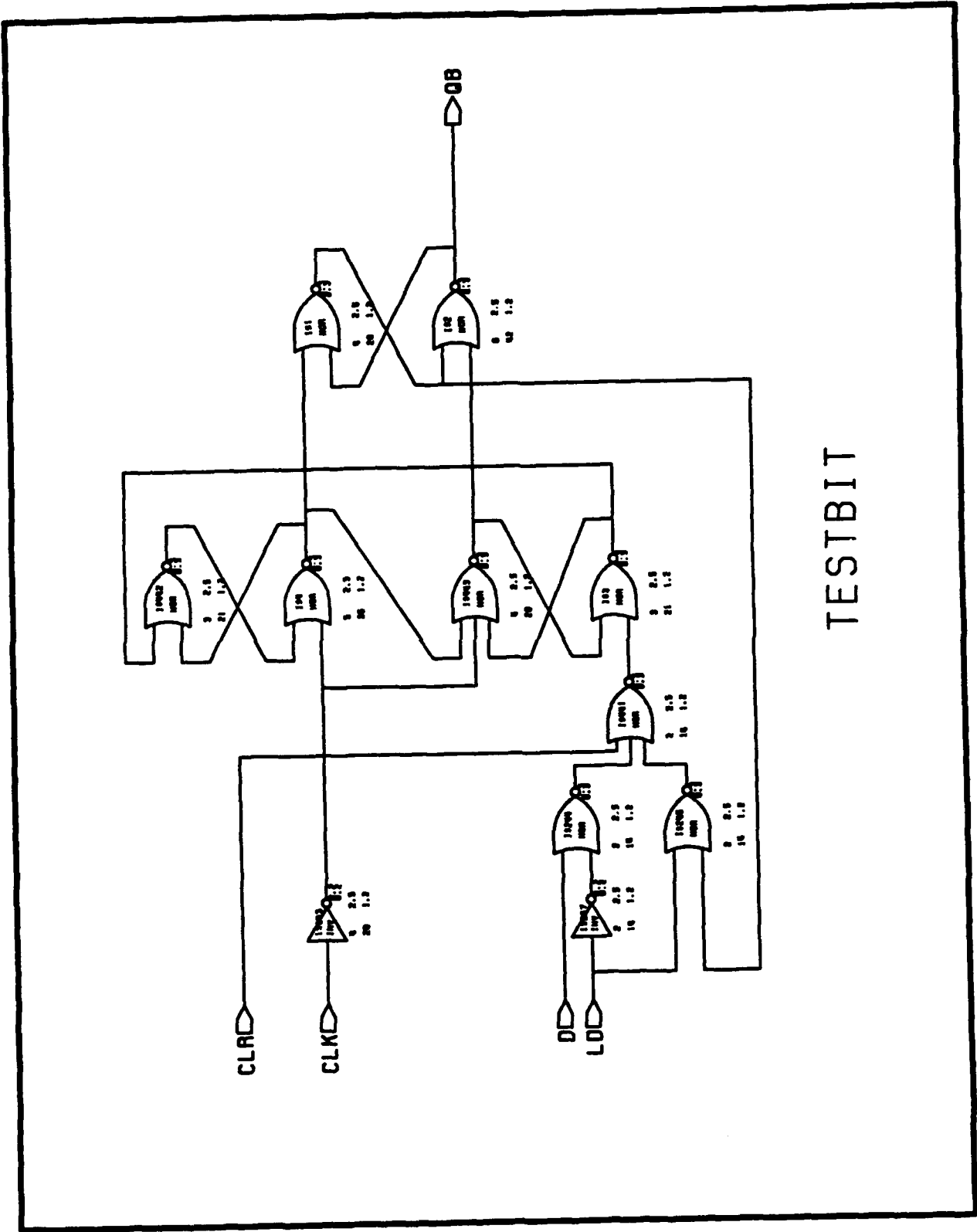
SRCMUX1



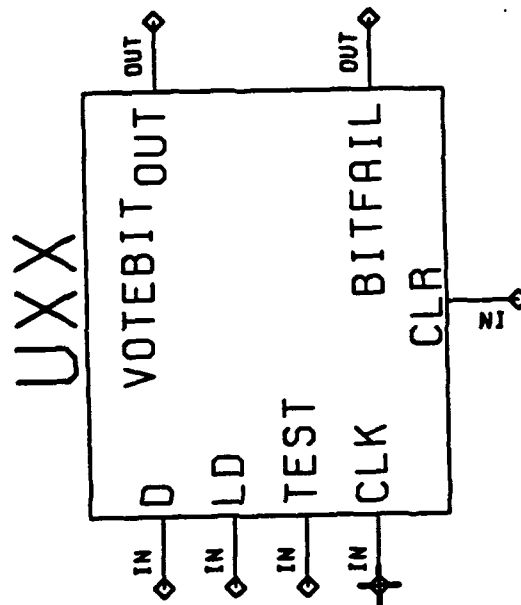




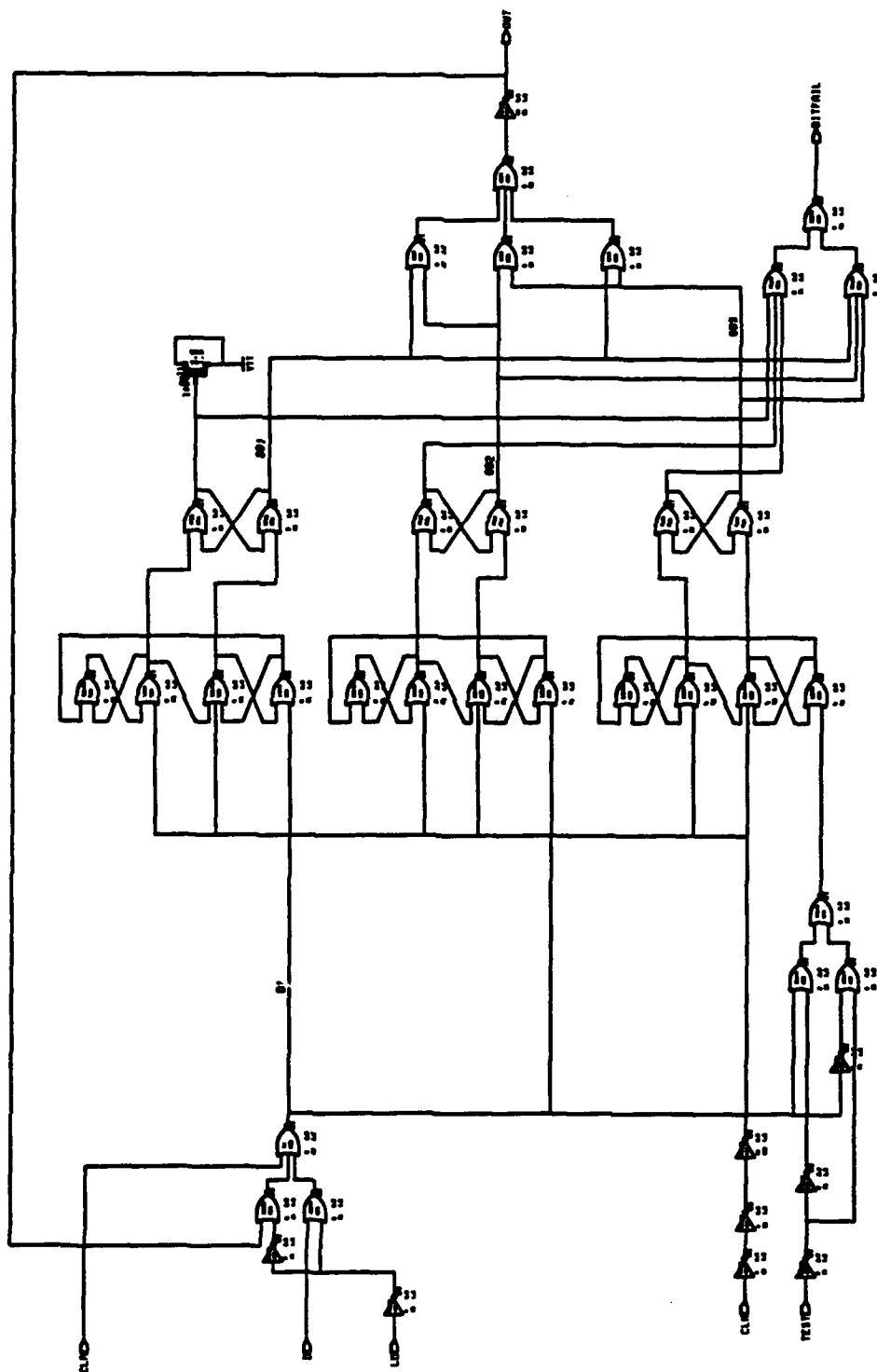


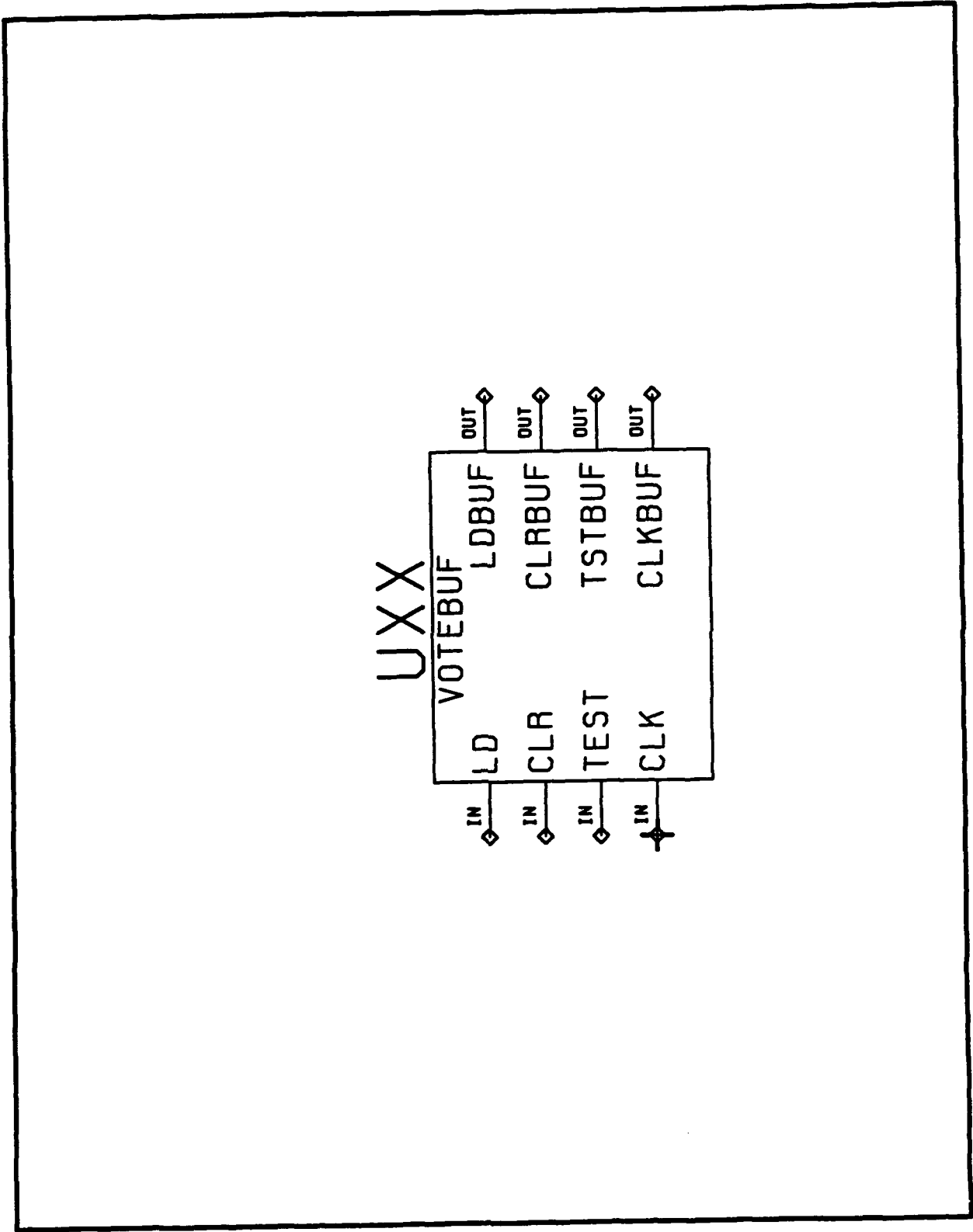


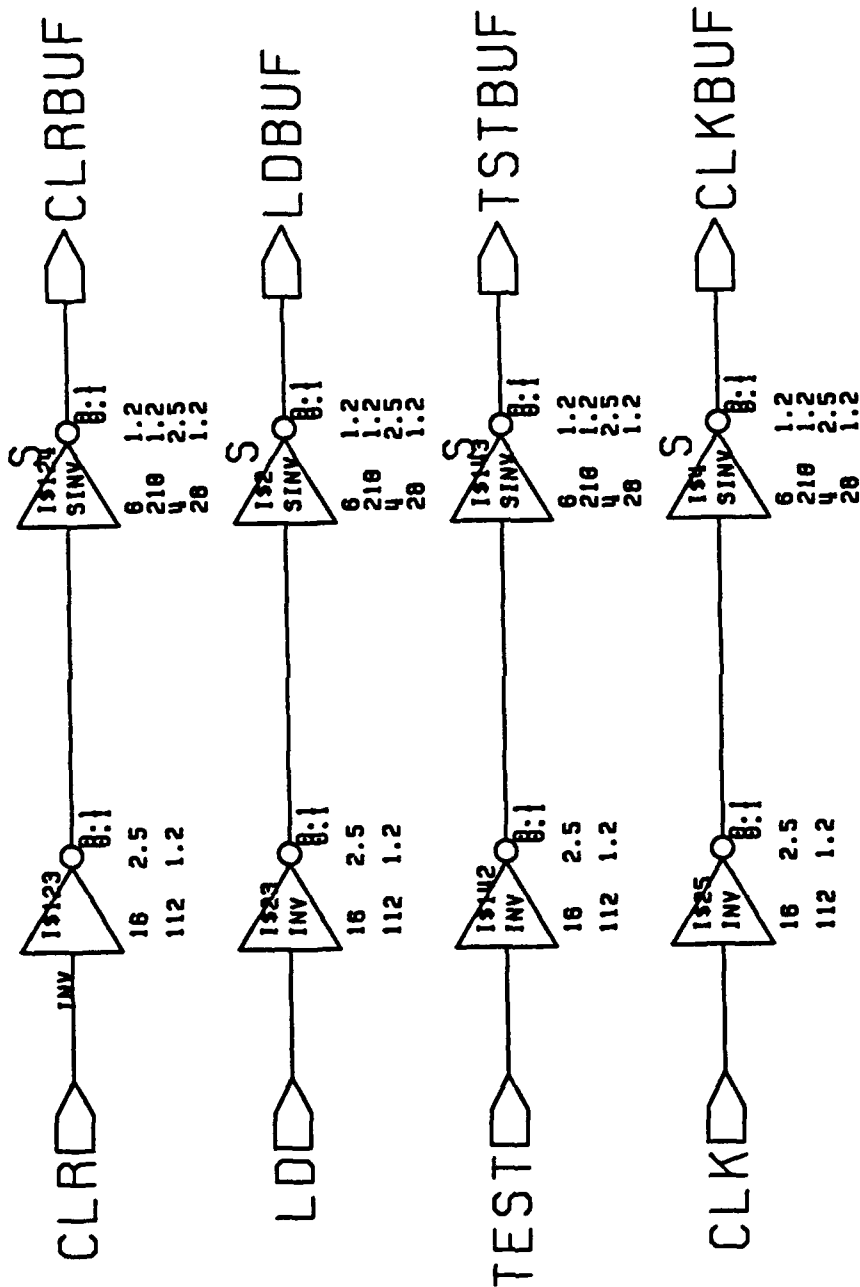
TESTBIT



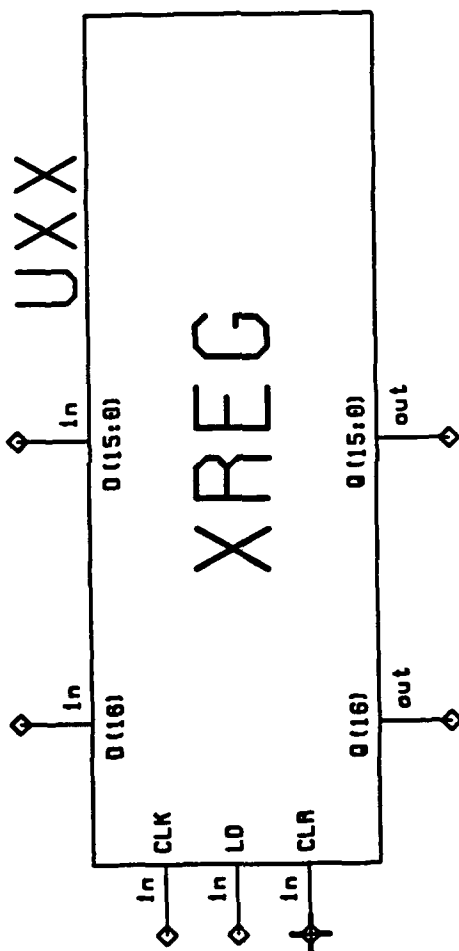
MAJORITY VOTE CIRCUIT WITH LATCHED INPUTS

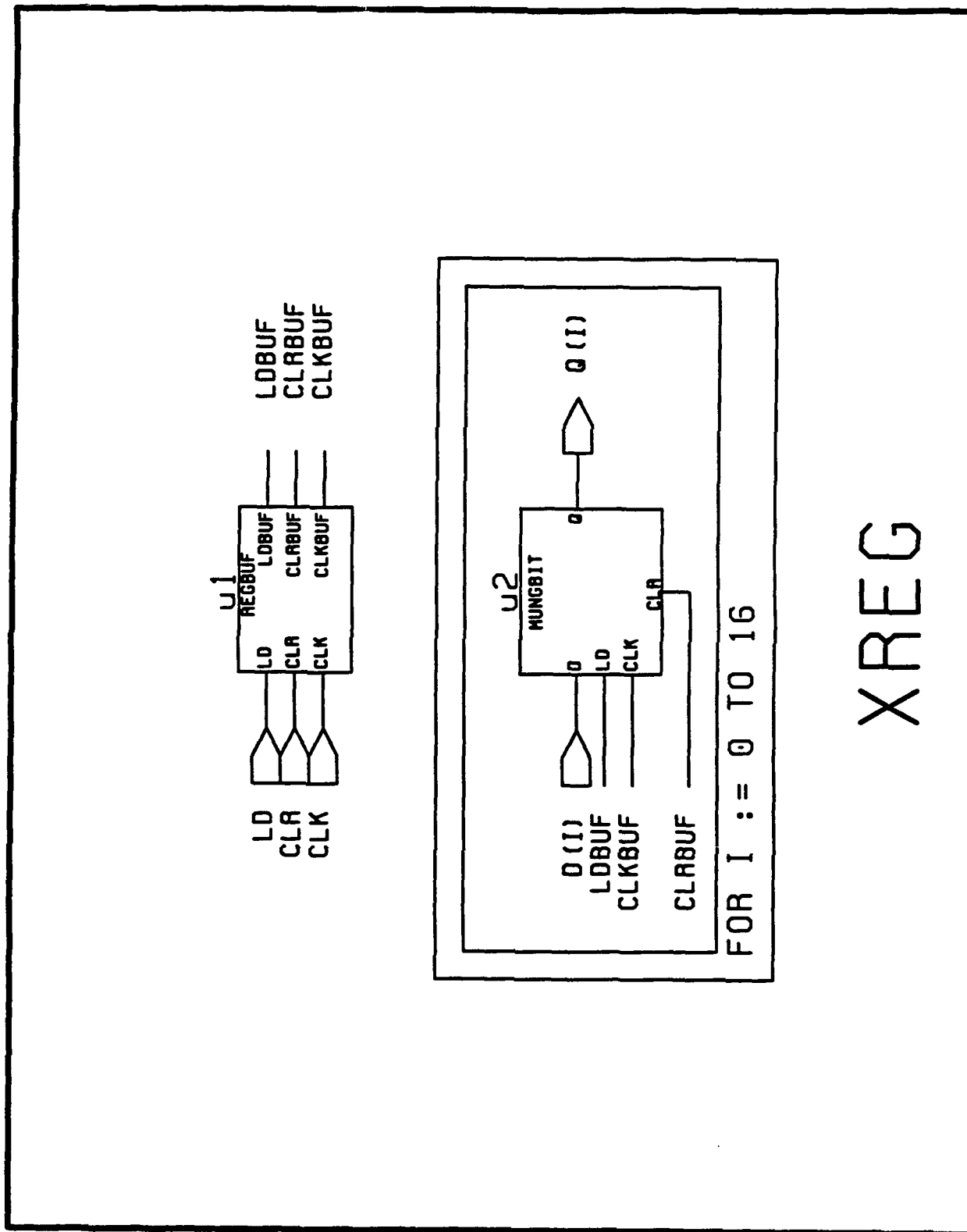


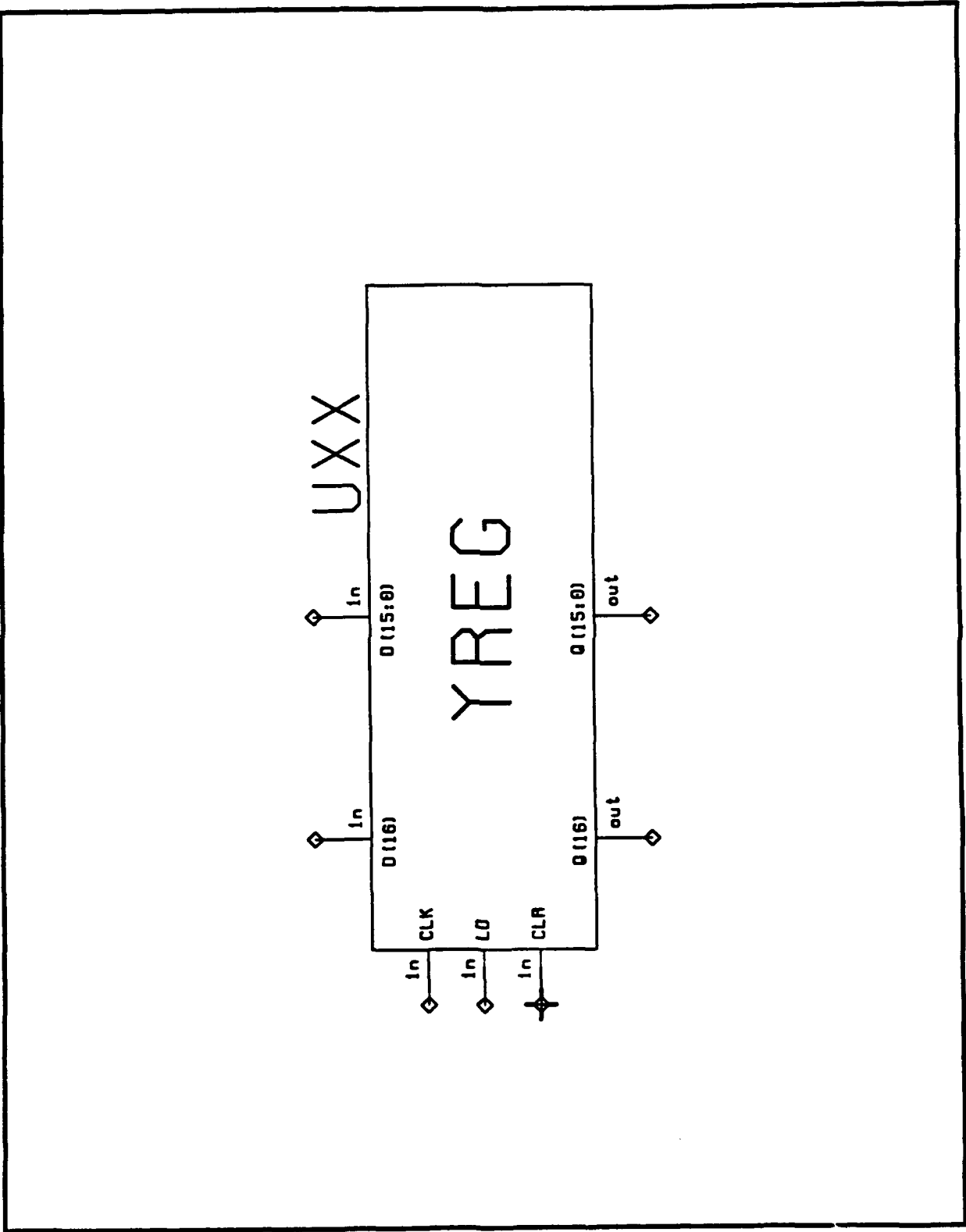




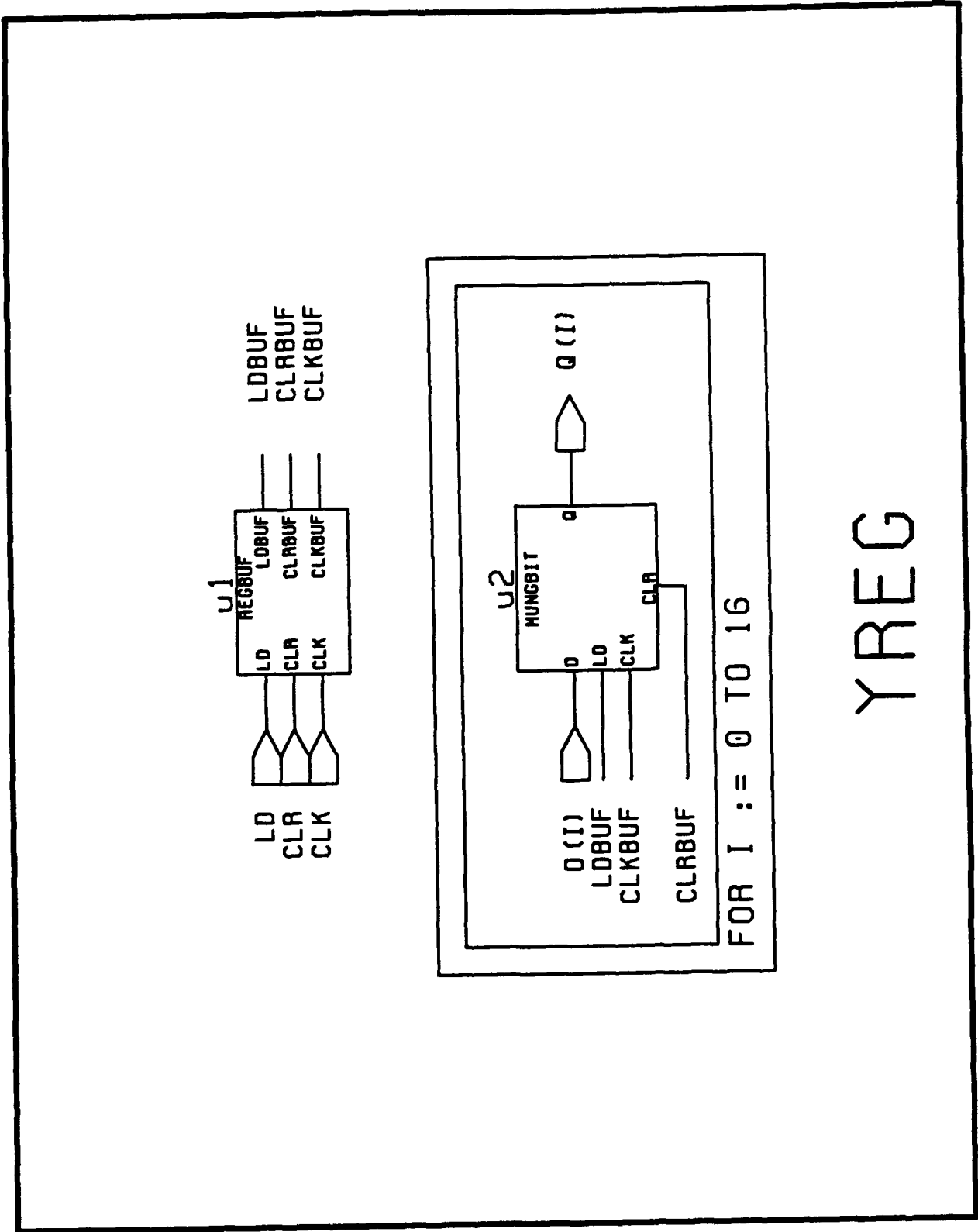
VOTEBUF: buffer for VOTEBIT



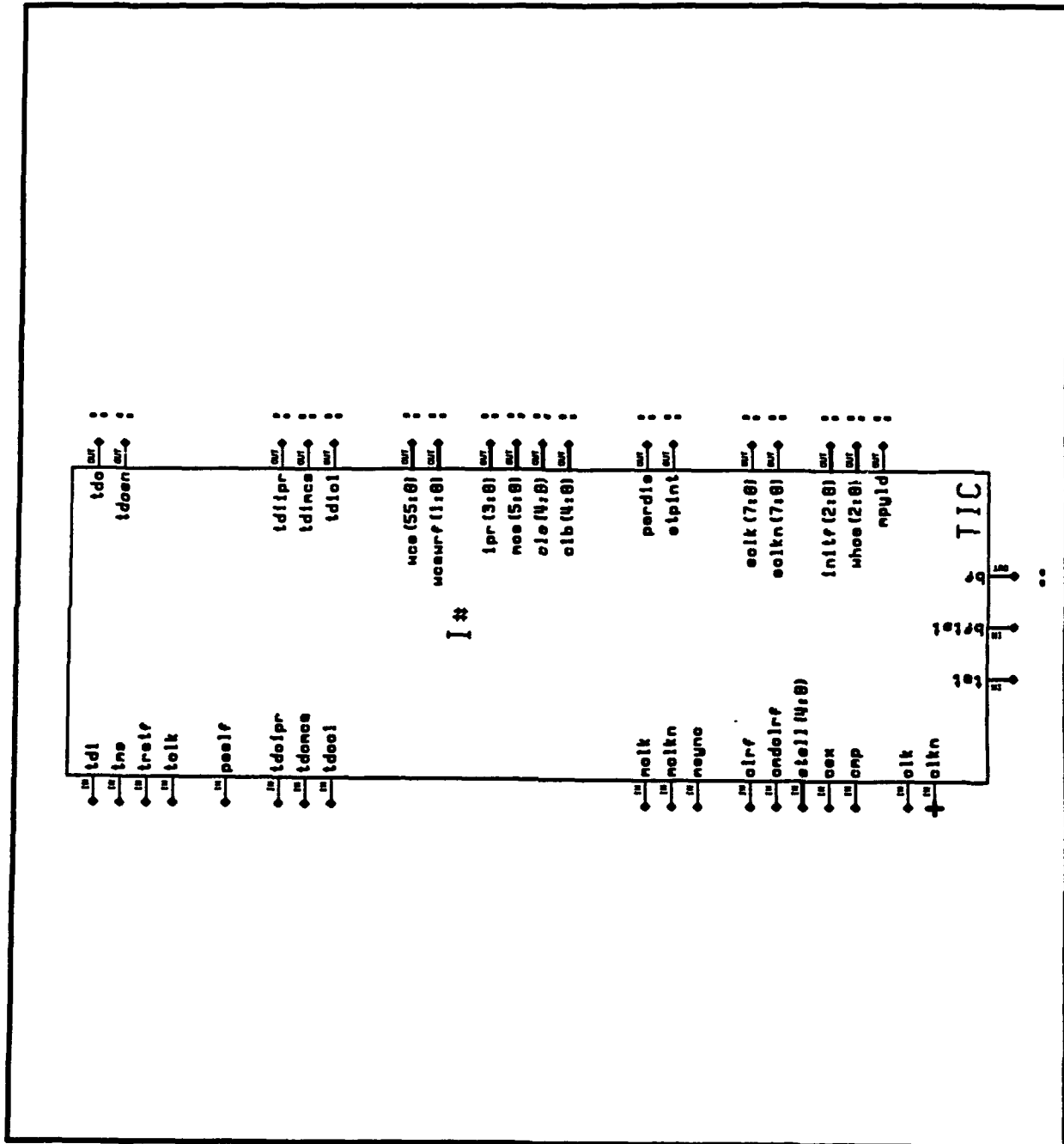




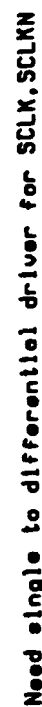




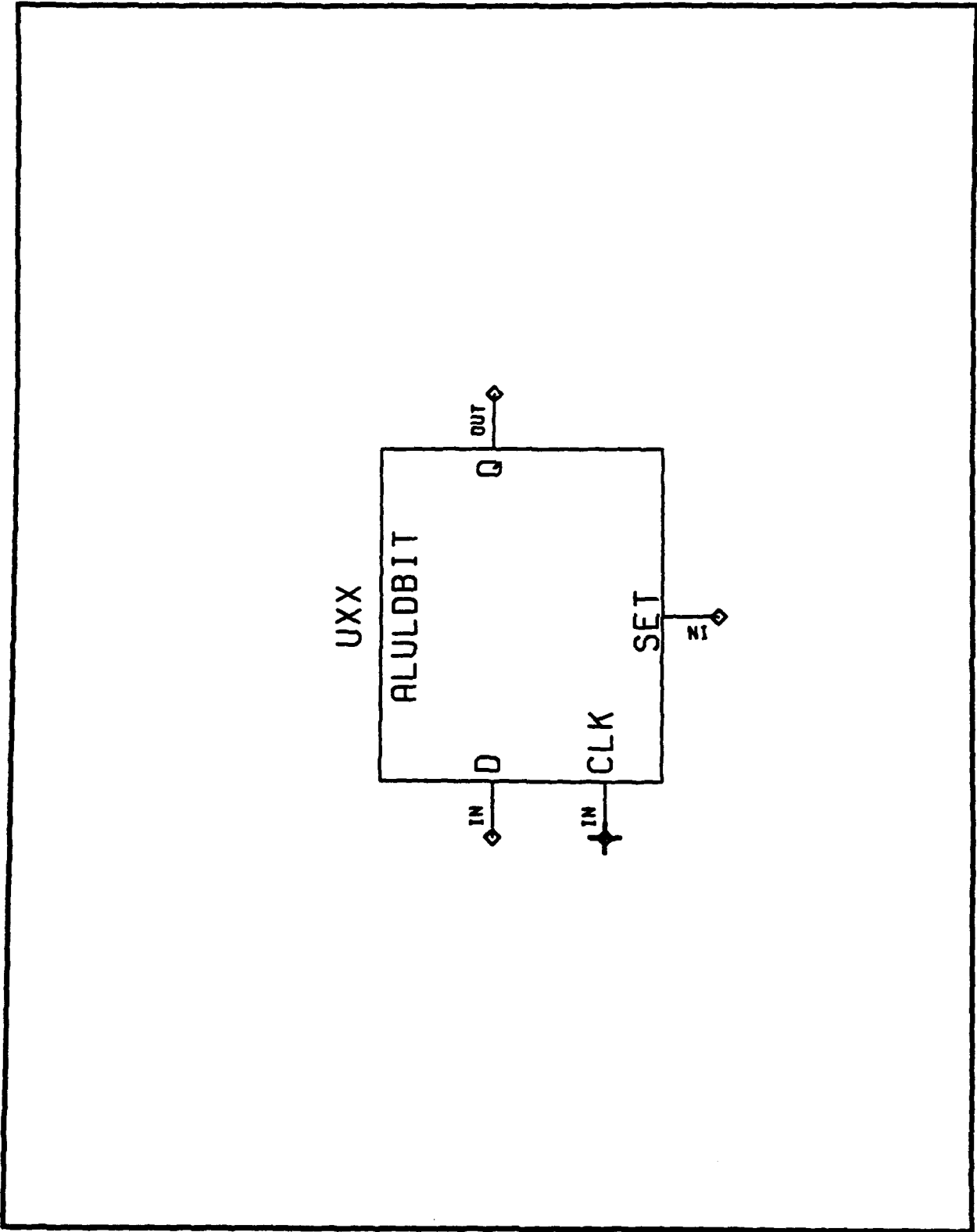
YREG



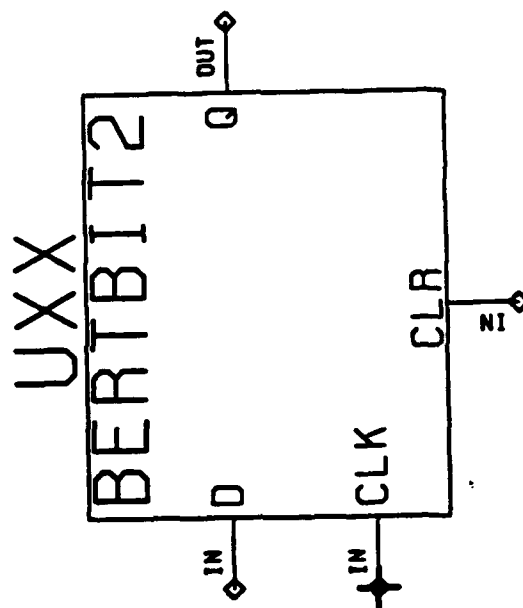




TIC: Sheet 2 of 2

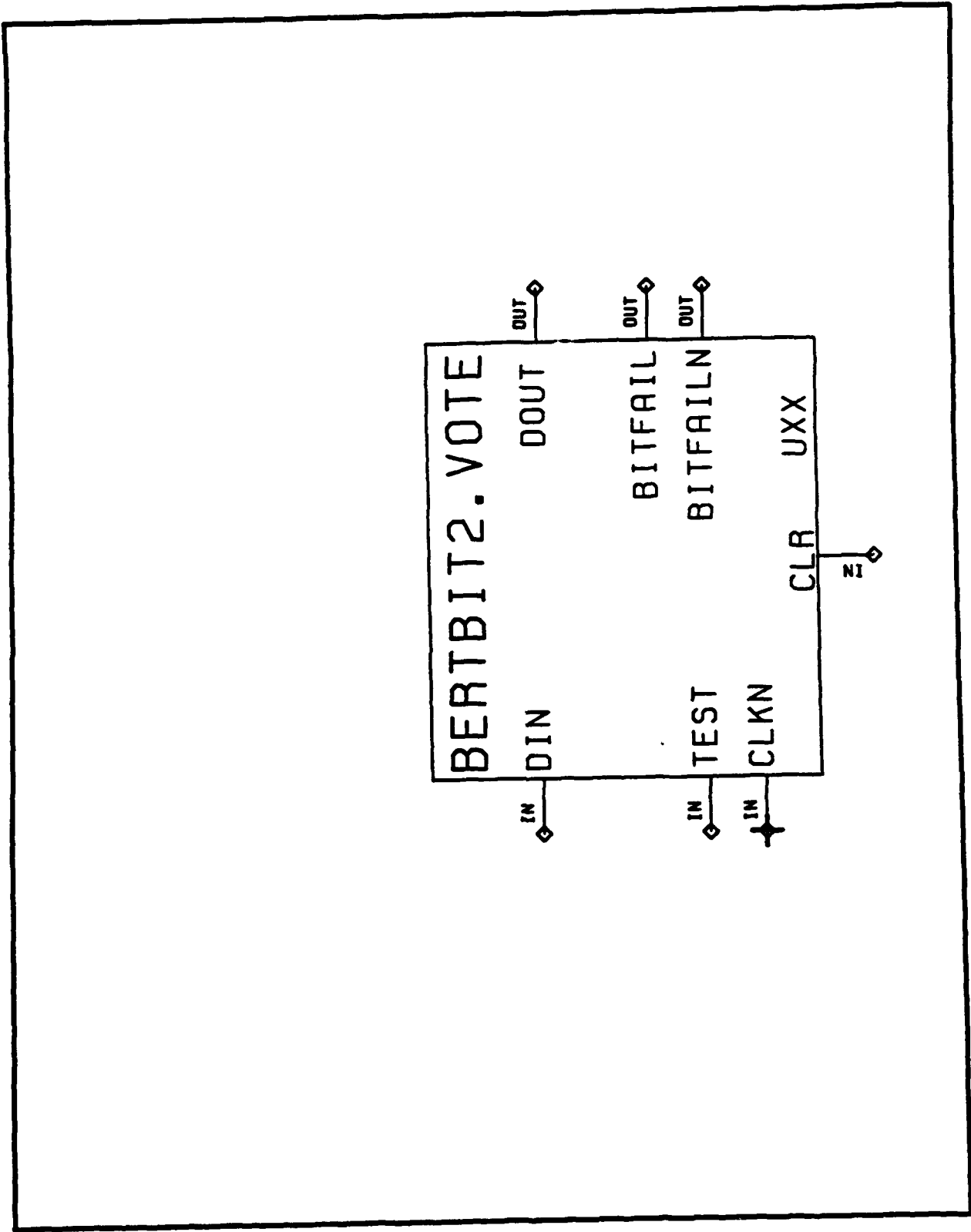




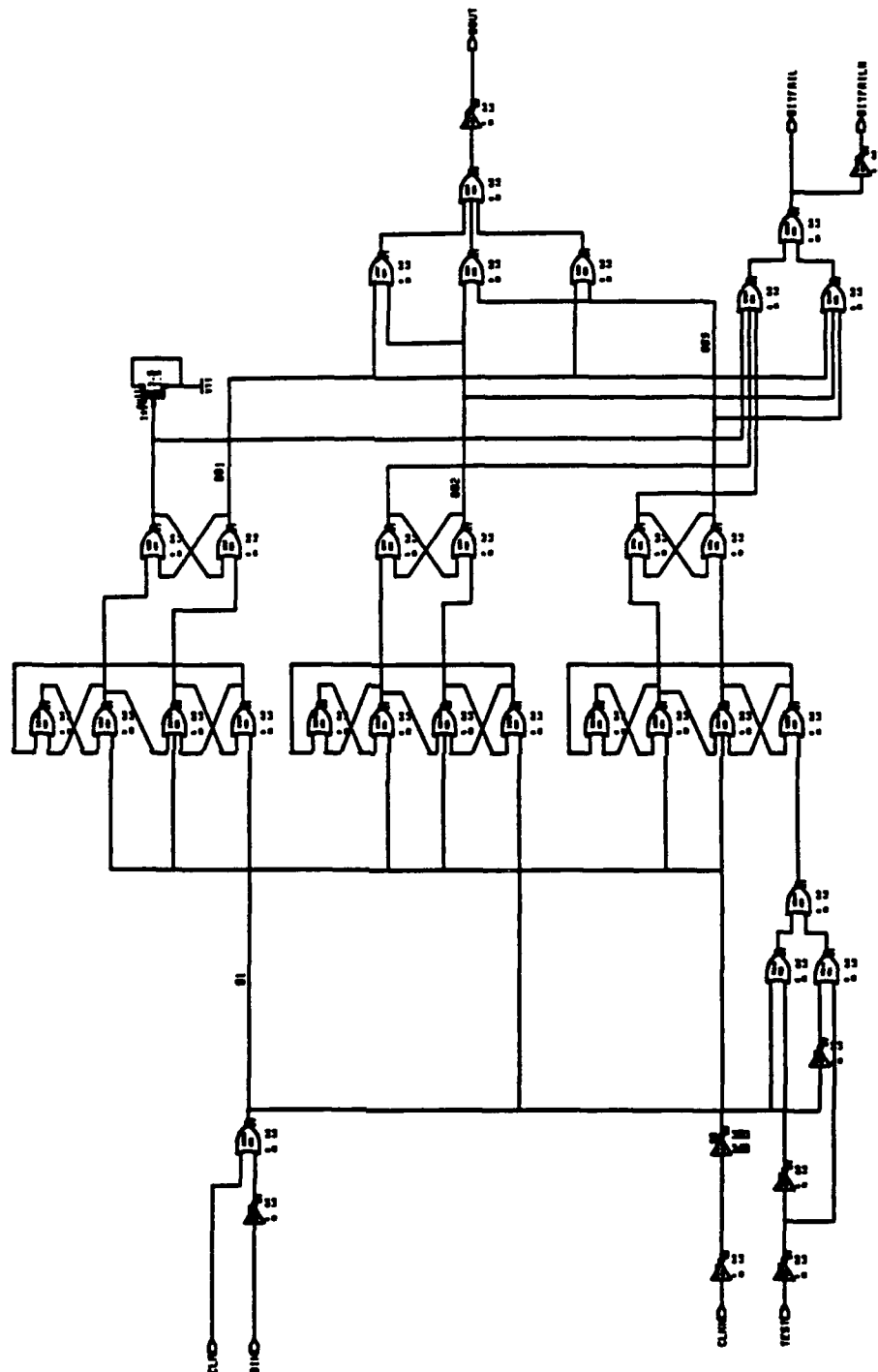


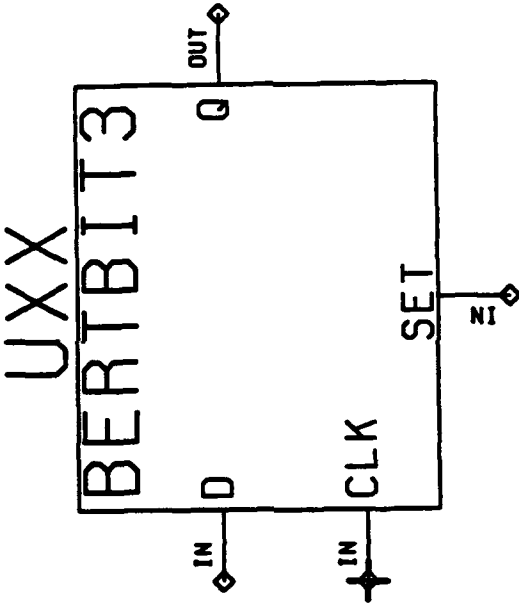


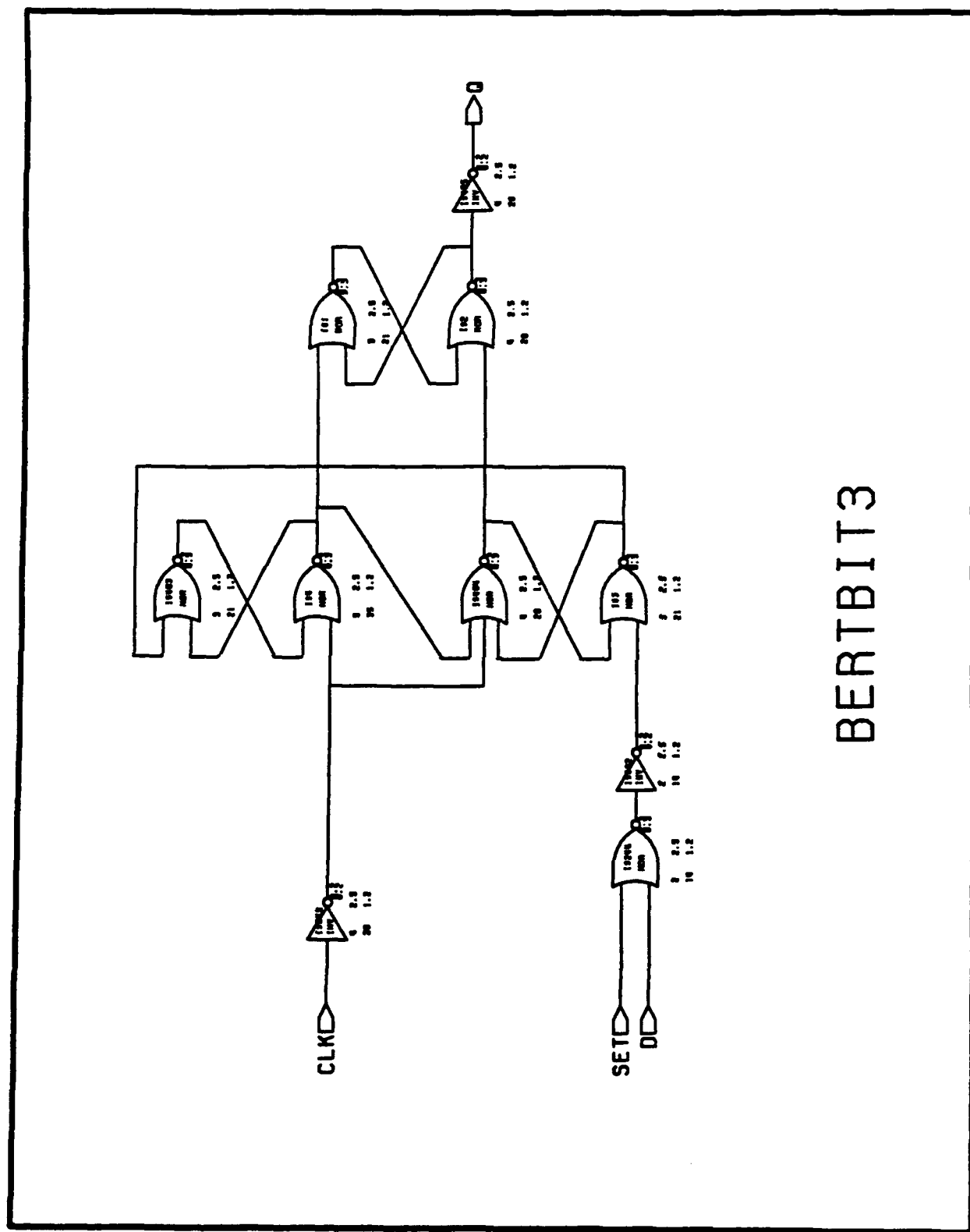


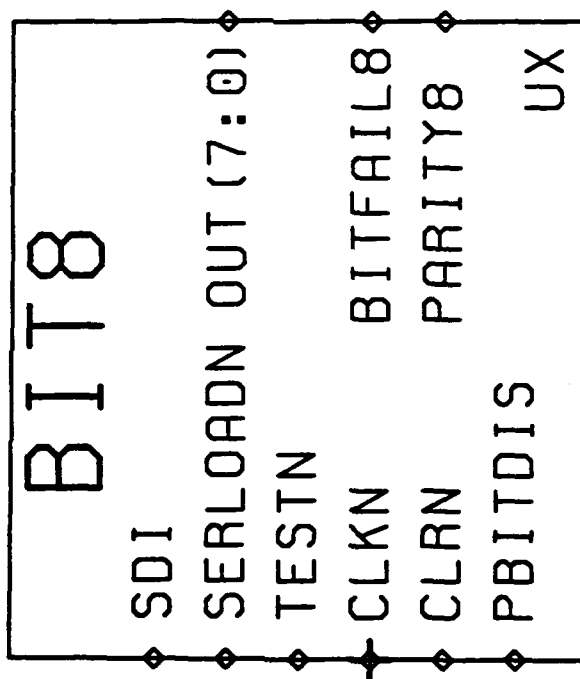


# BERTBIT2.VOTE

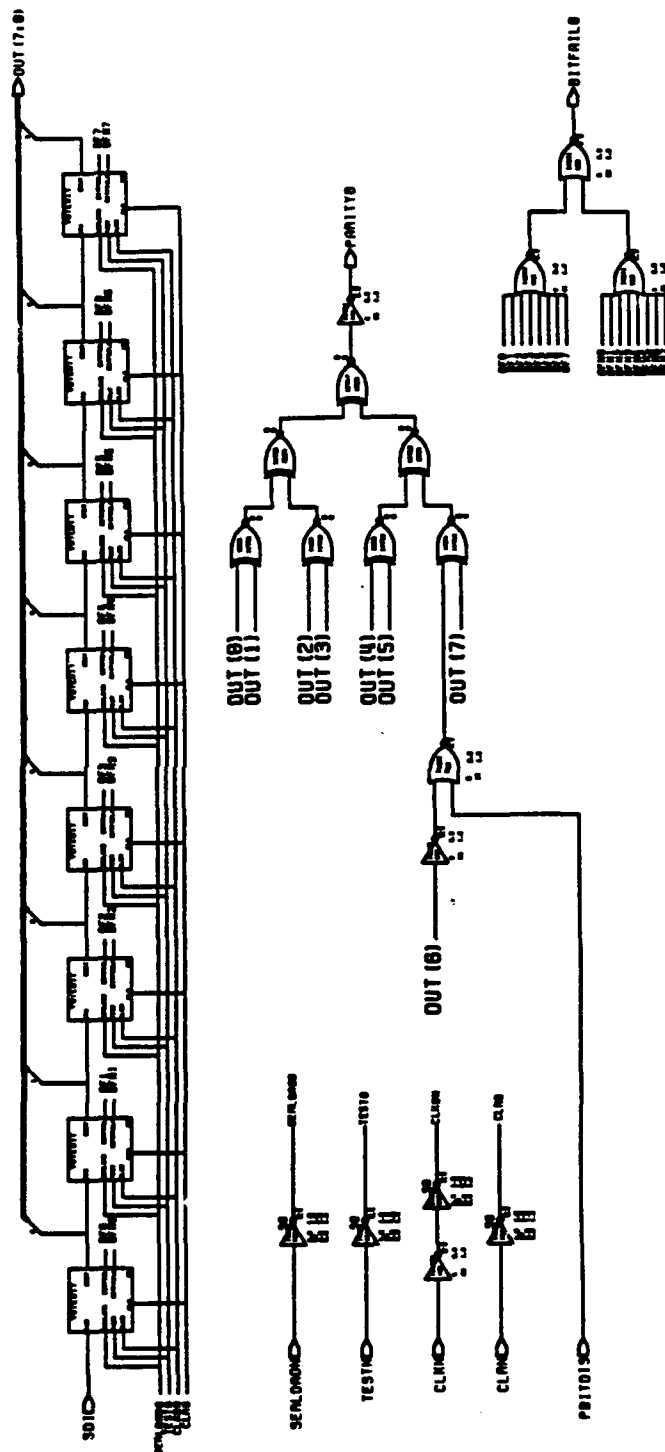


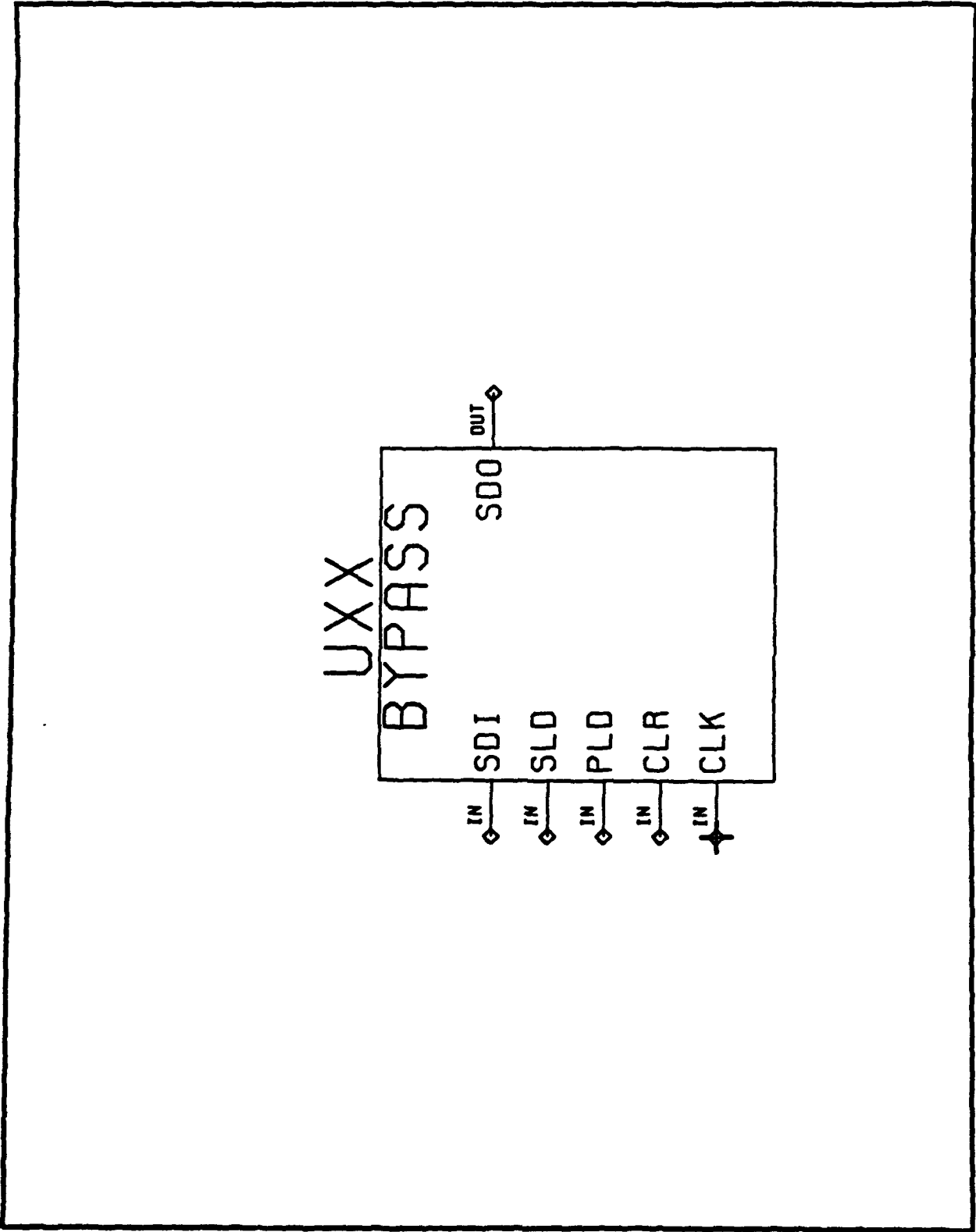


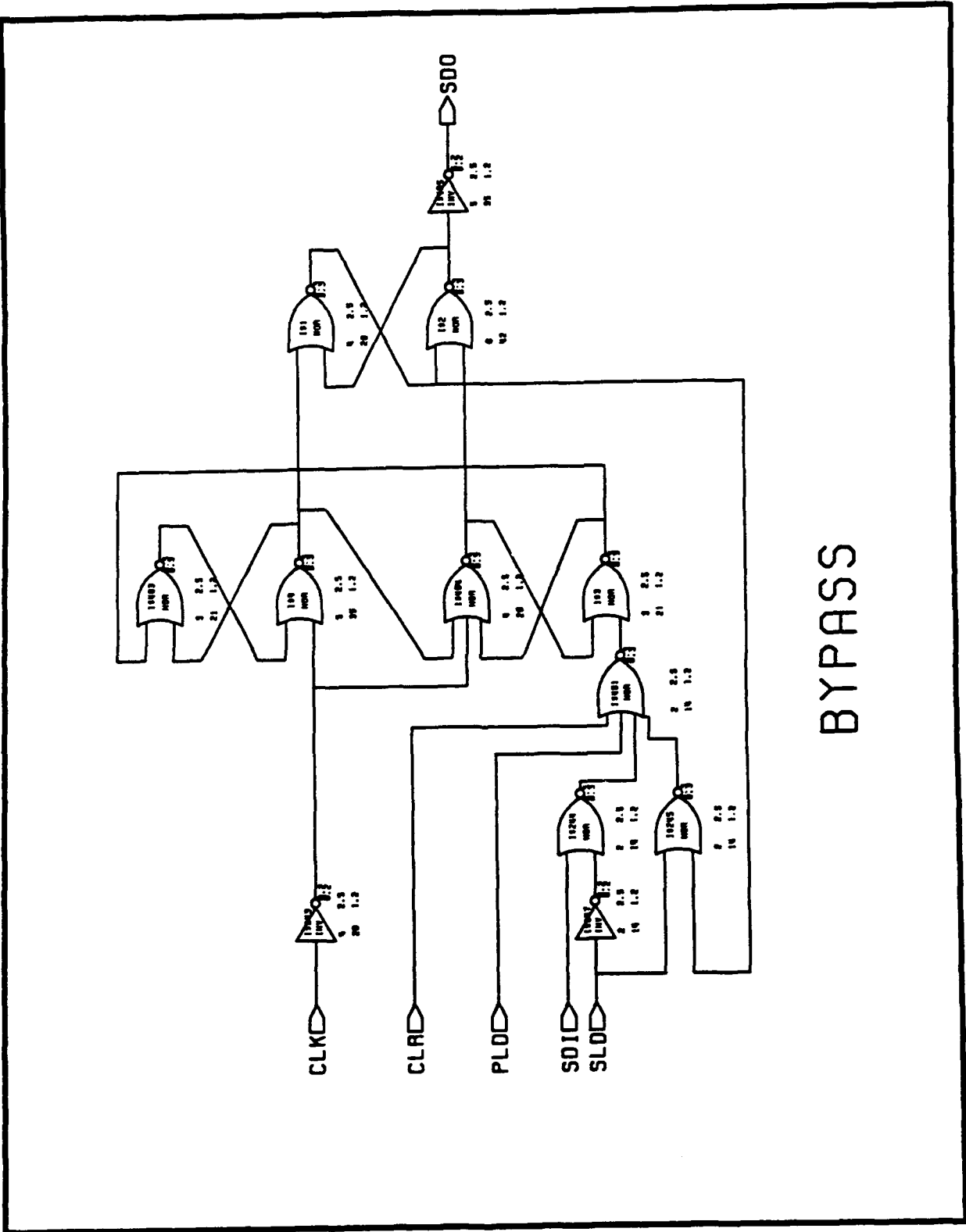




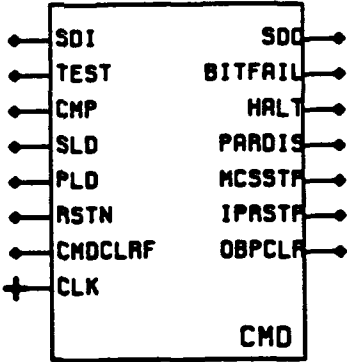
# BIT8

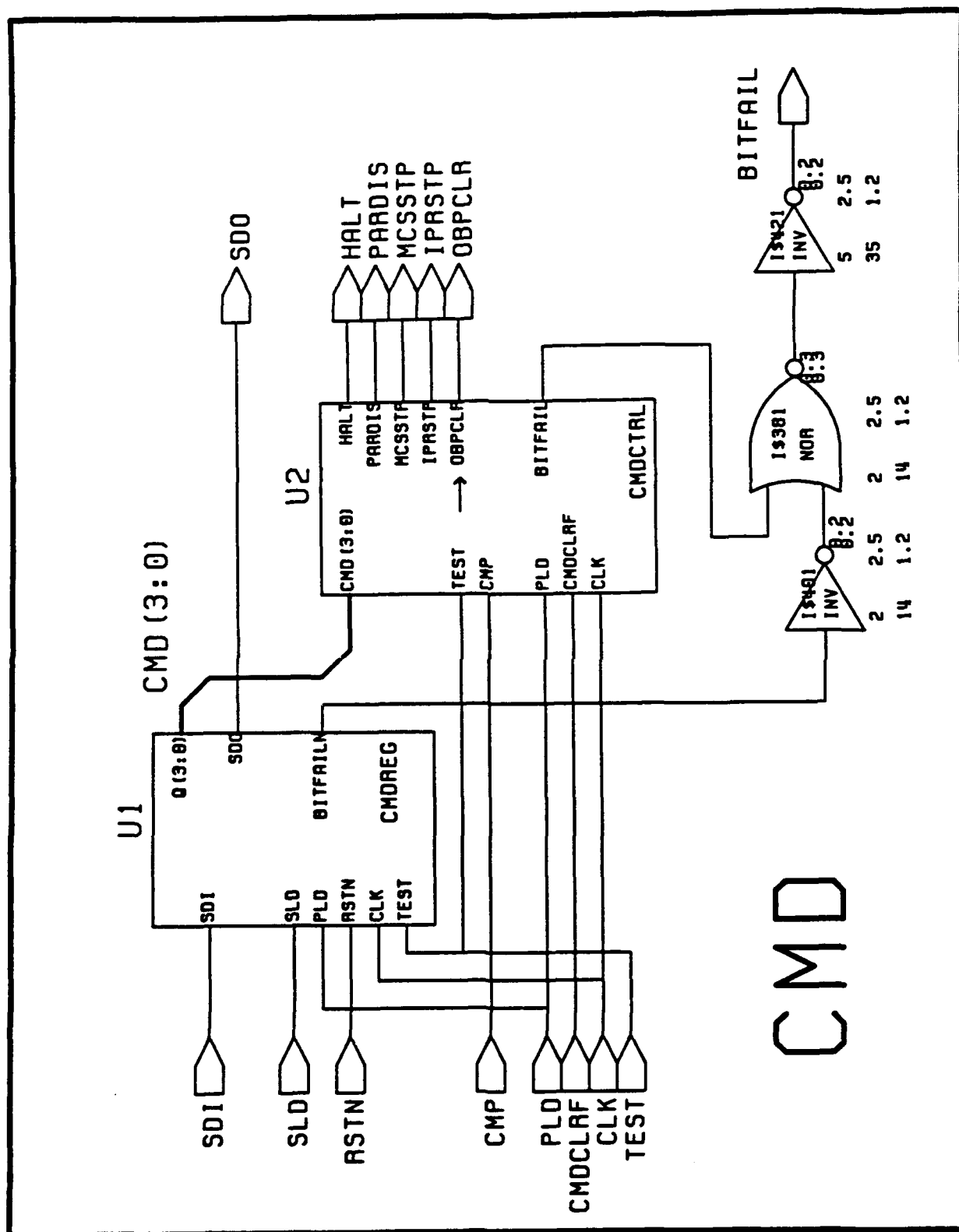


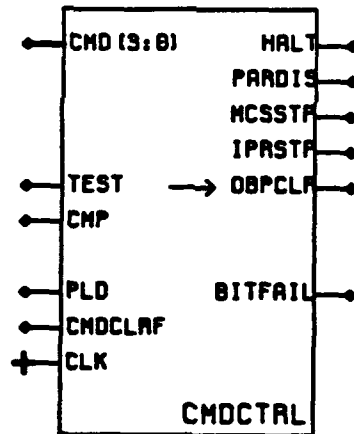




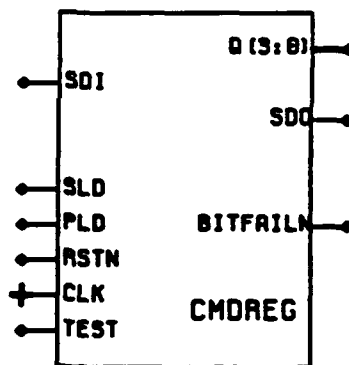


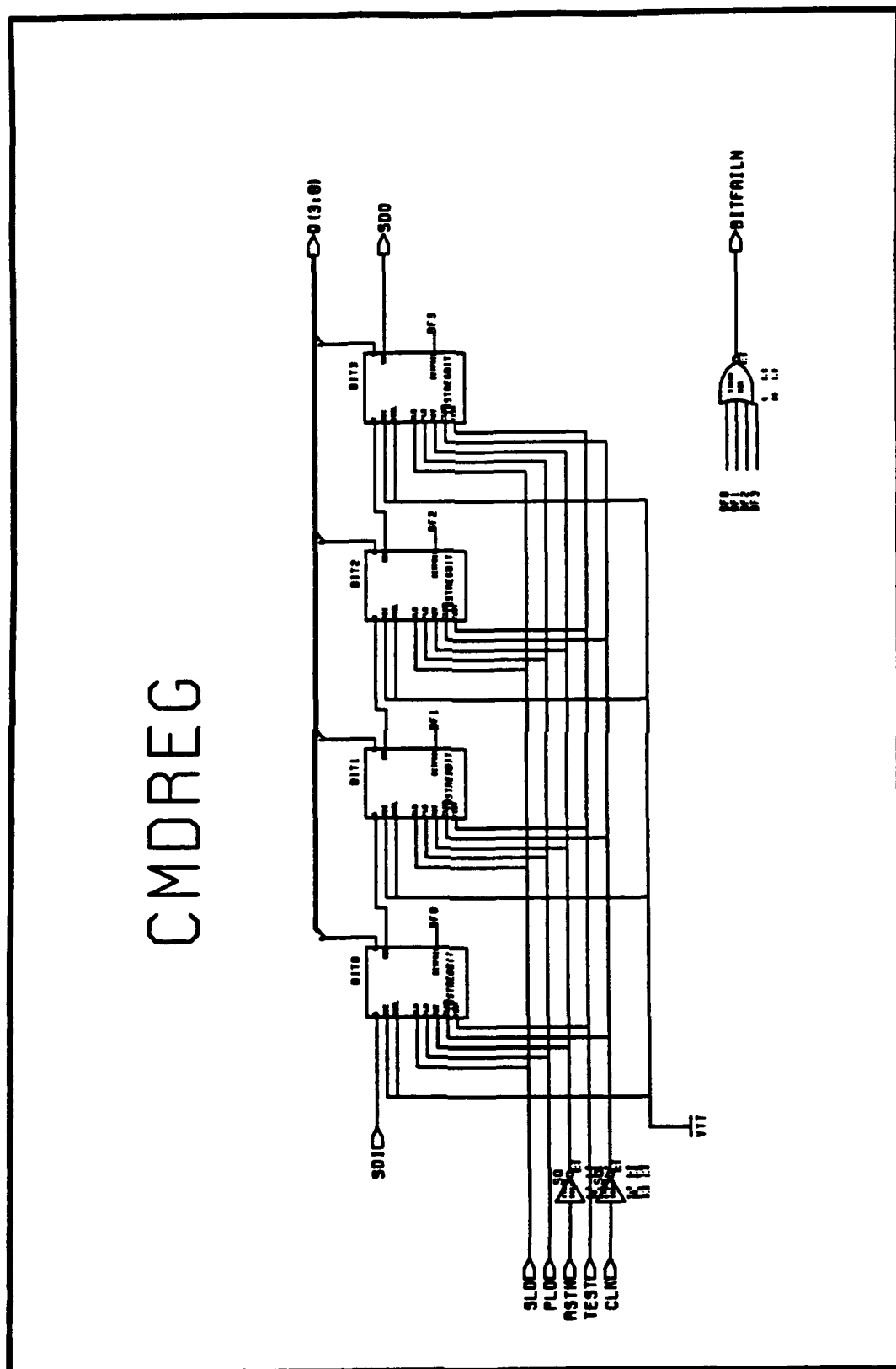










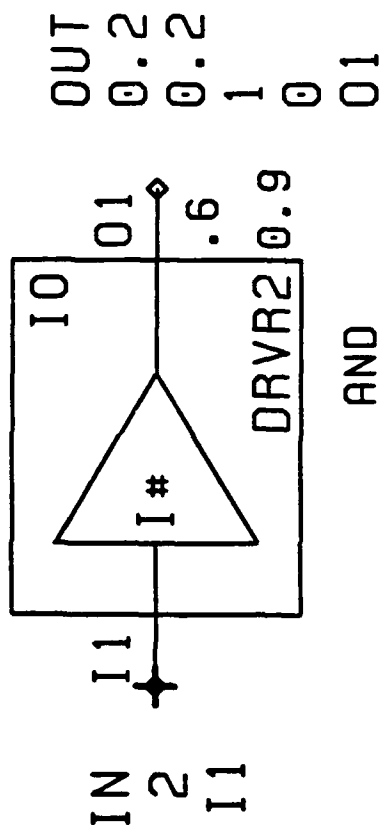


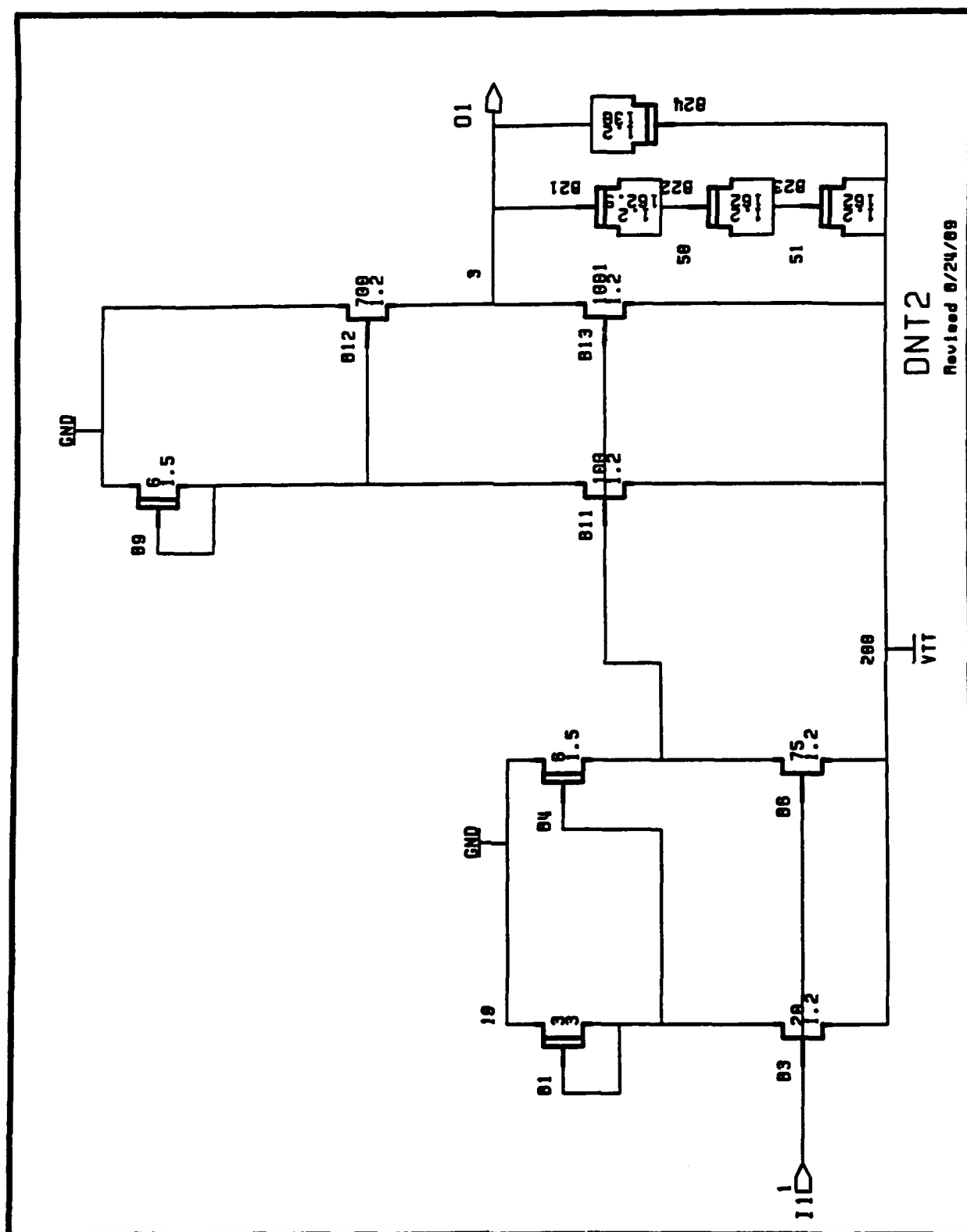
# VITESSE GAAS CELL LIBRARY

Version 0.8

NAME: DRV2

DESCRIPTION: LOW POWER 2 VOLT DRIVER WITH PAD







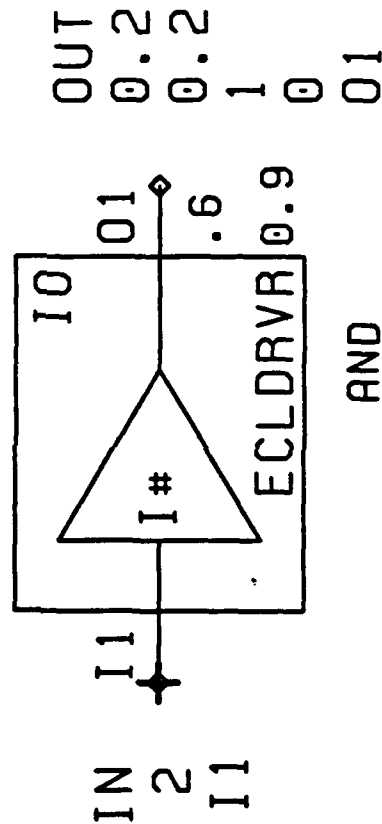
# VITESSE GAAS CELL LIBRARY

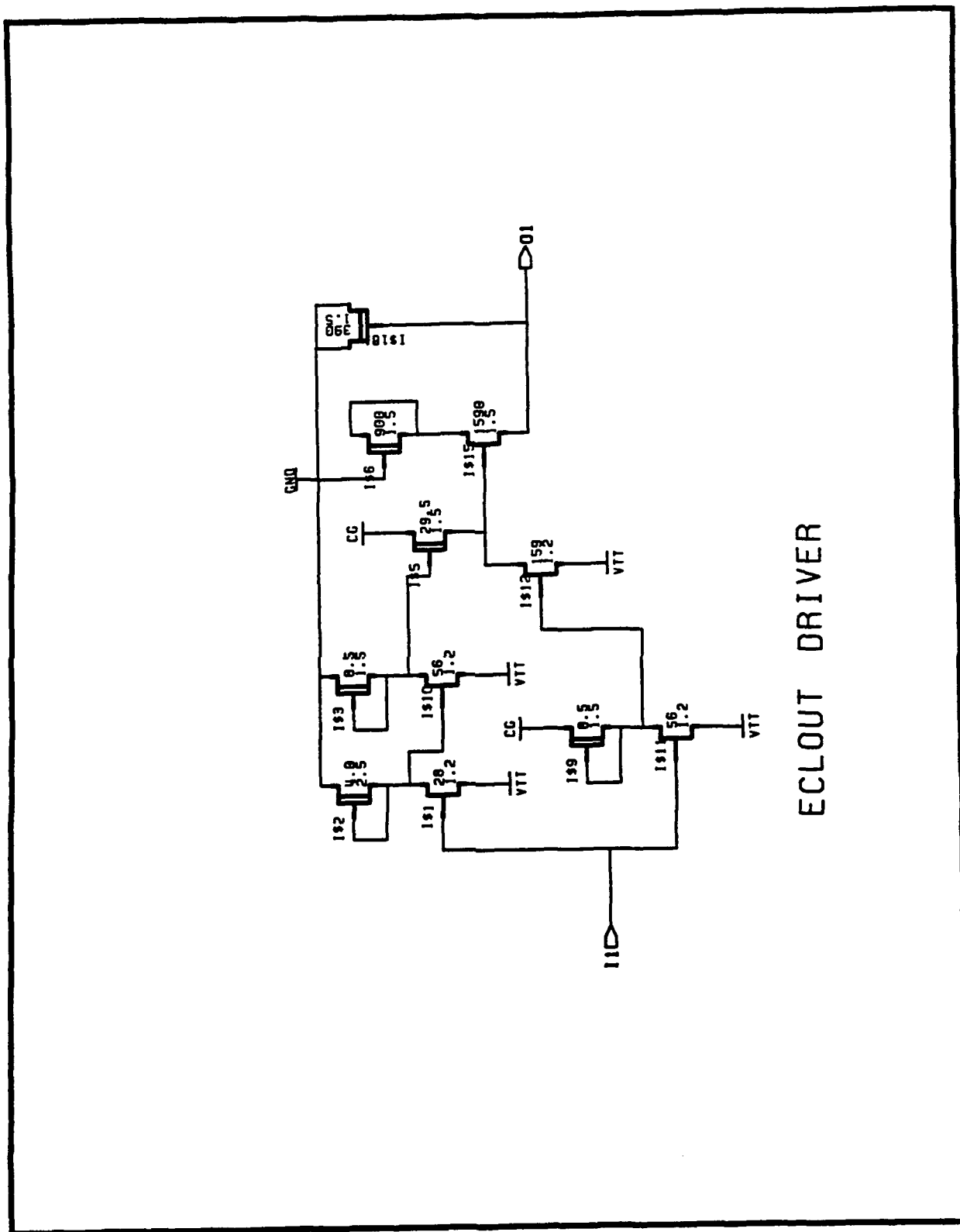
Version 0.8

NAME:

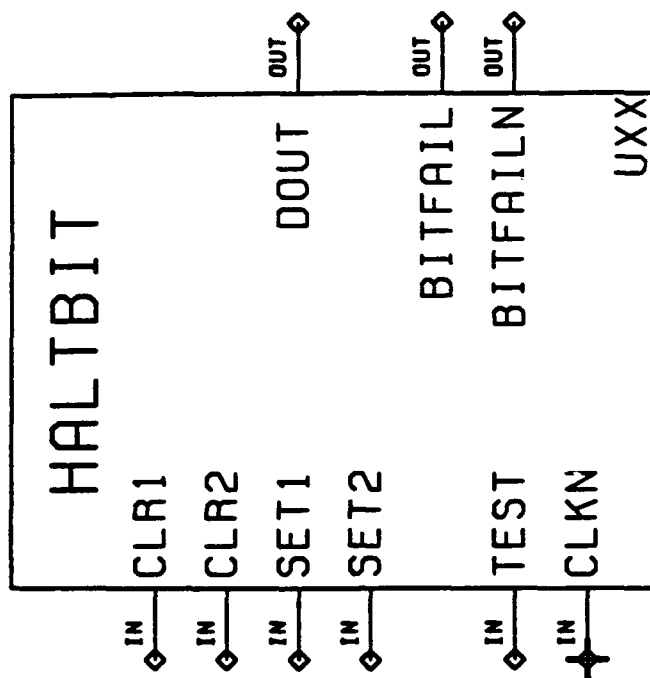
ECLOUT

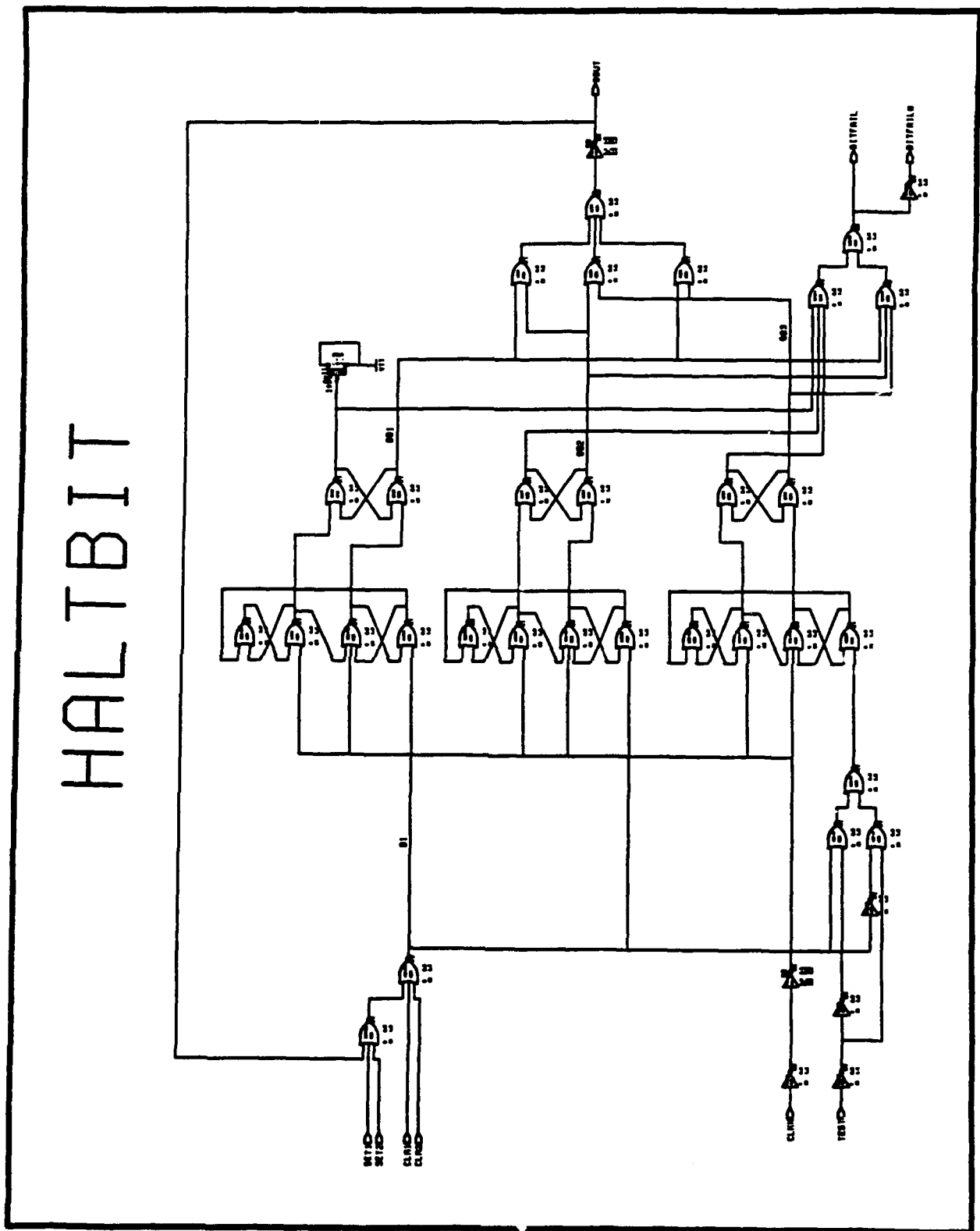
DESCRIPTION: ECL OUTPUT DRVR FOR DMC

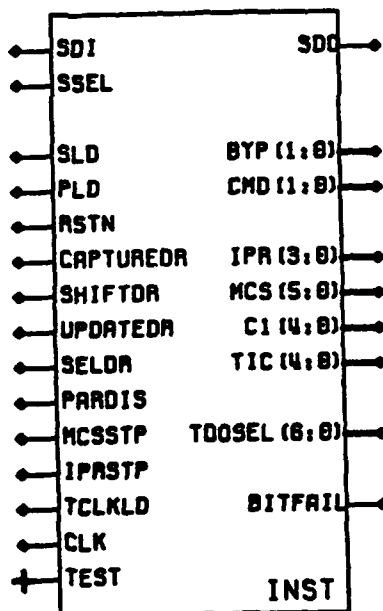


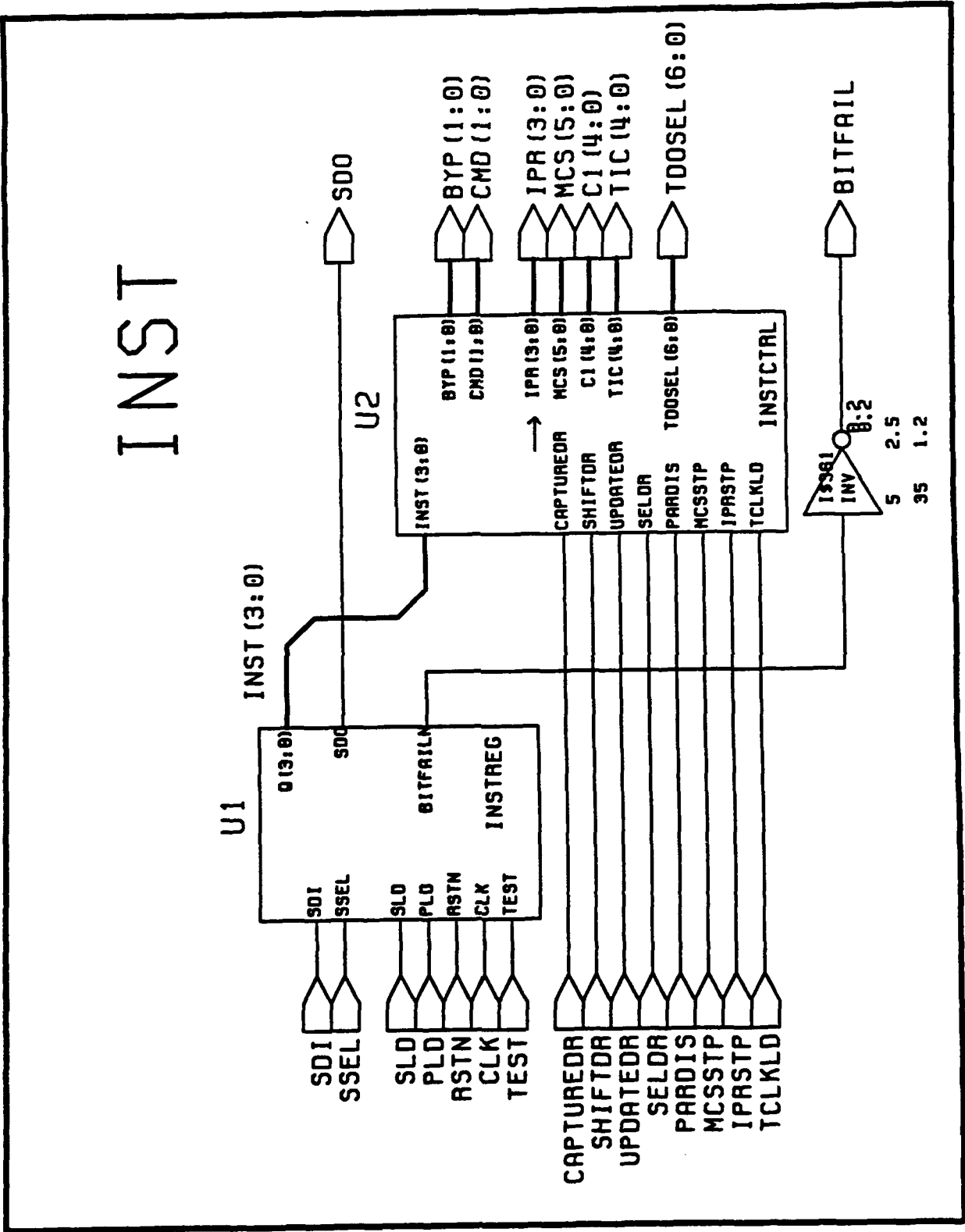


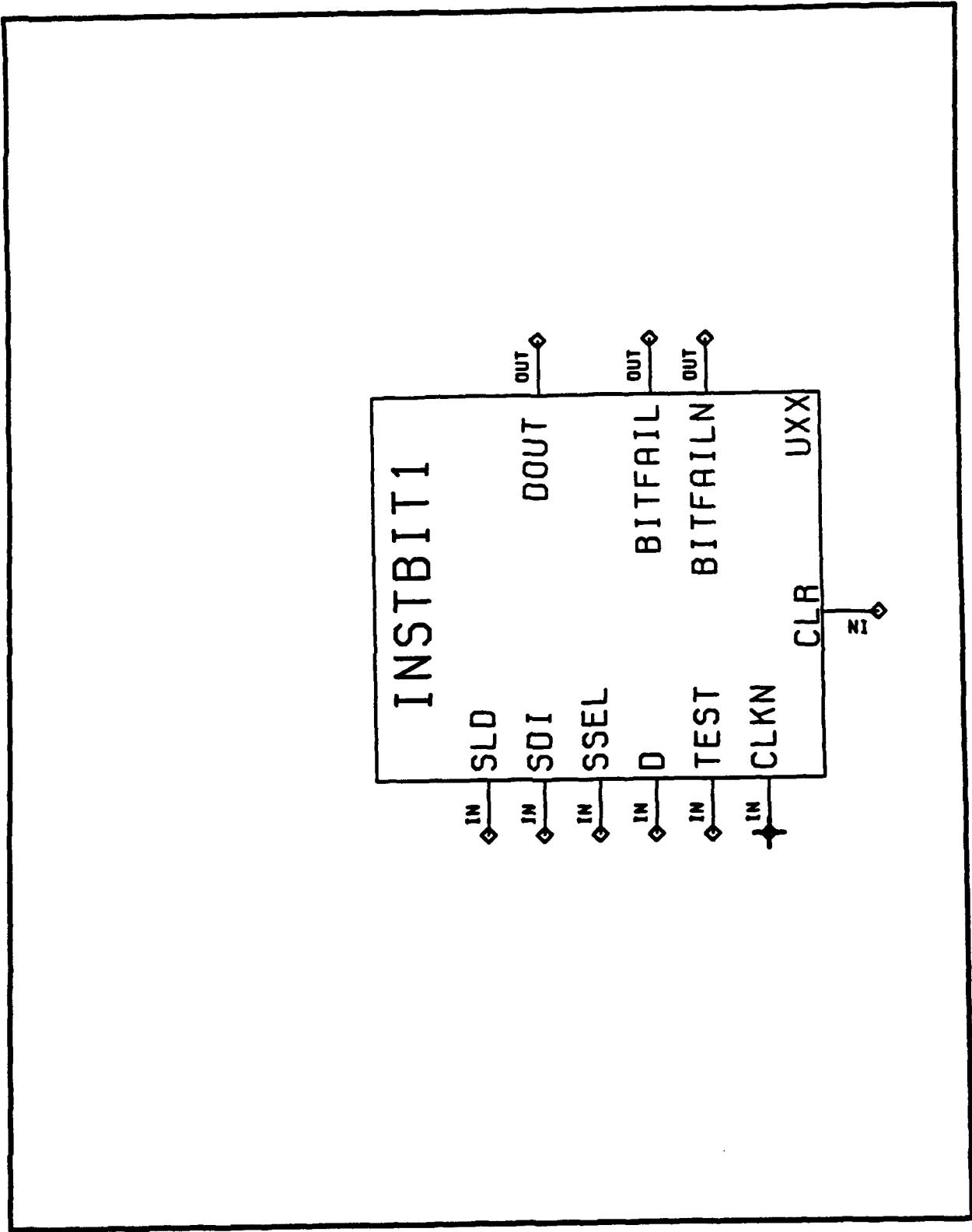
ECLOUT DRIVER

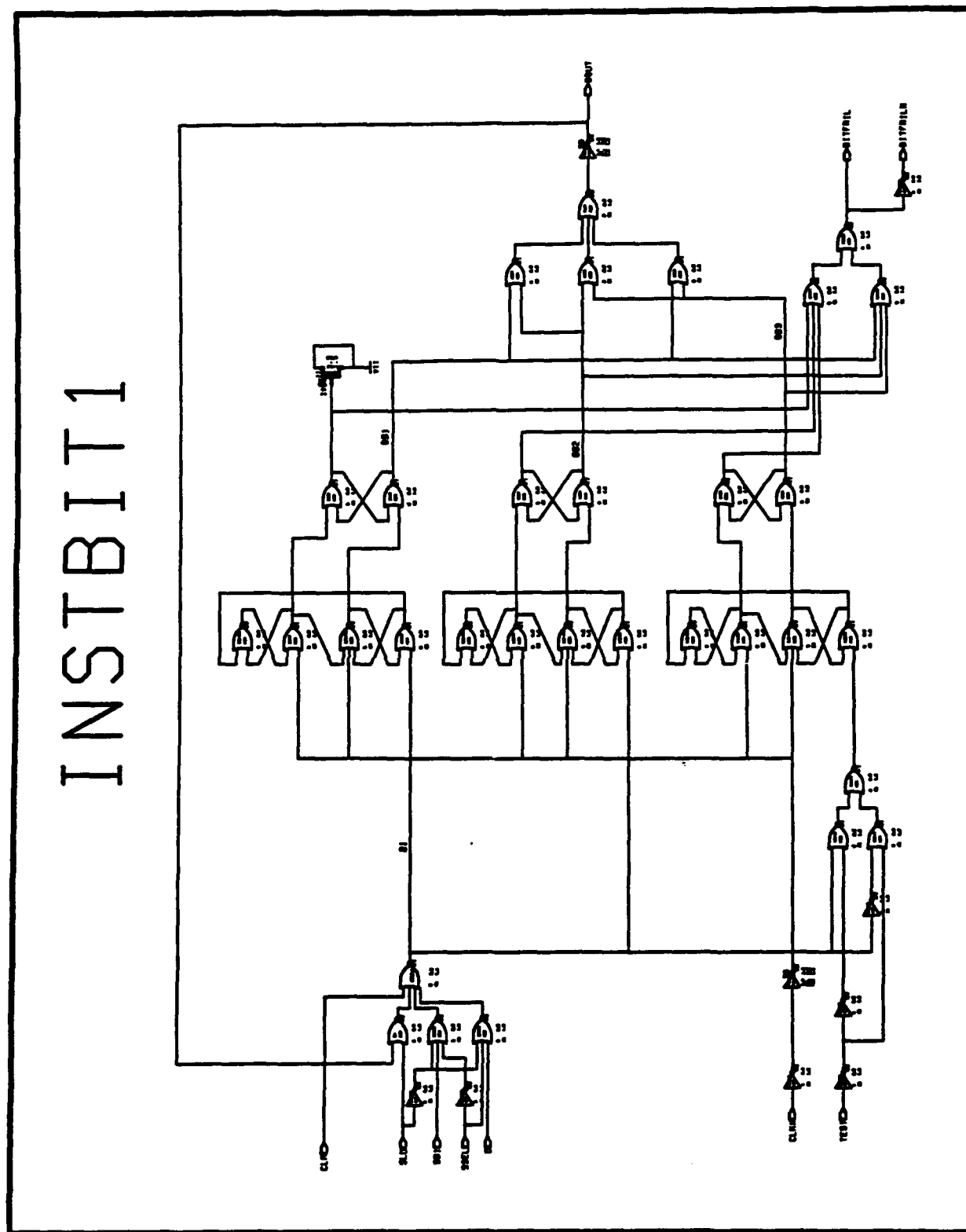




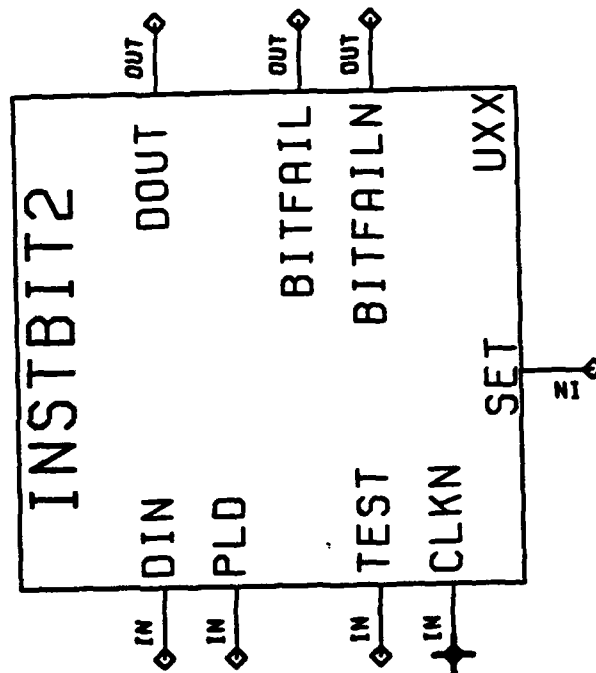


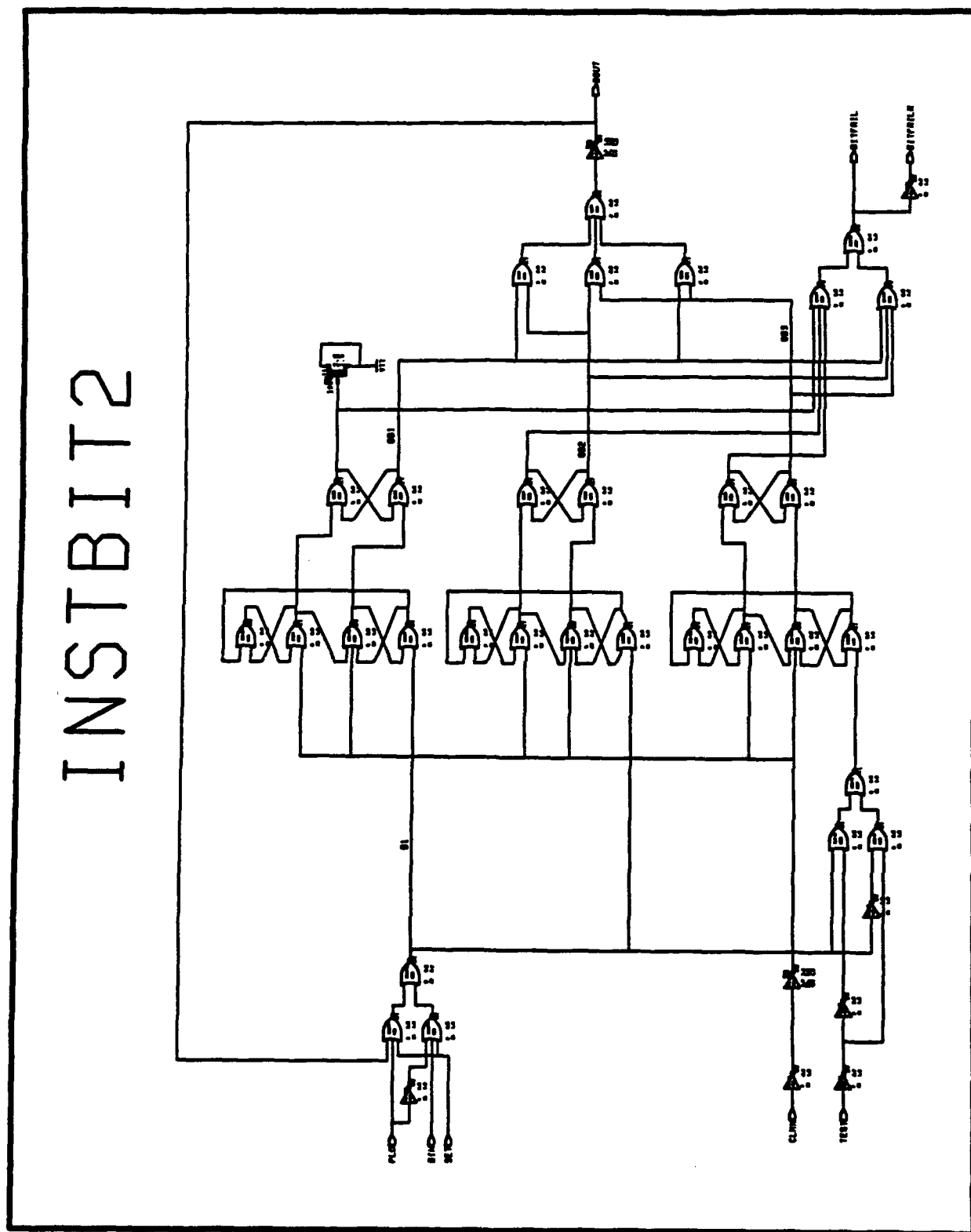


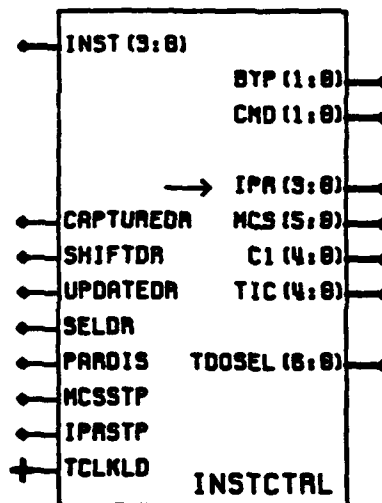




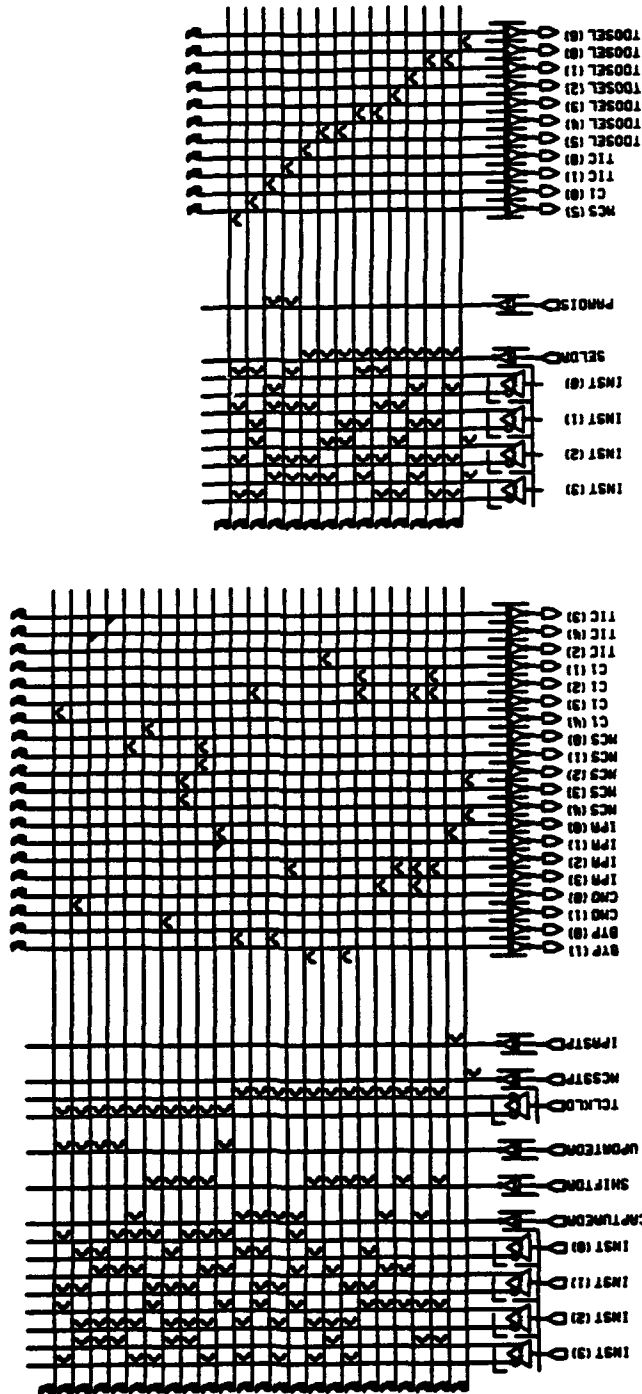


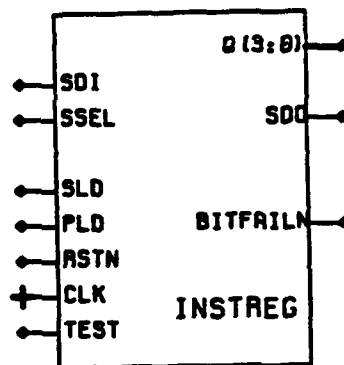


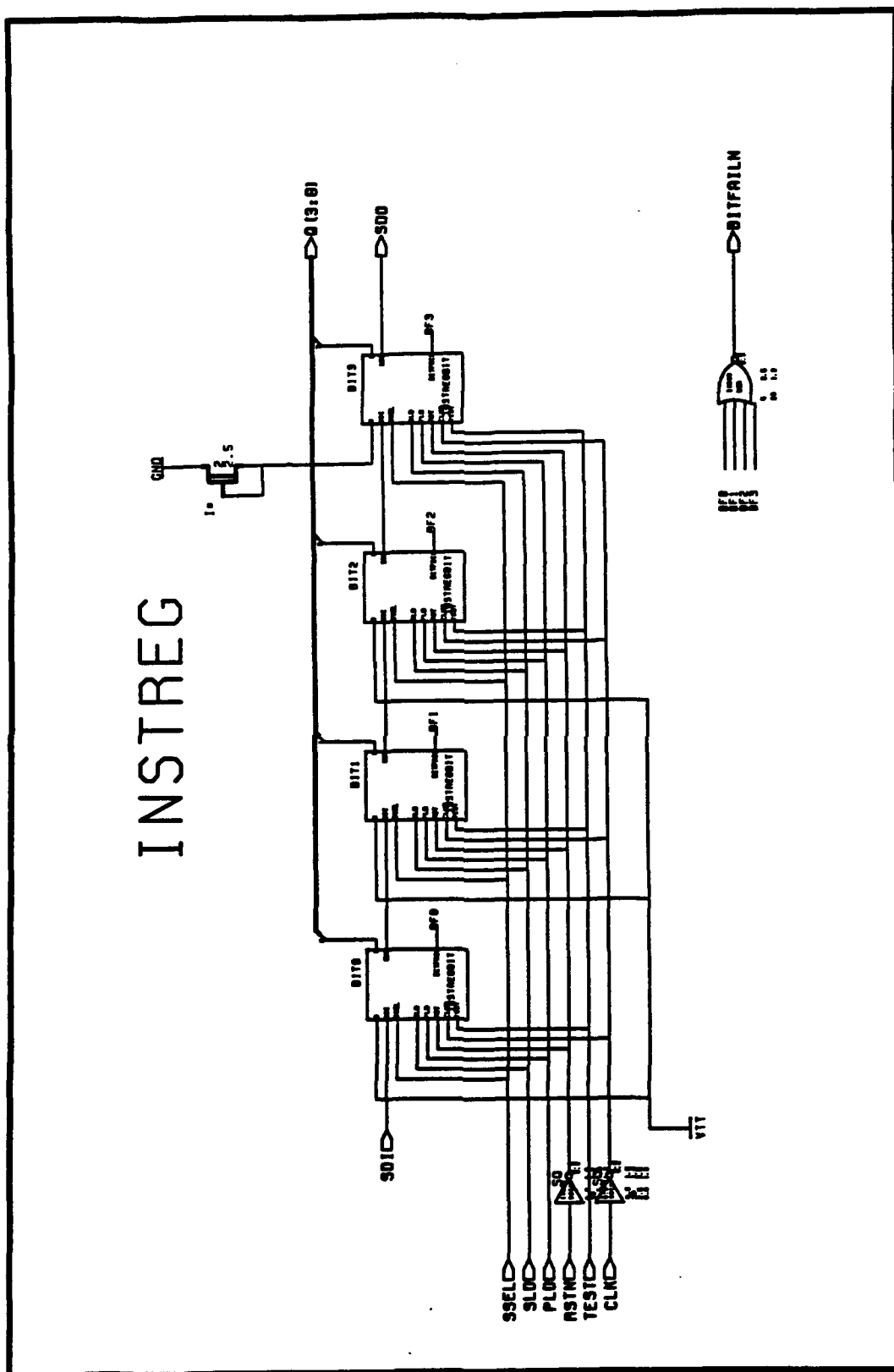


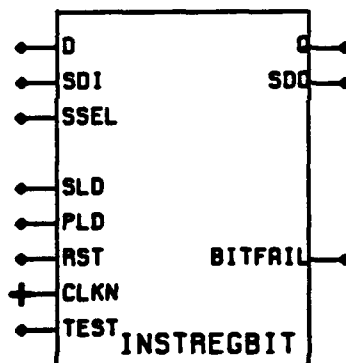


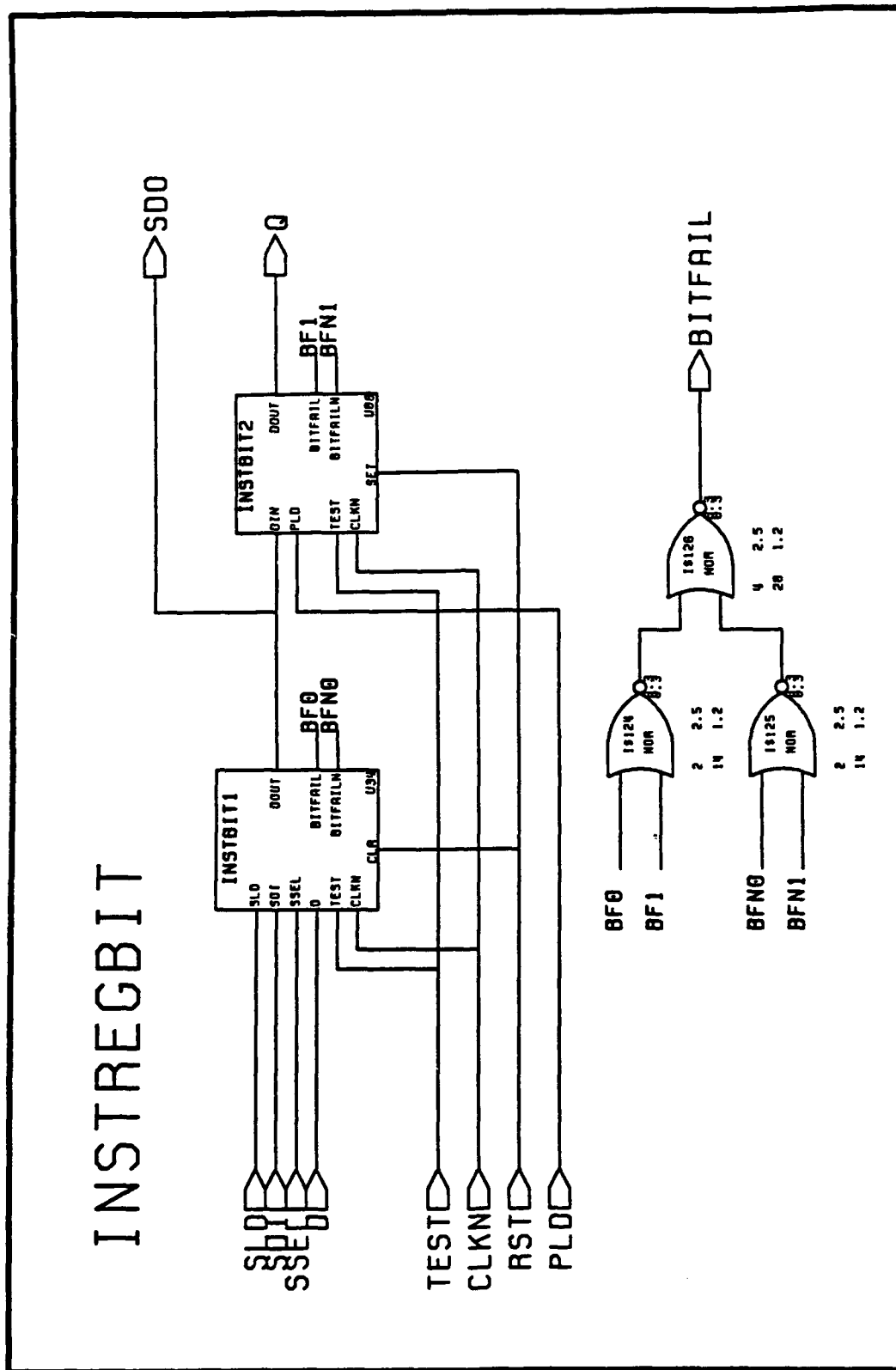
INSTCTRL



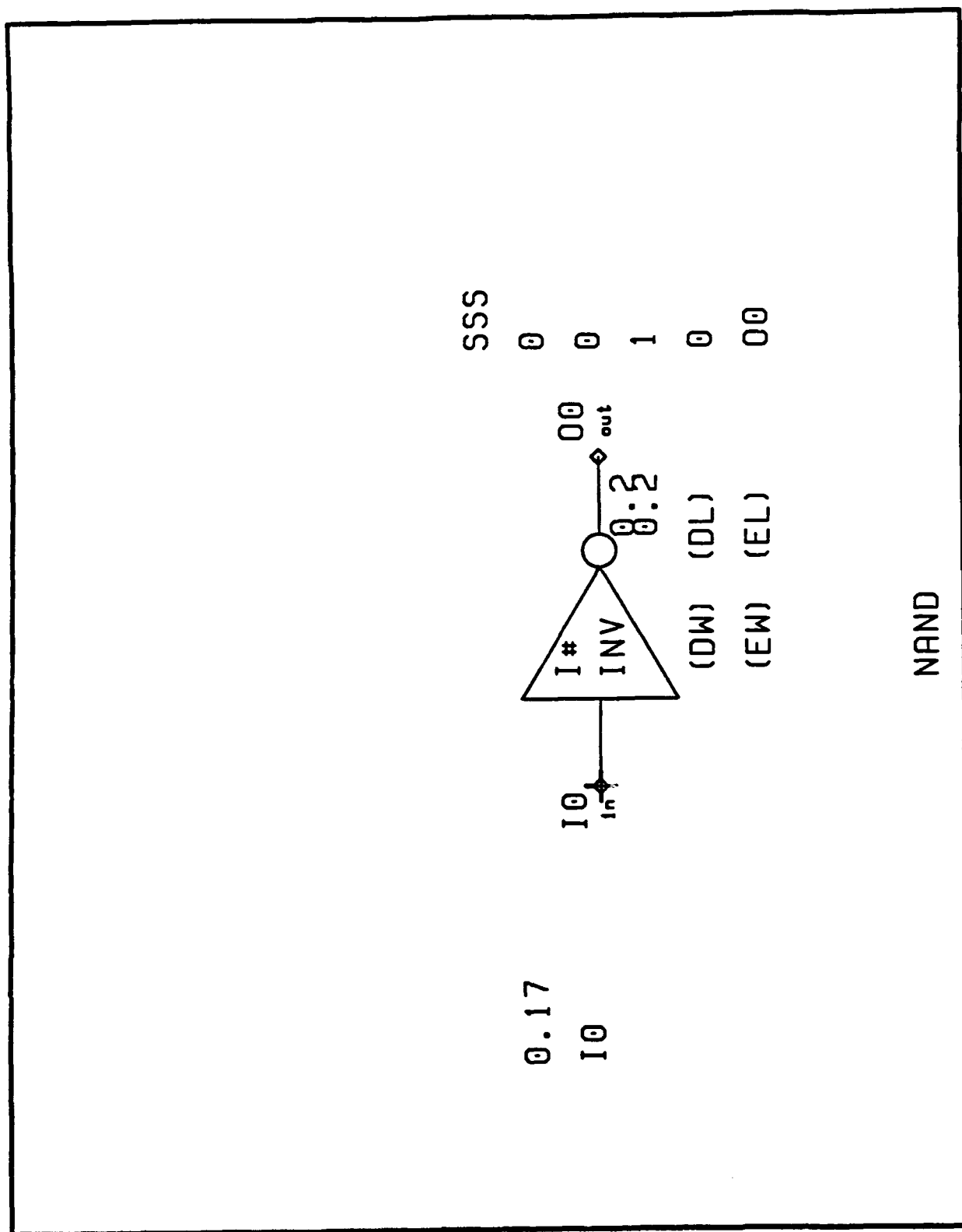


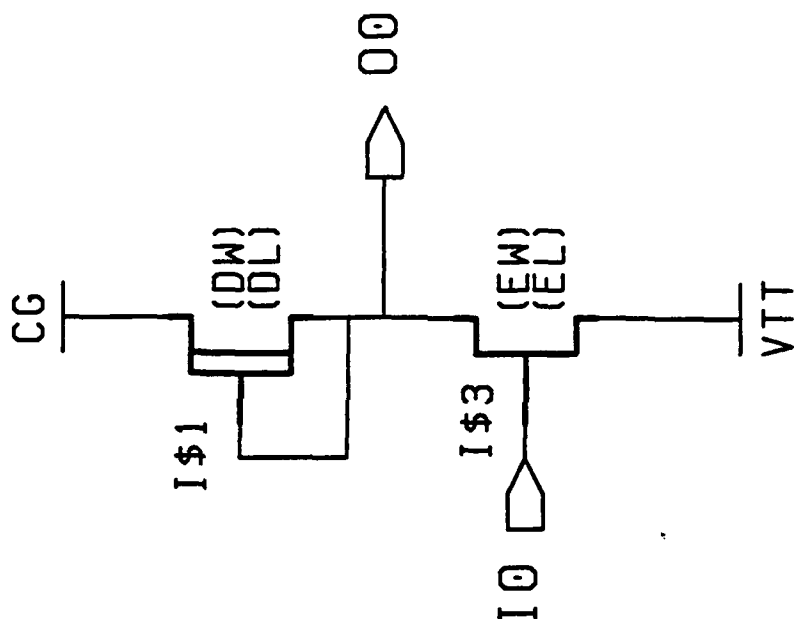


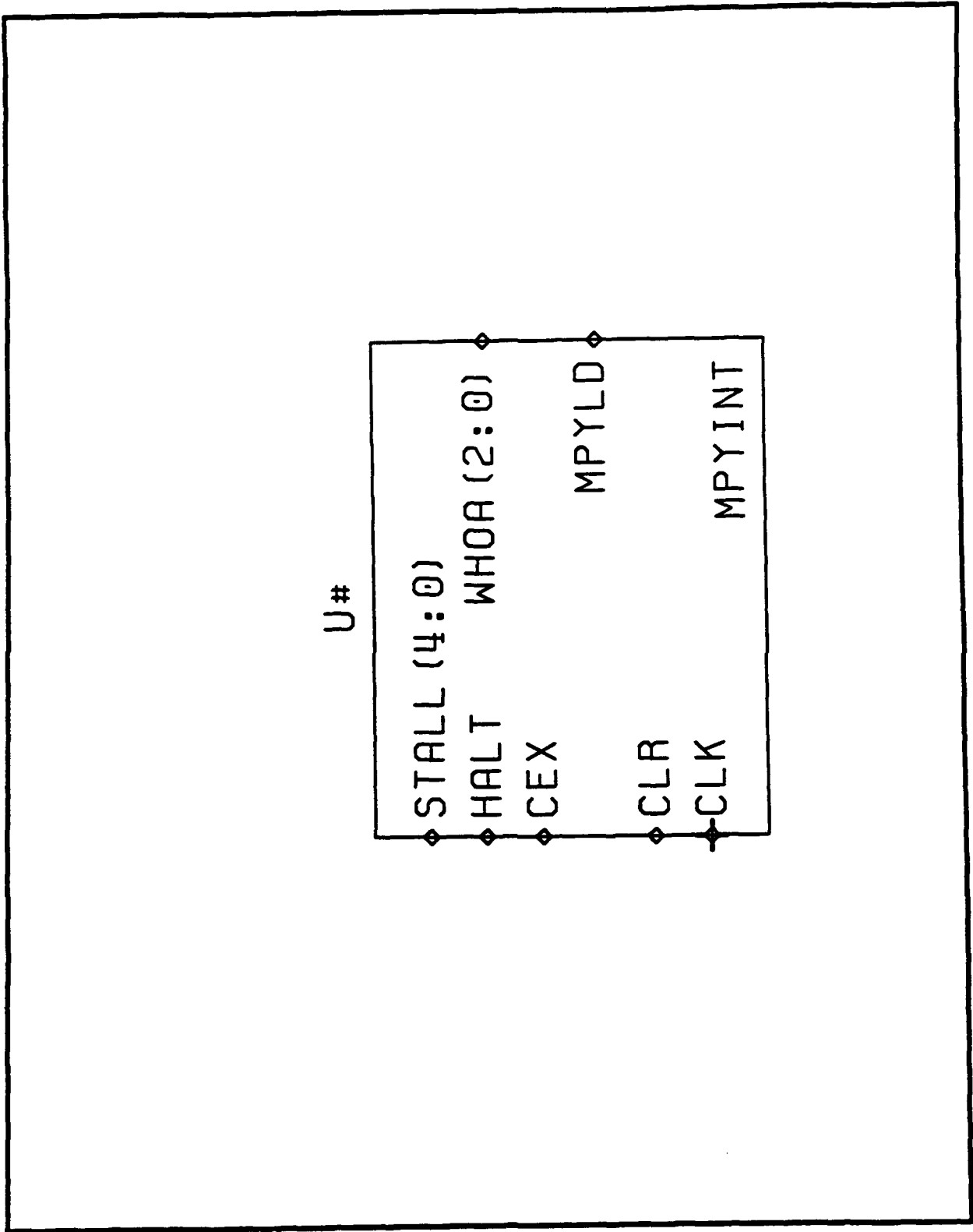


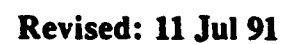


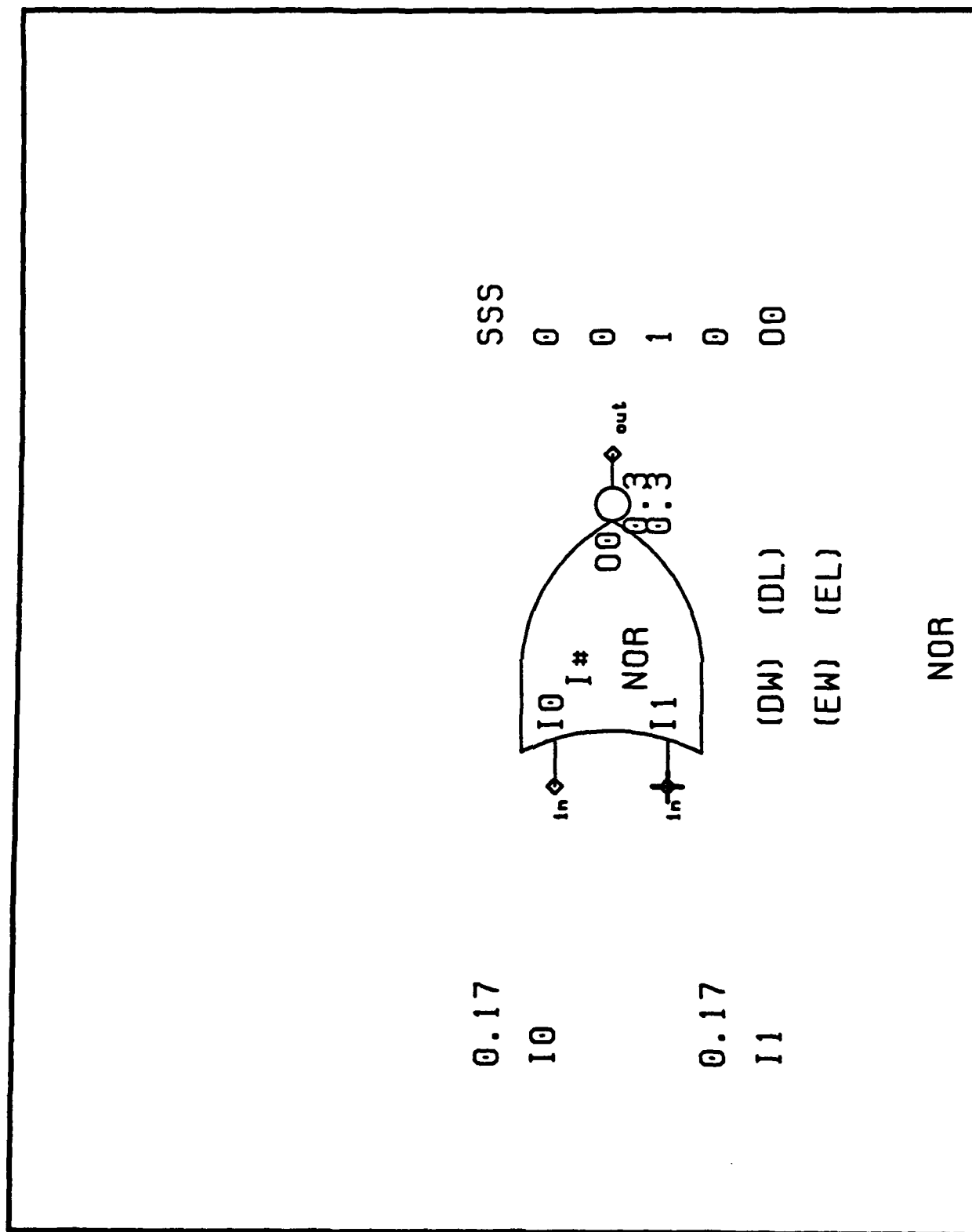


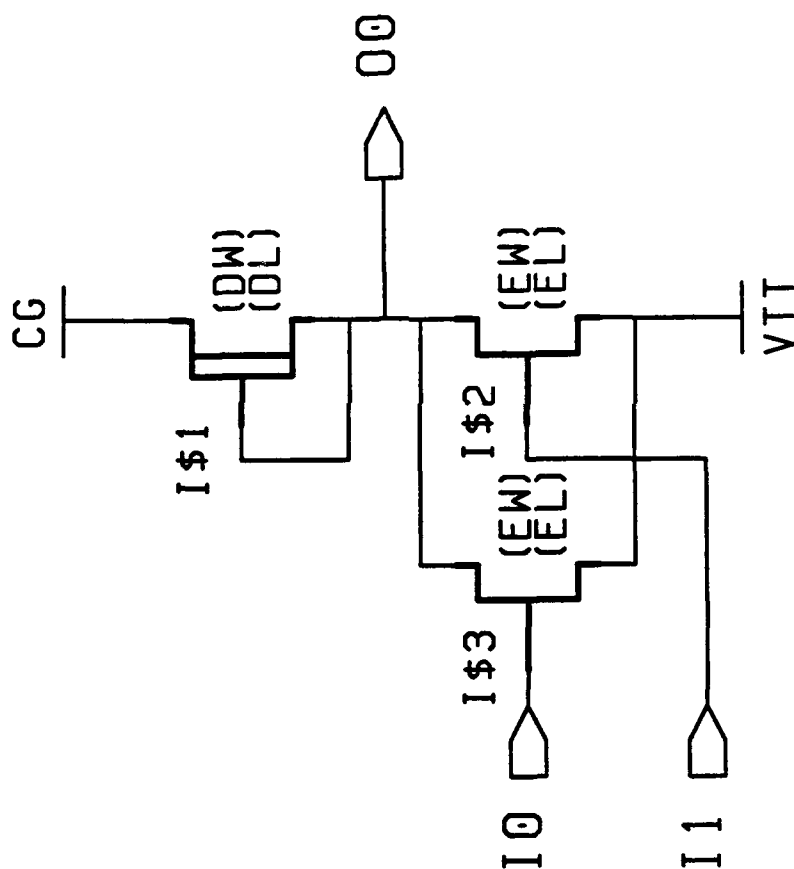


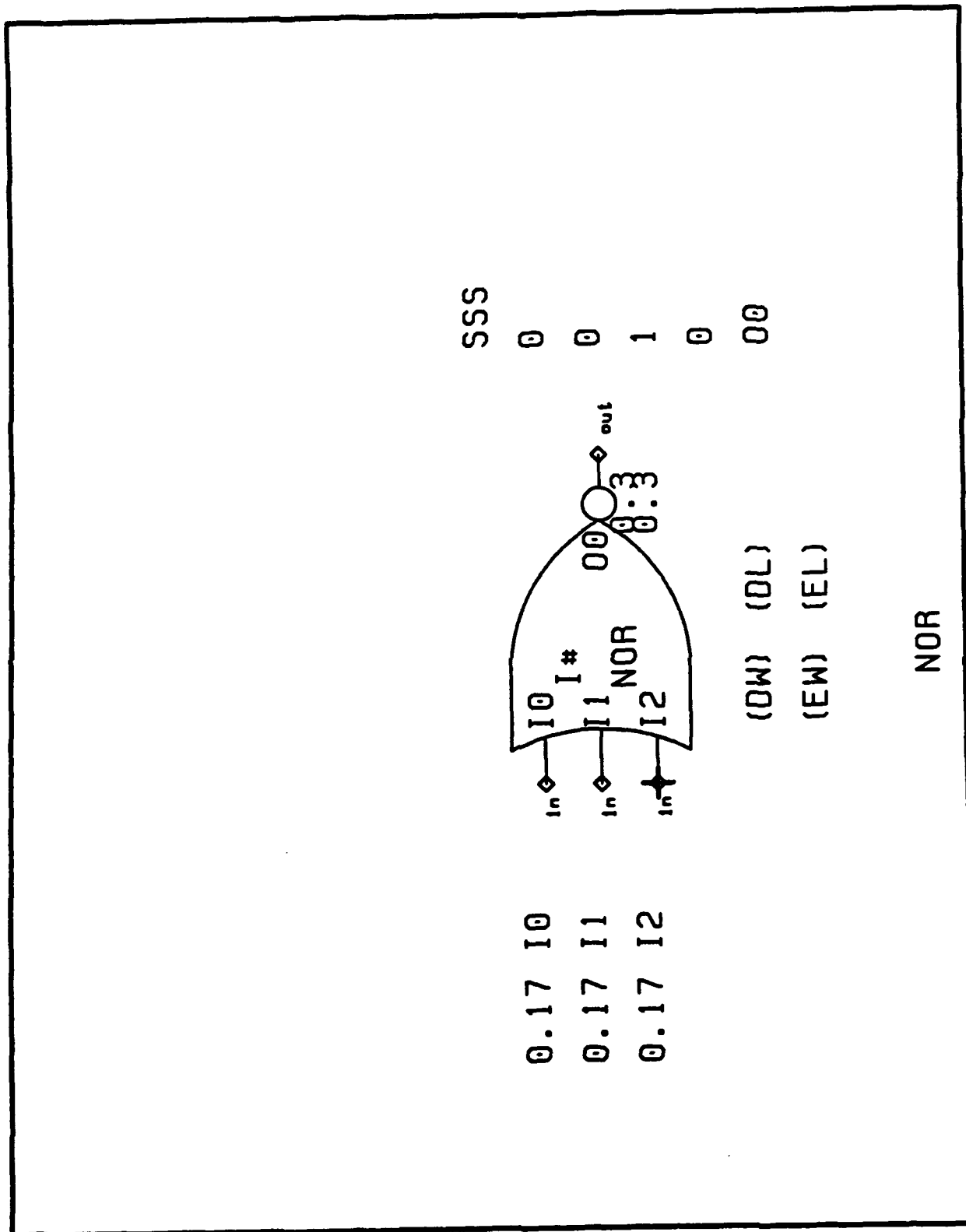


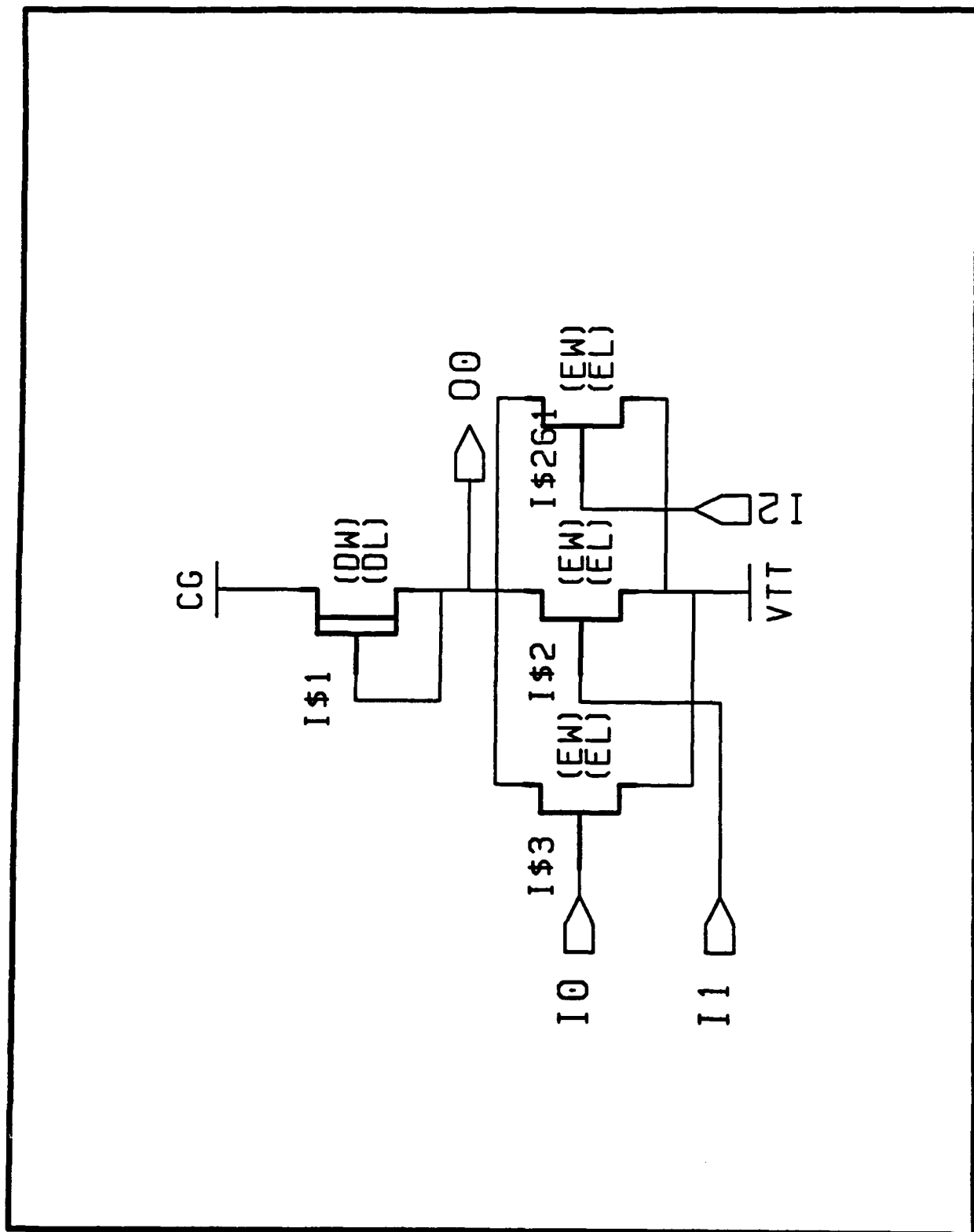




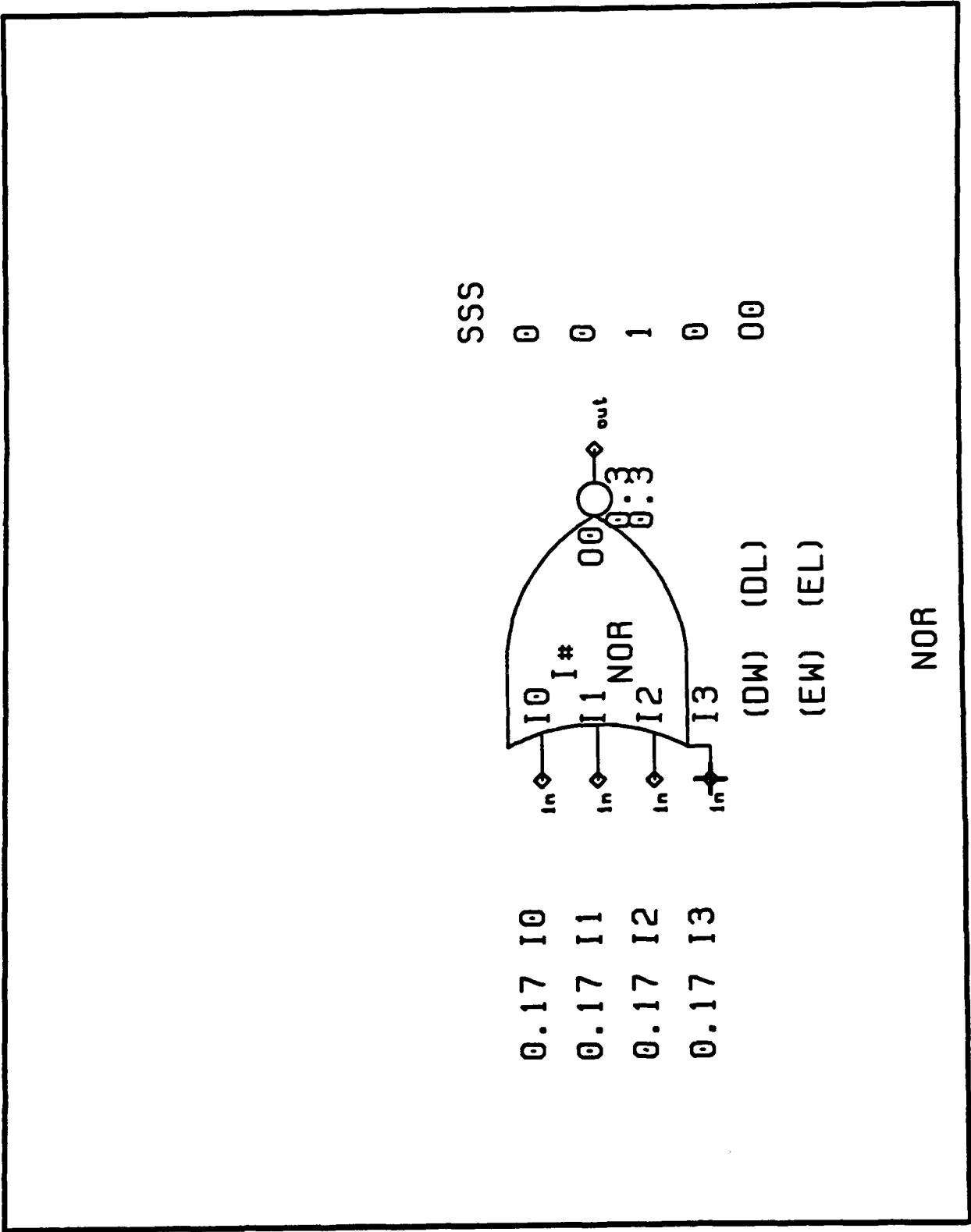


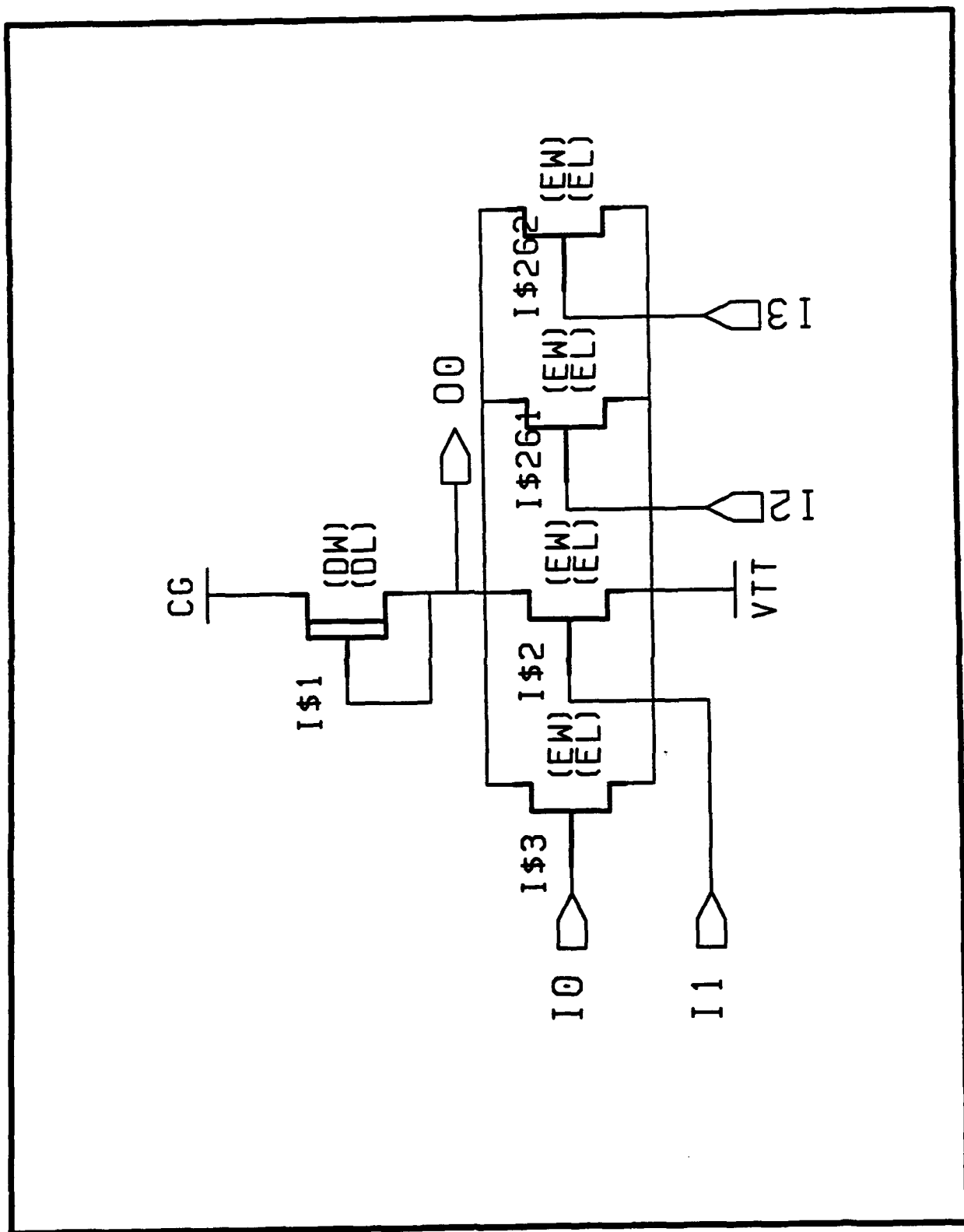


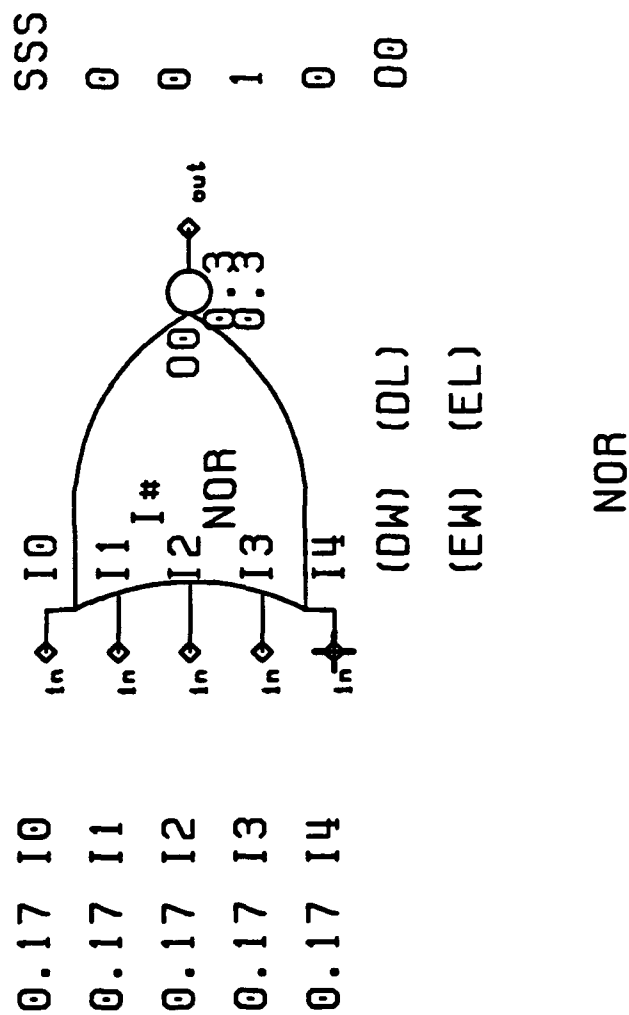


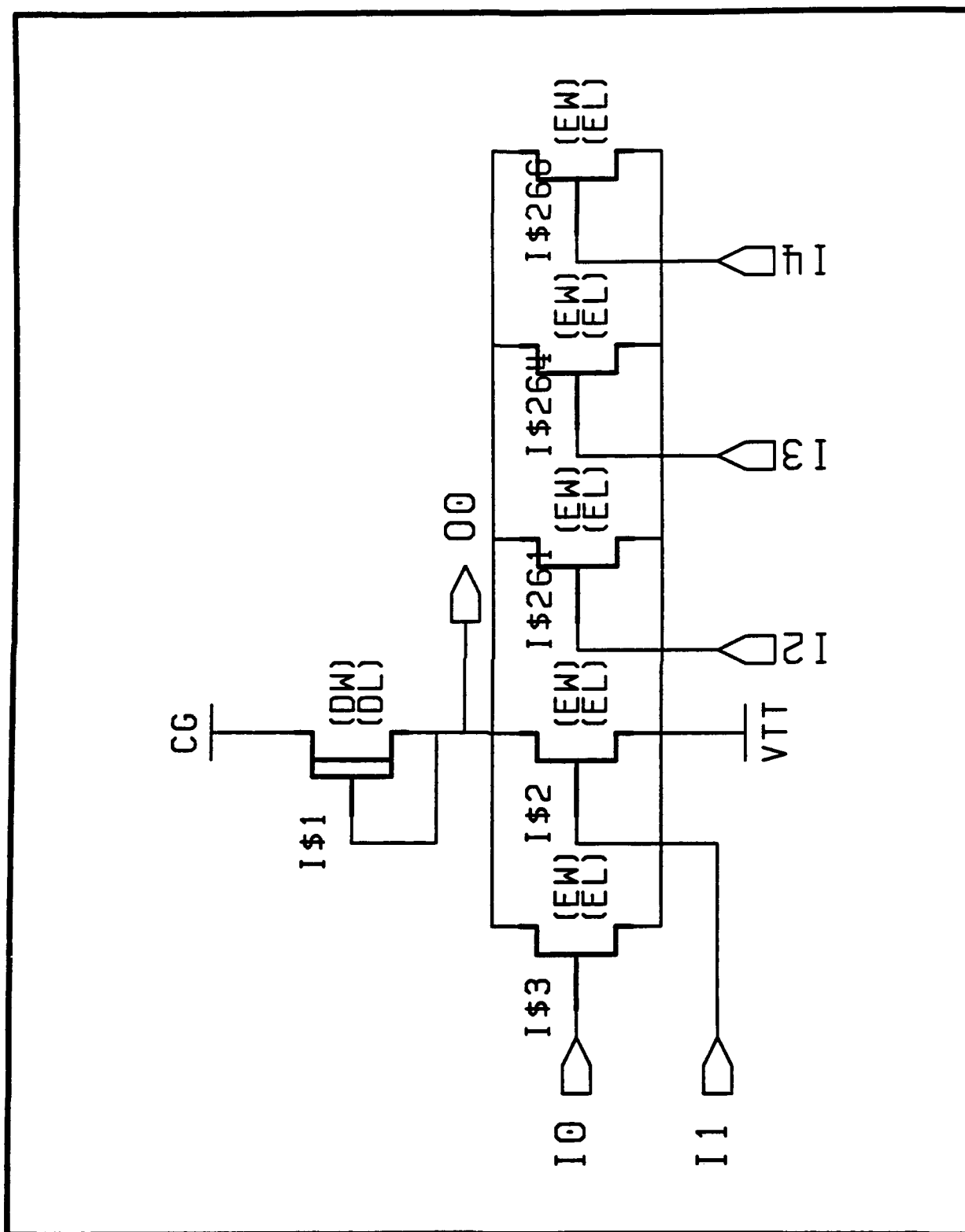


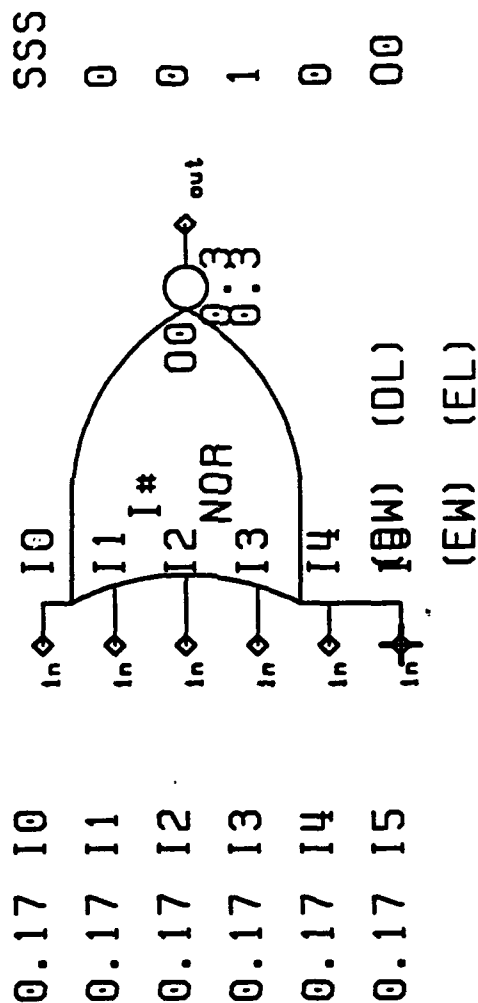


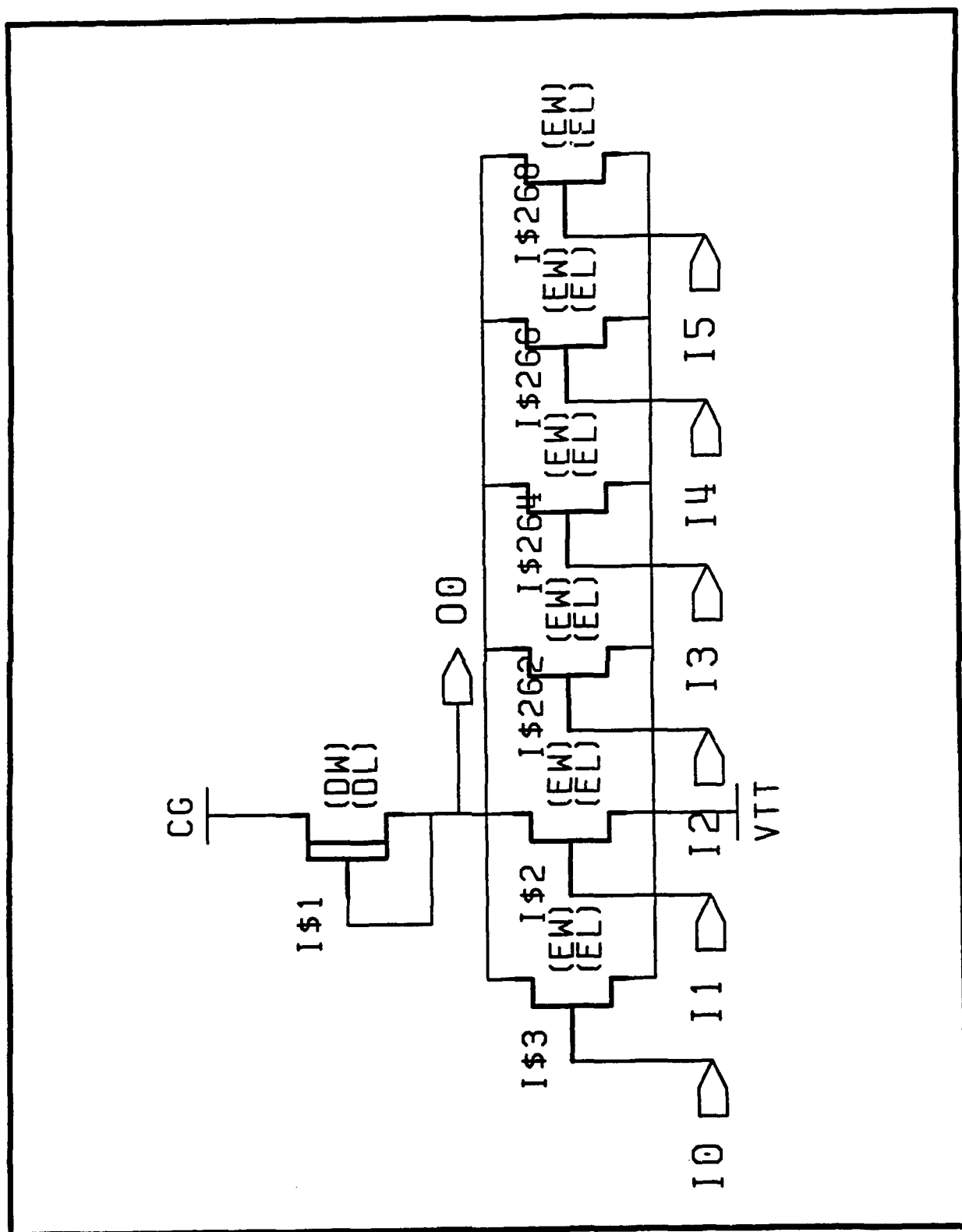


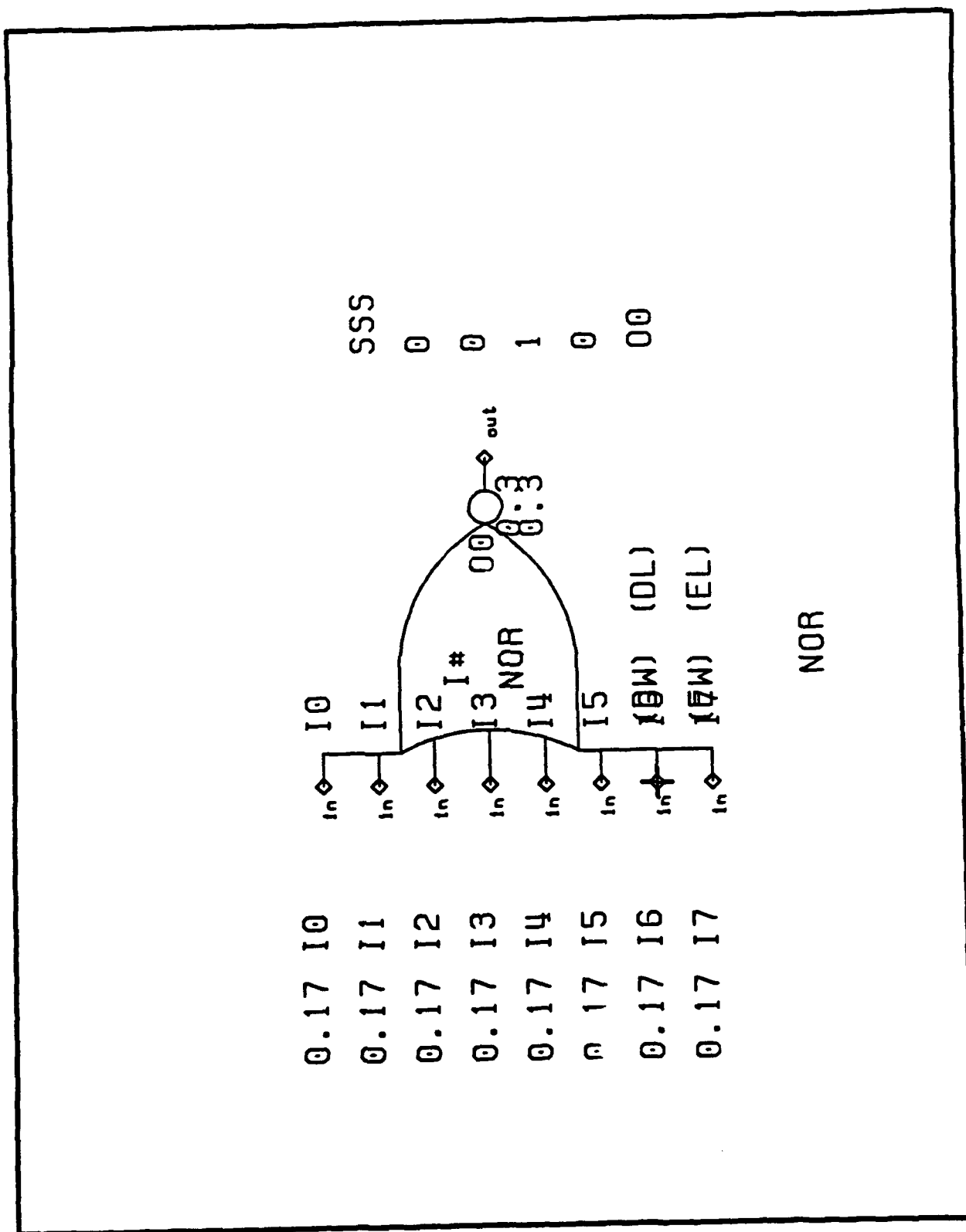


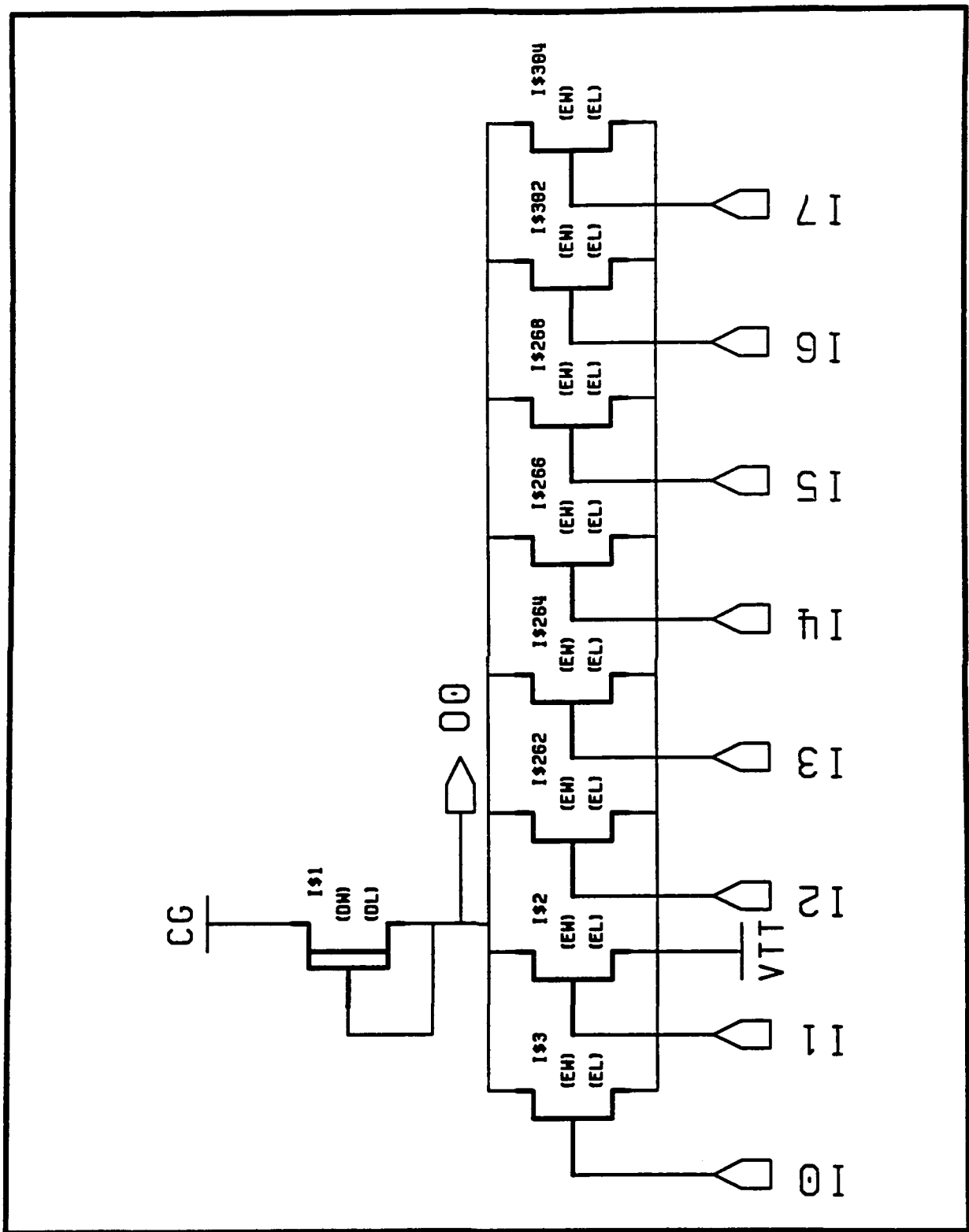






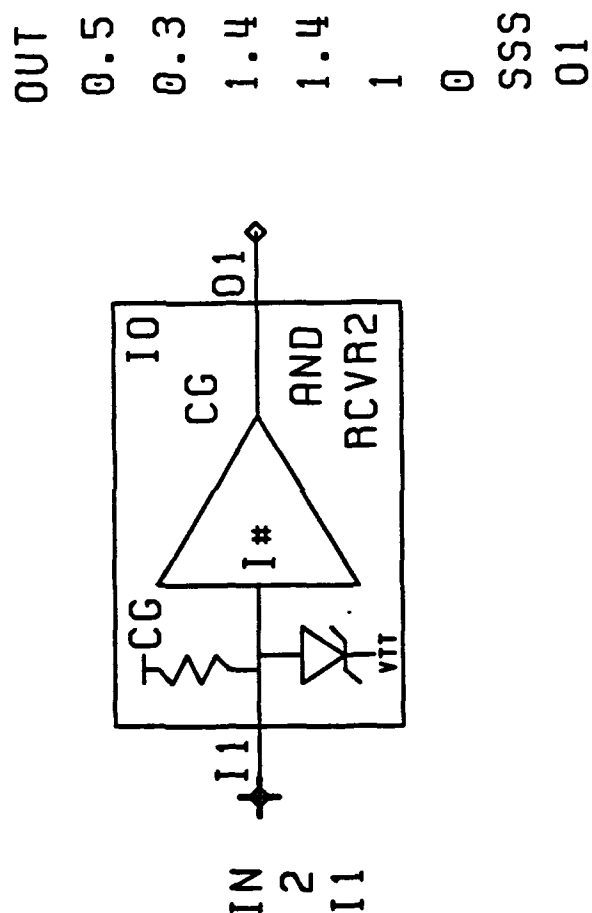


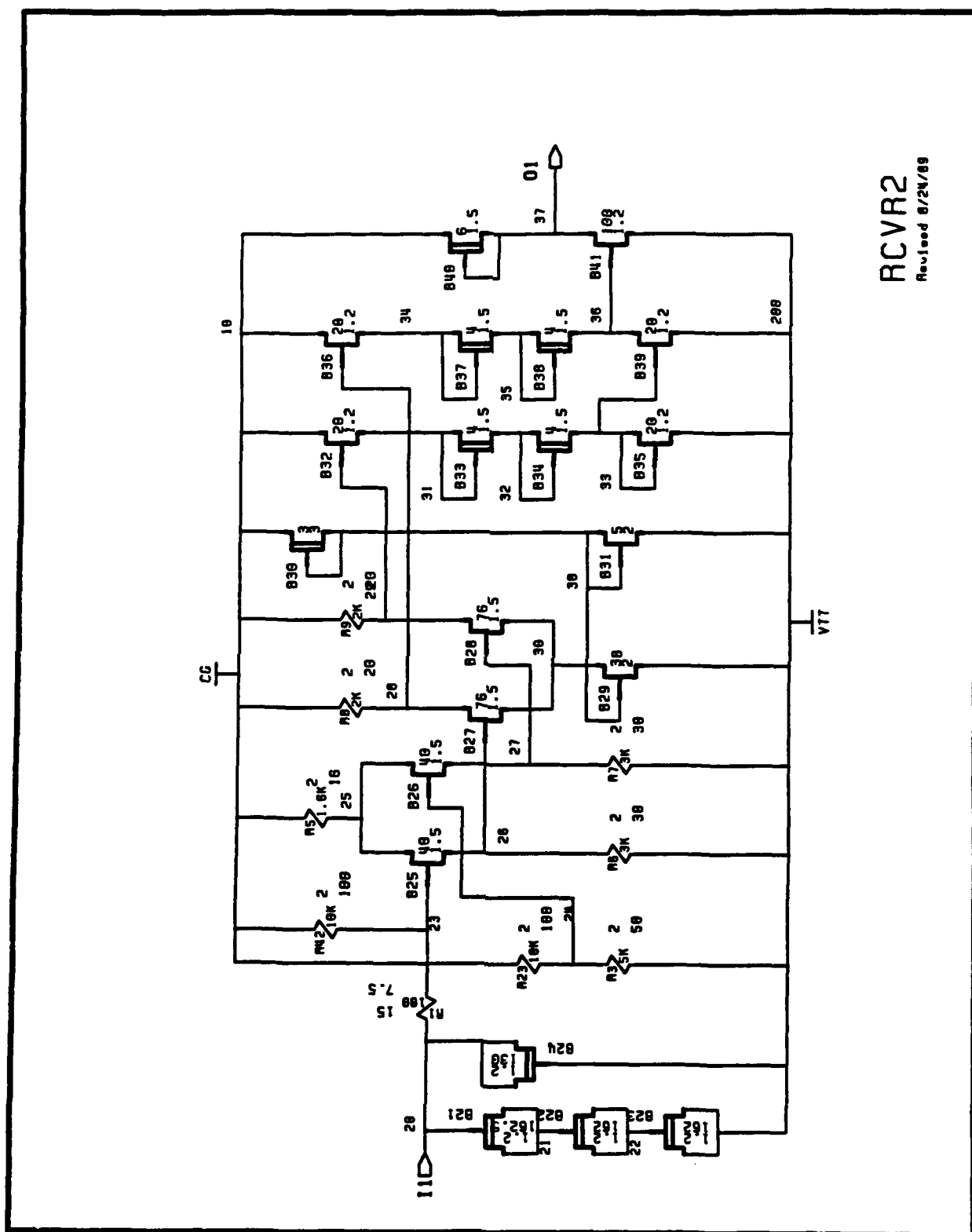




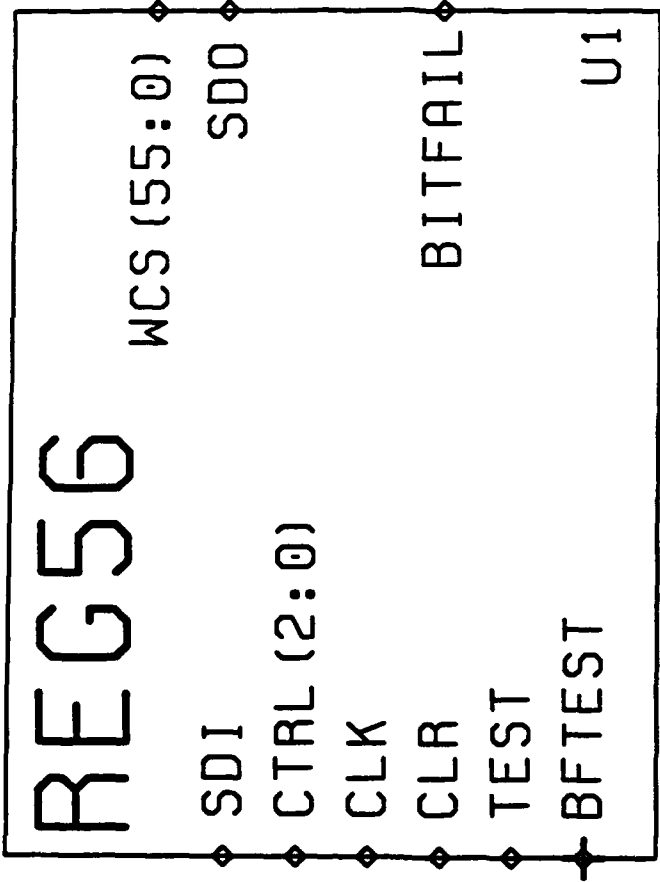


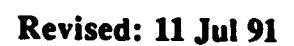
DESCRIPTION: LOW POWER 2 VOLT RECEIVER WITH PAD

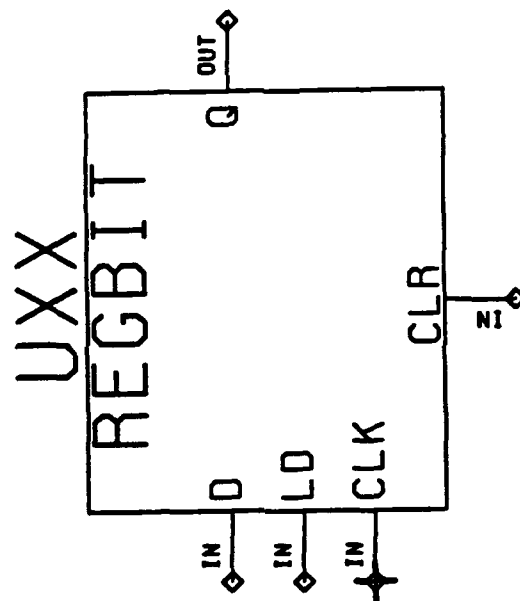


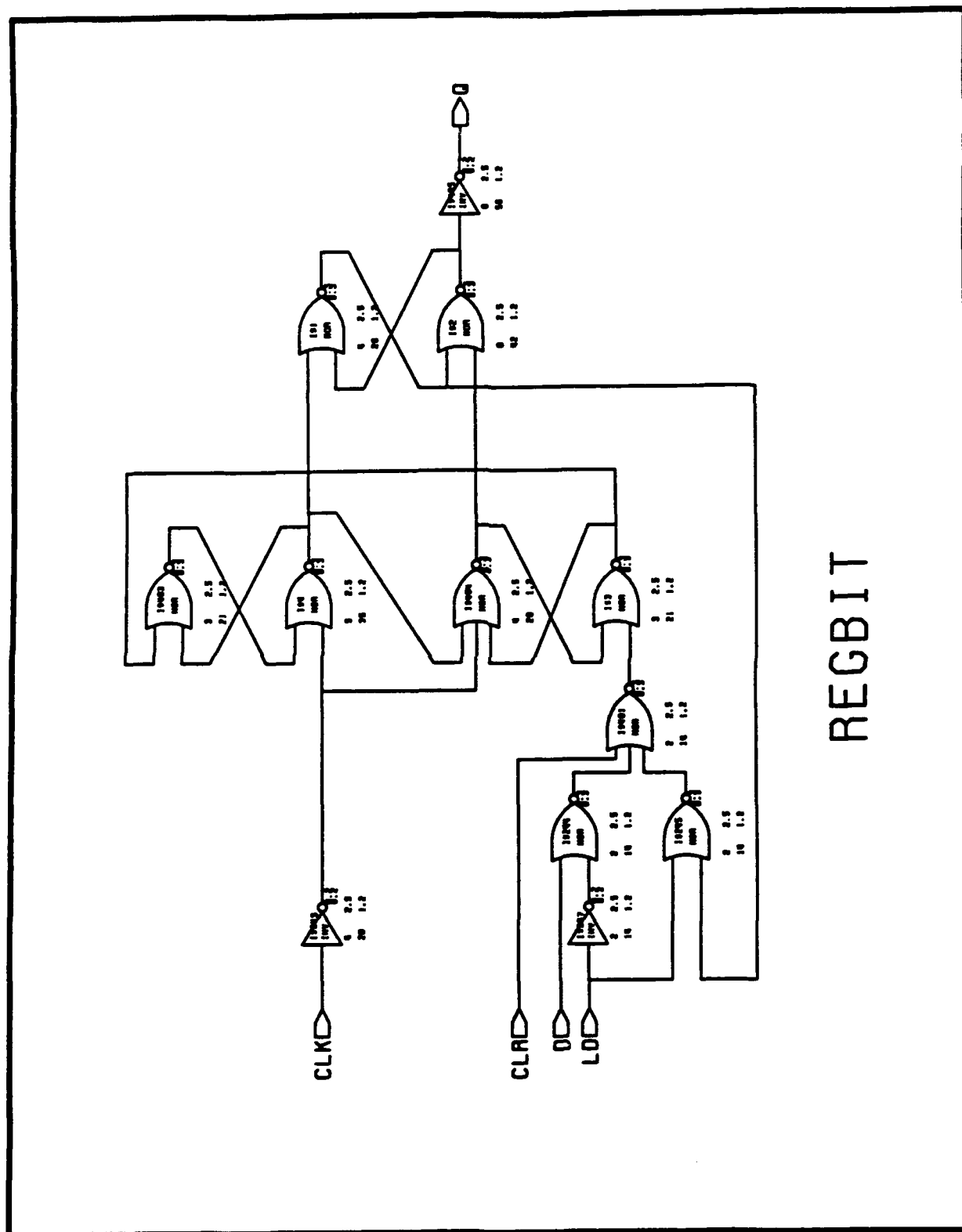


RCVR2  
Revised 8/24/88





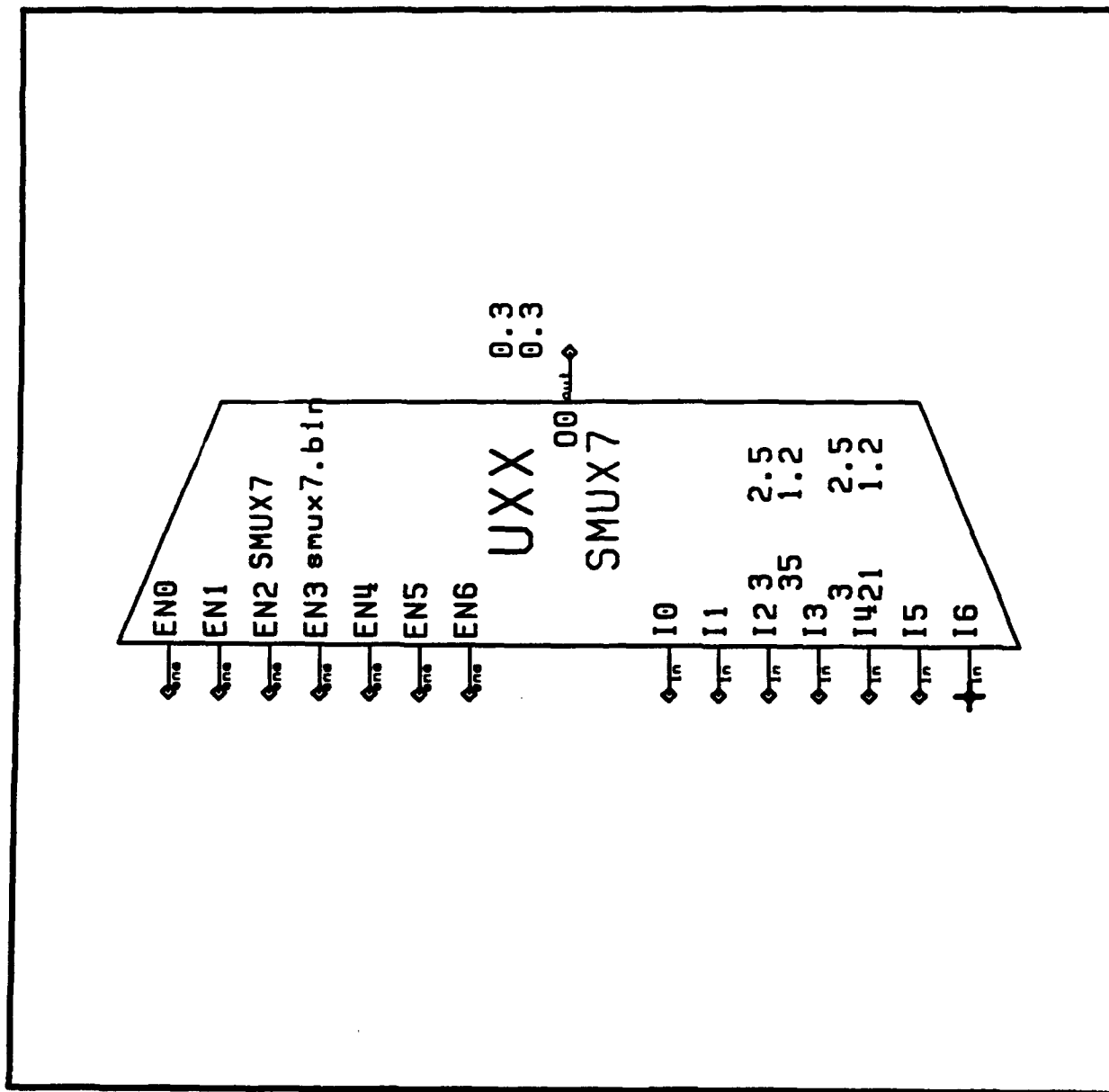


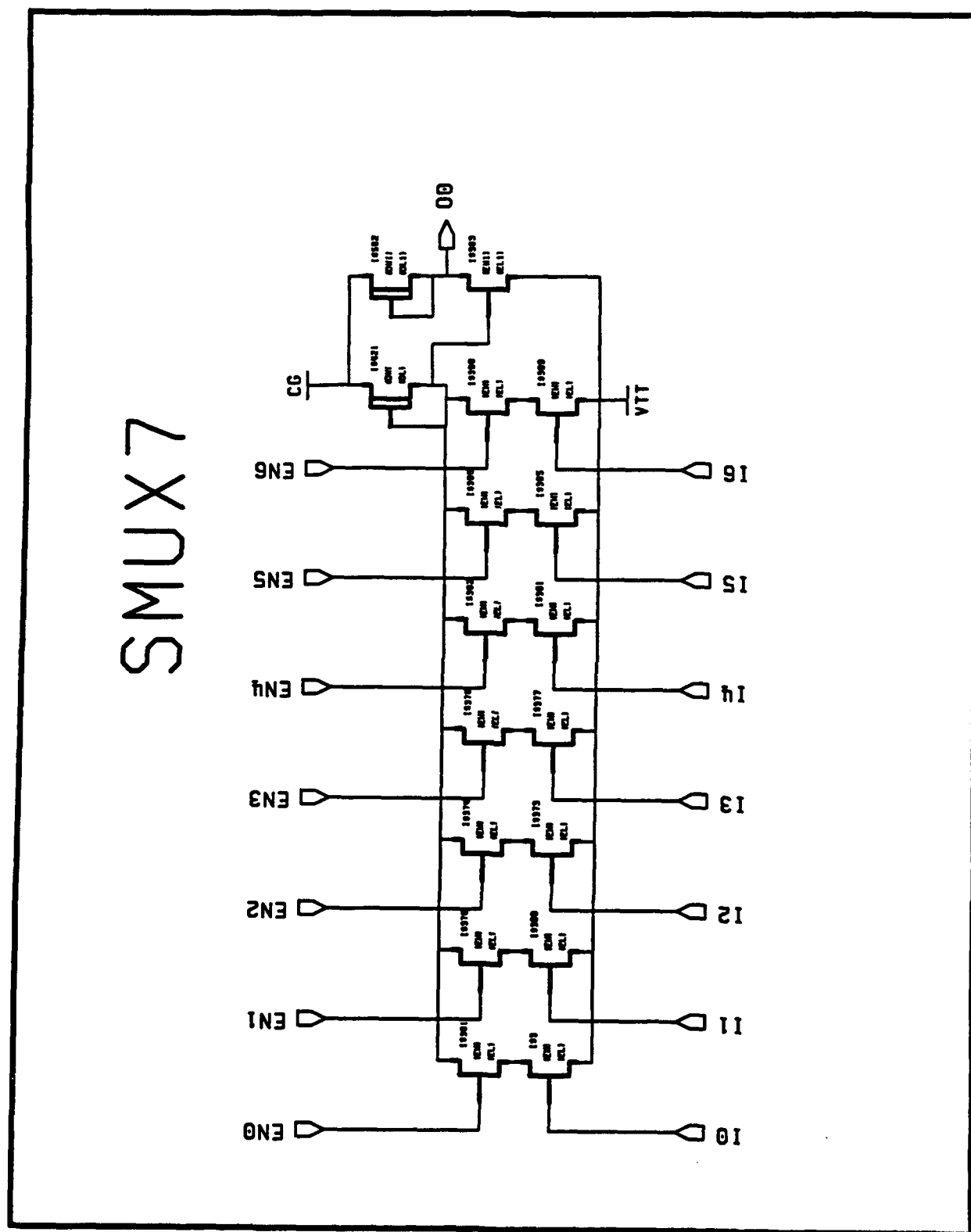


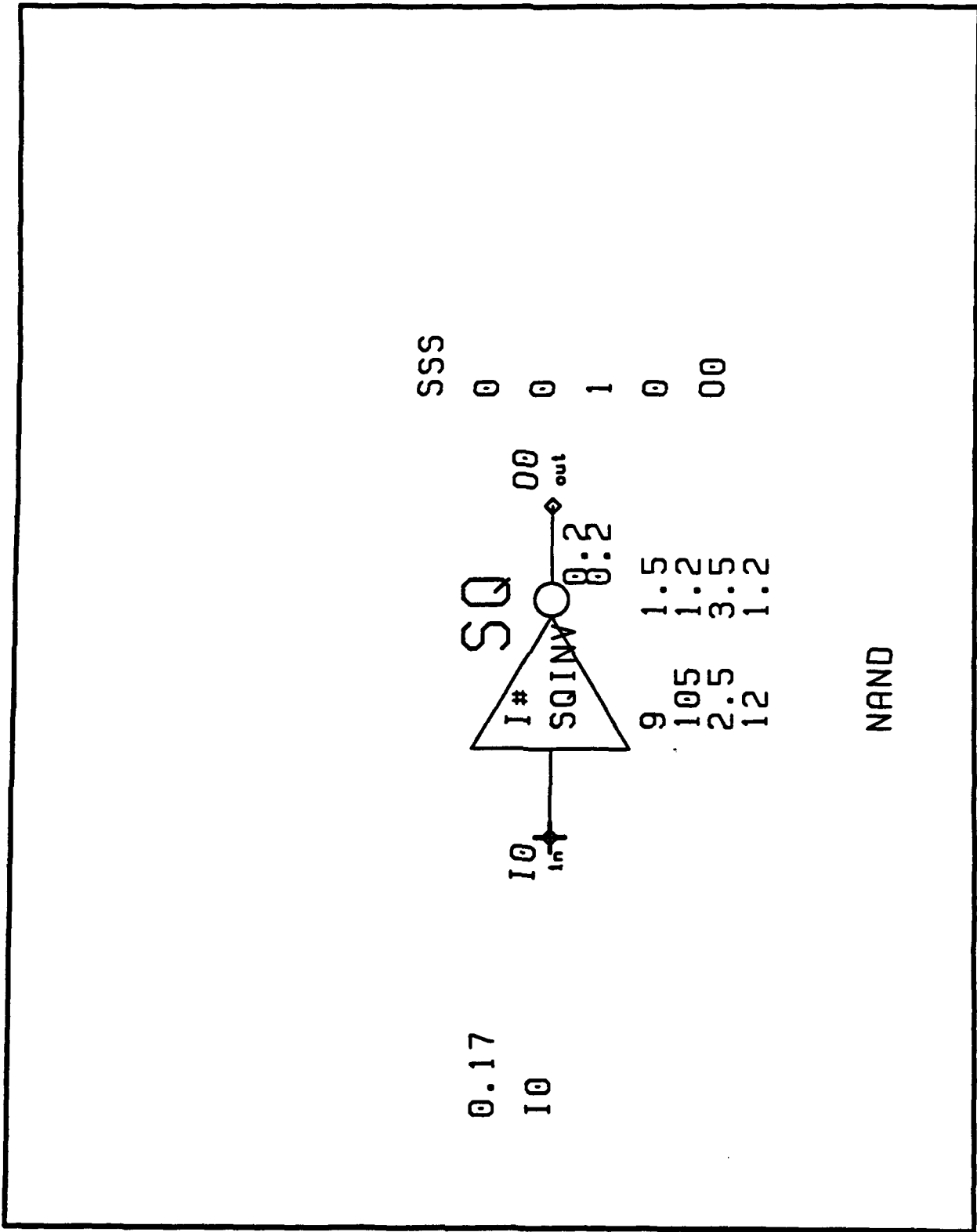


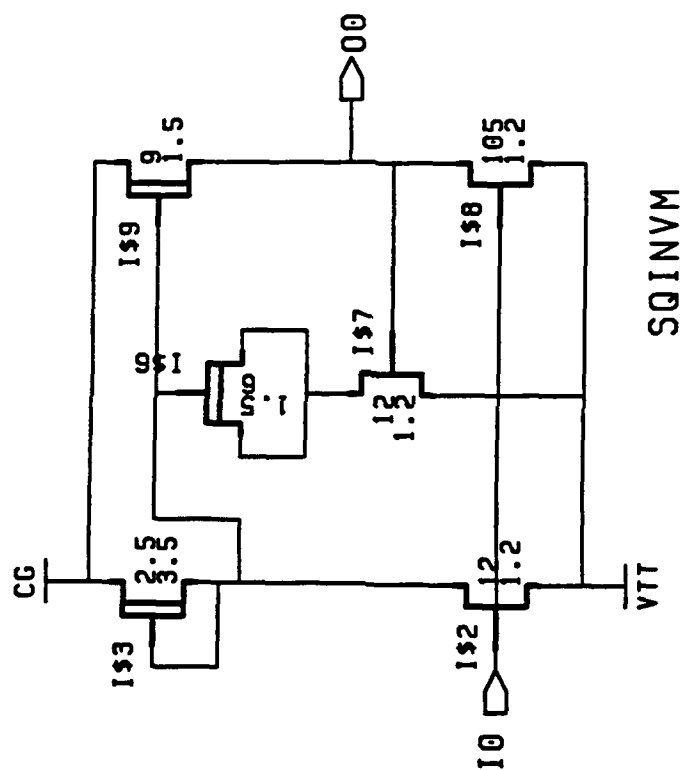


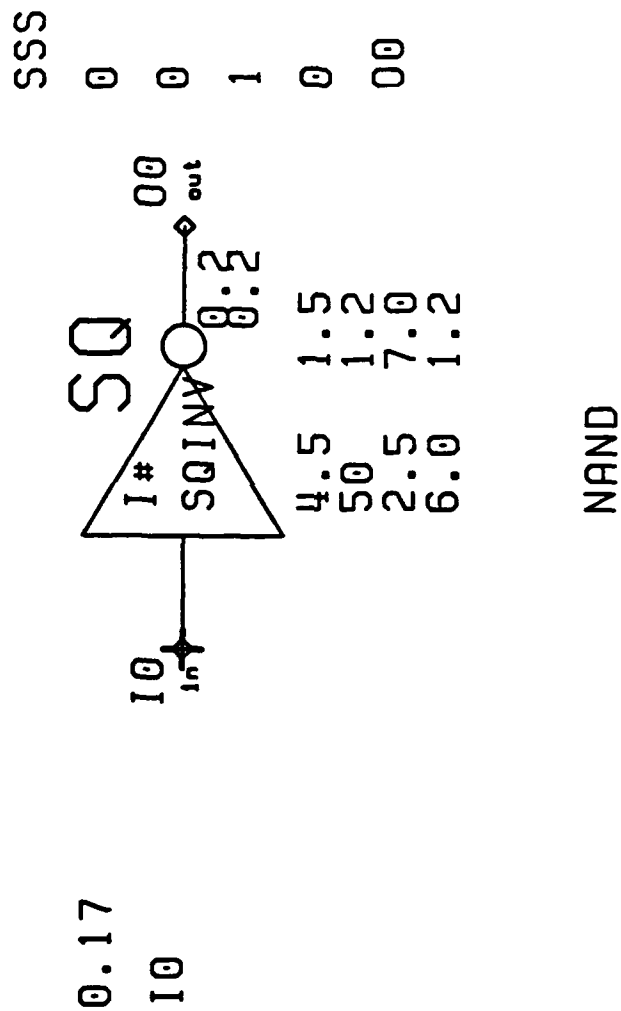


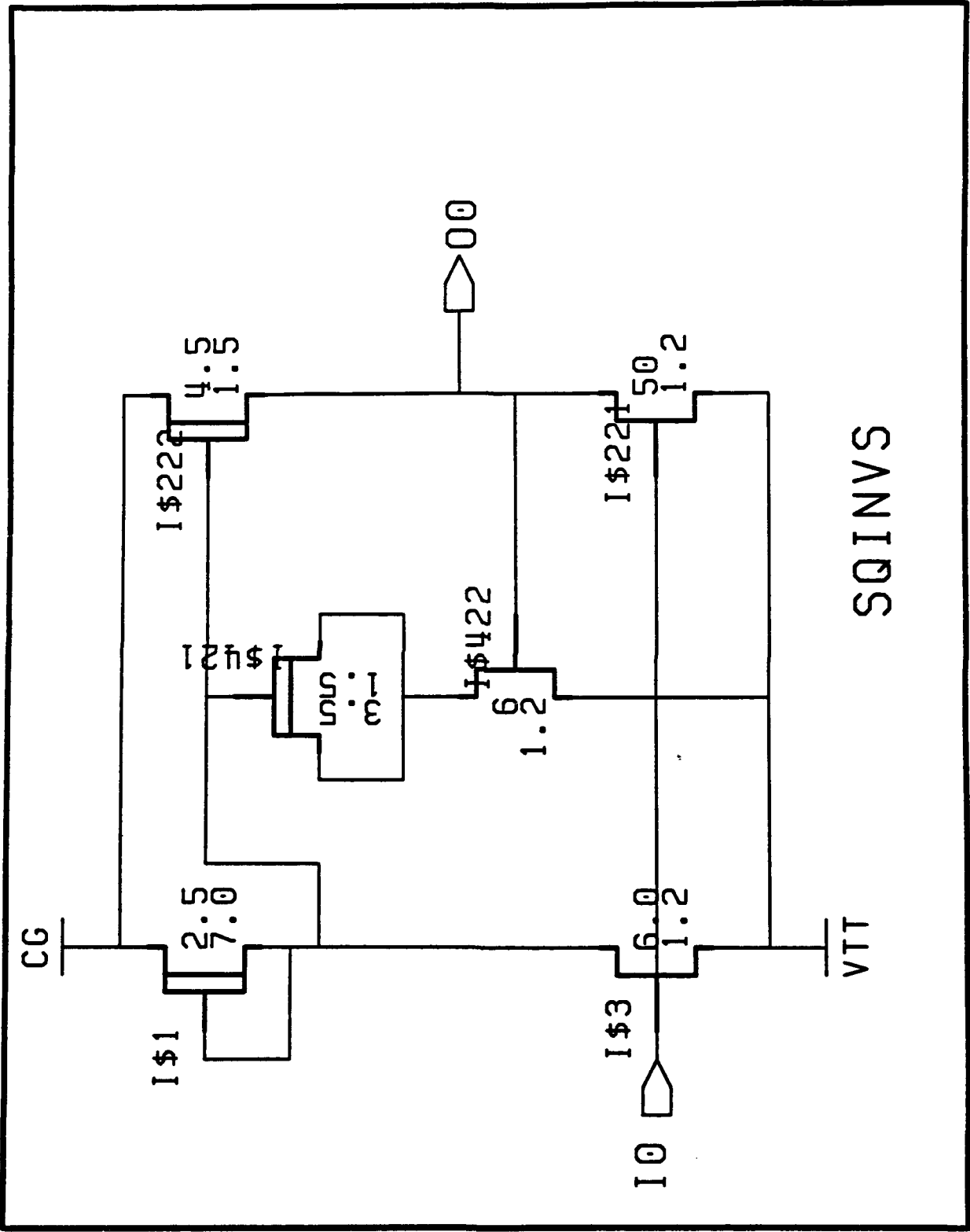


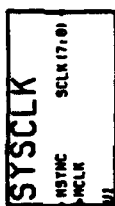






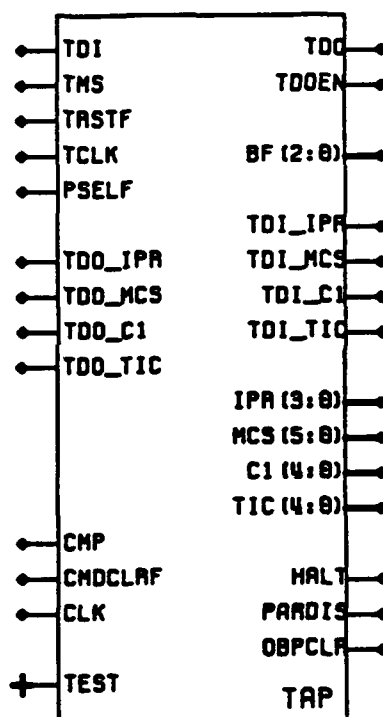




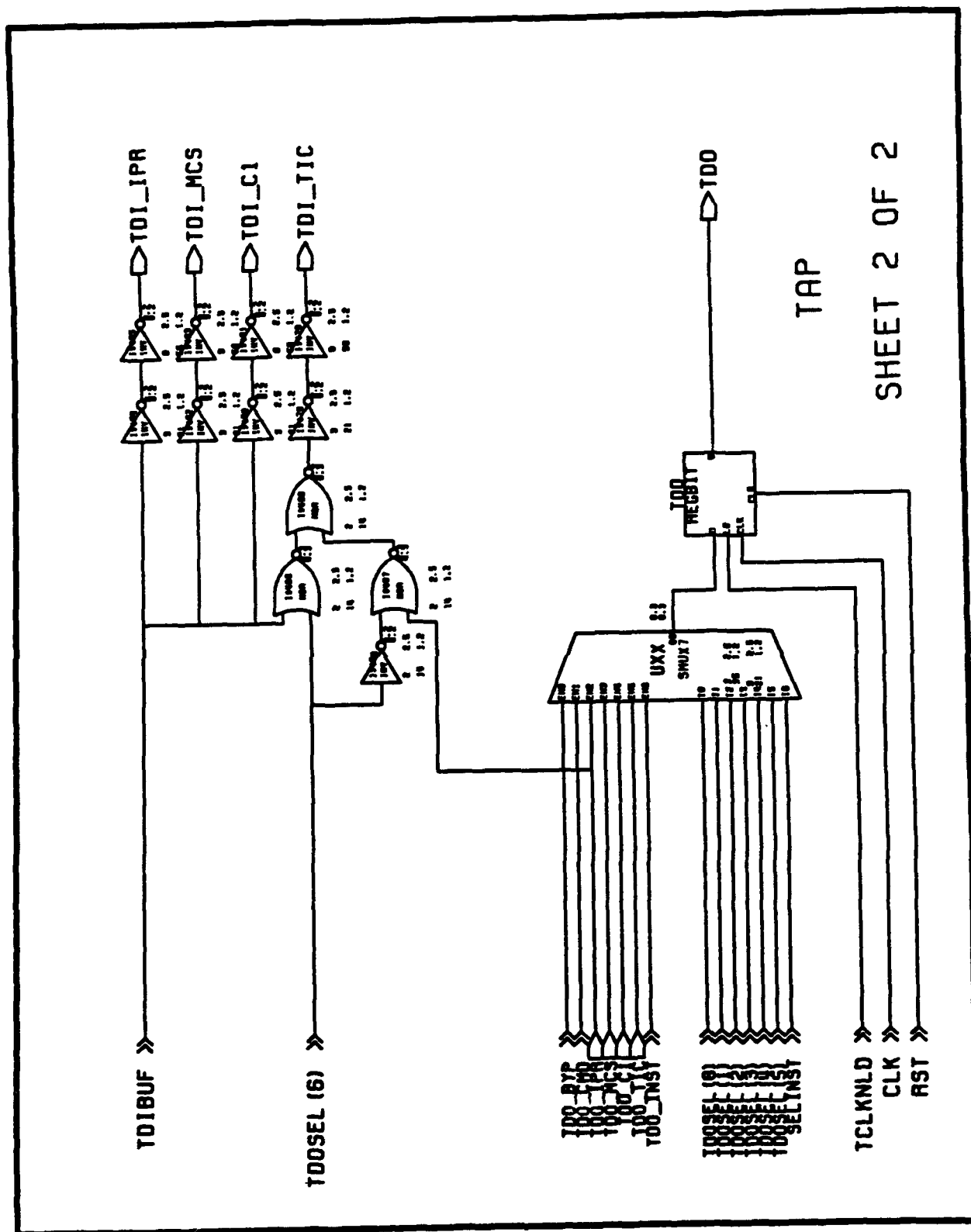


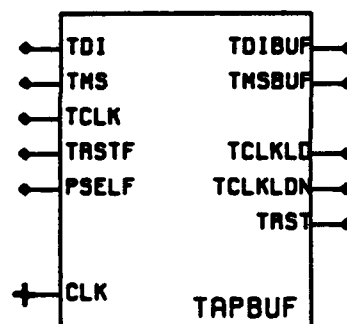


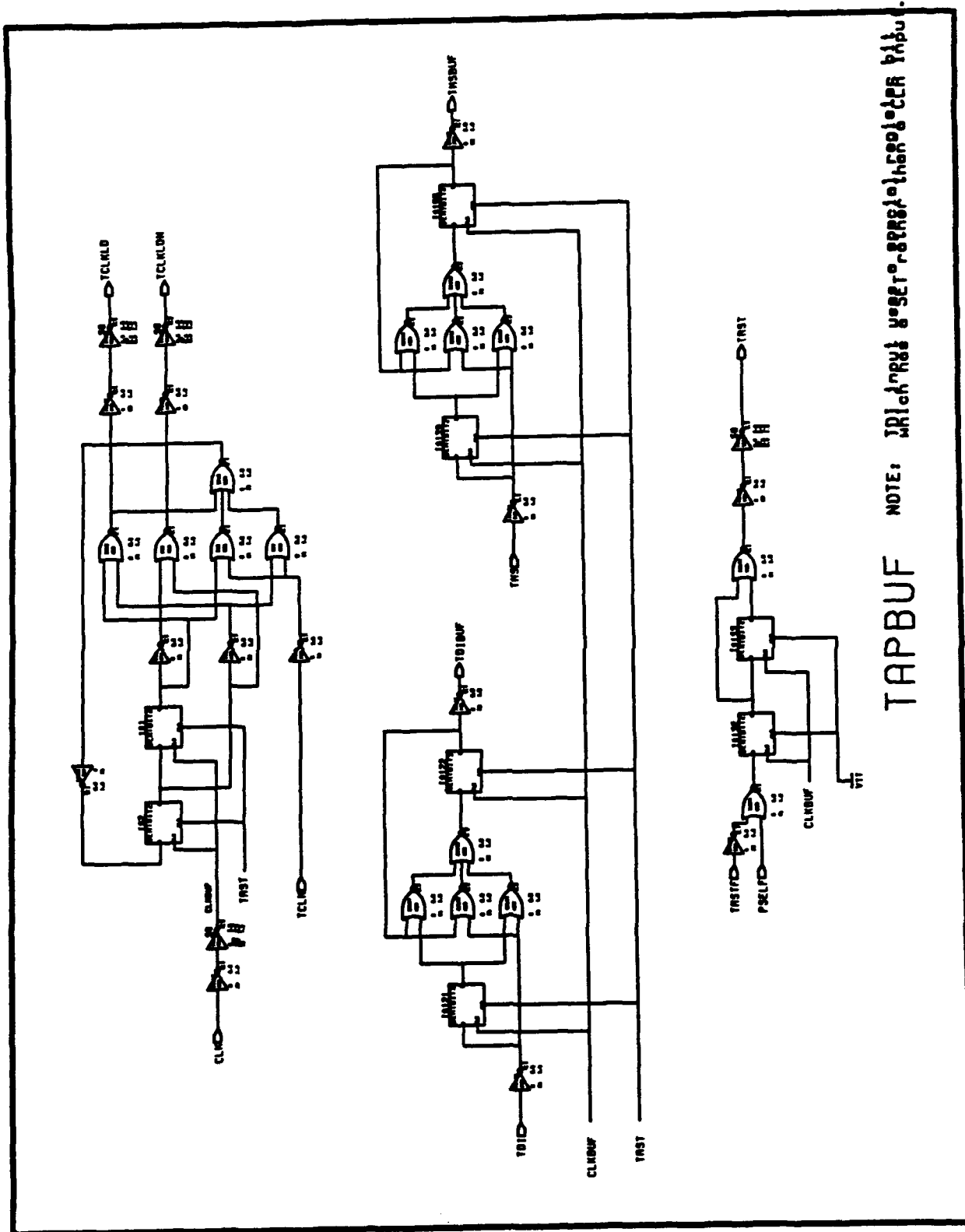


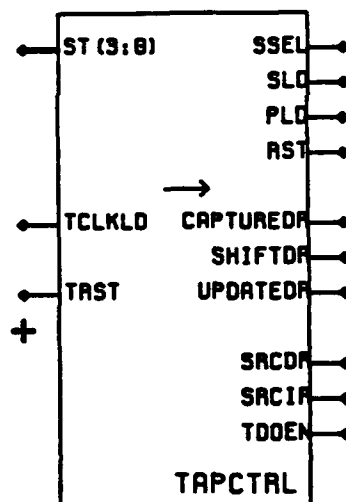




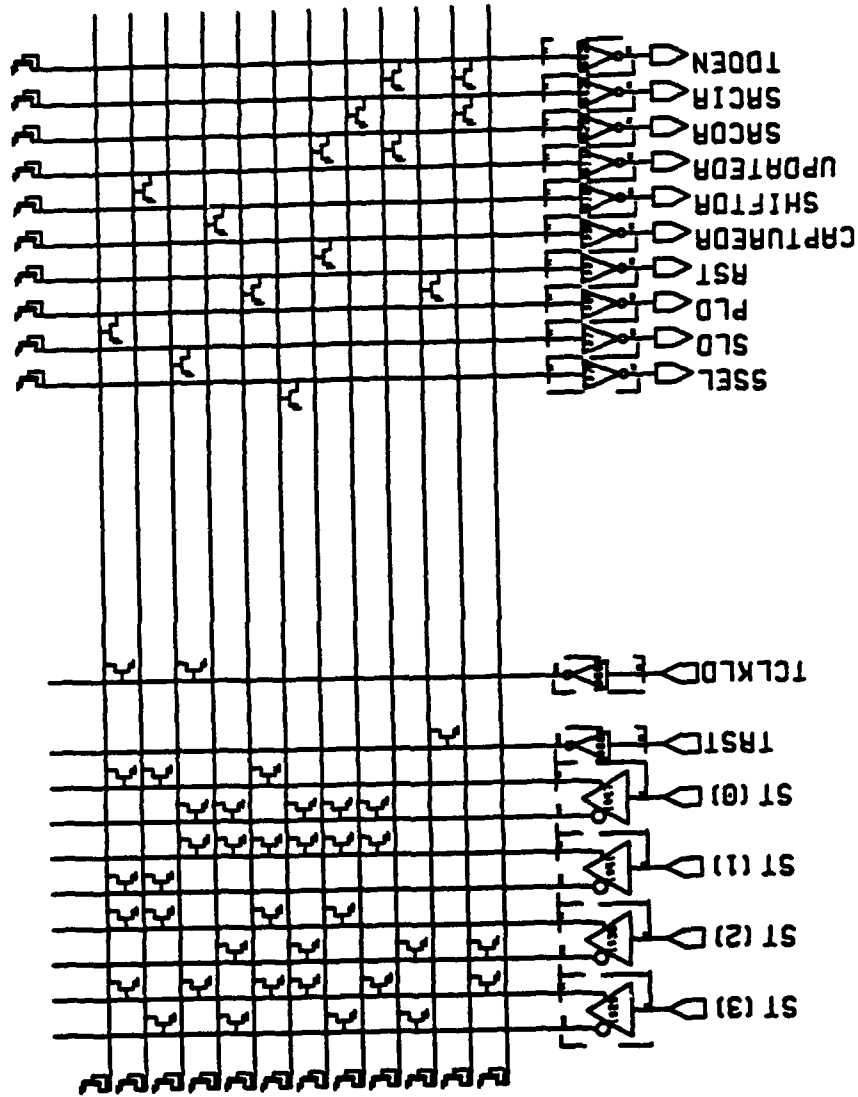


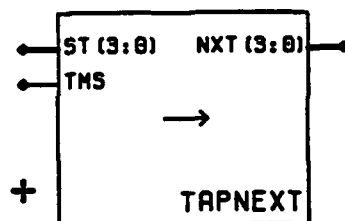




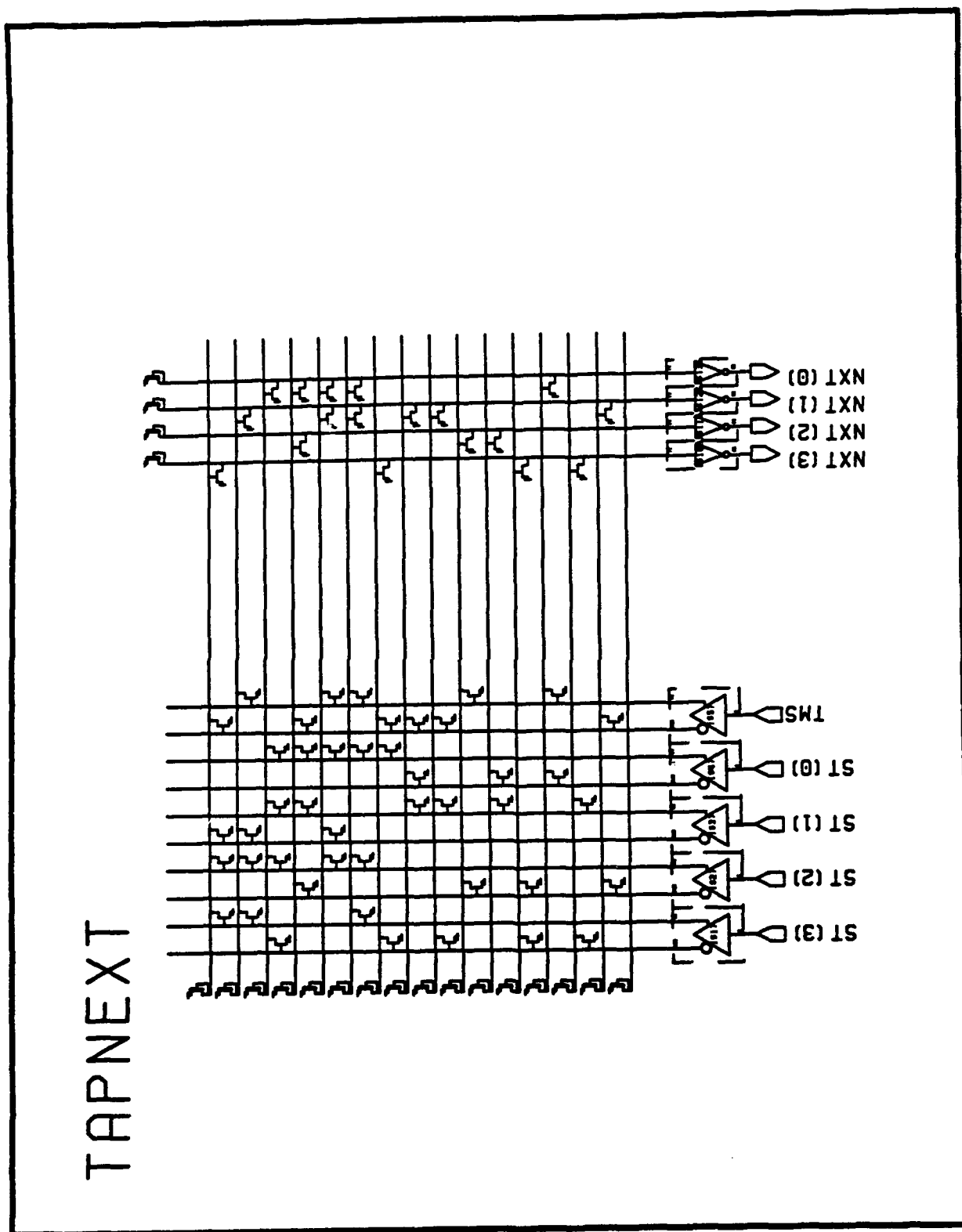


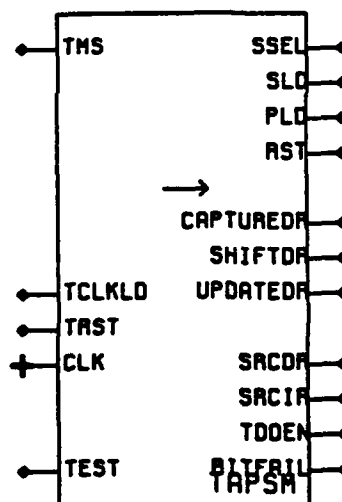
# TAPCTRL

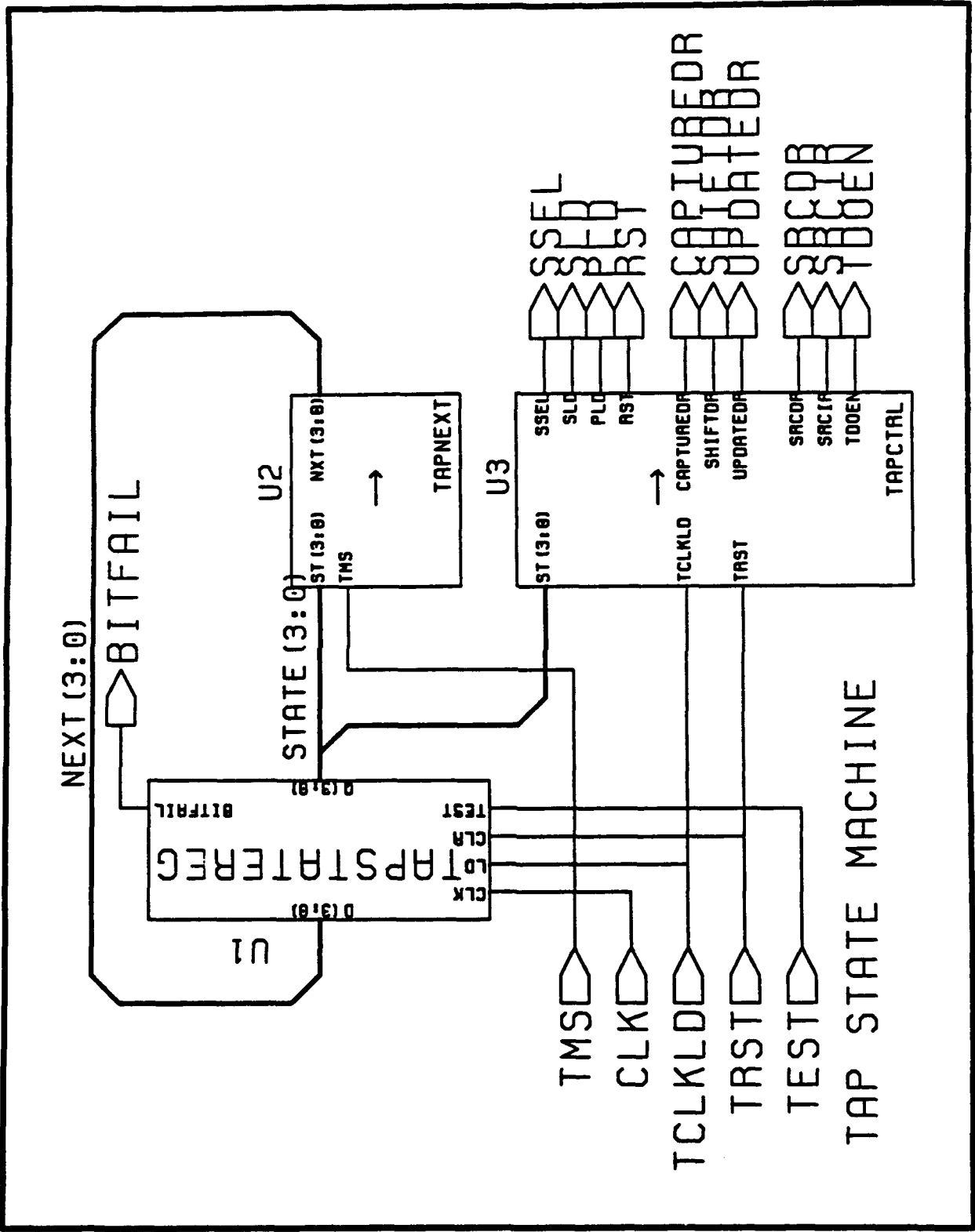


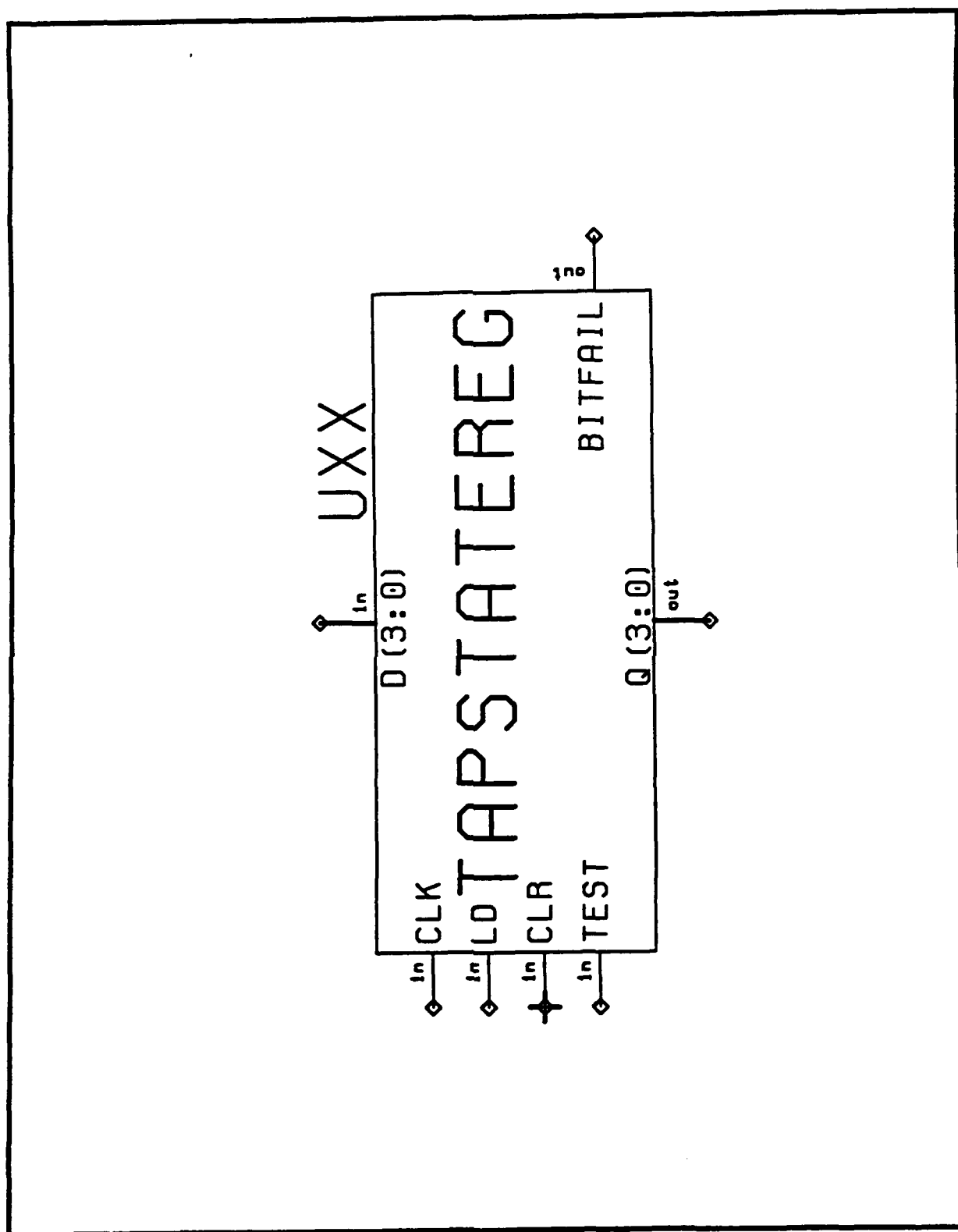


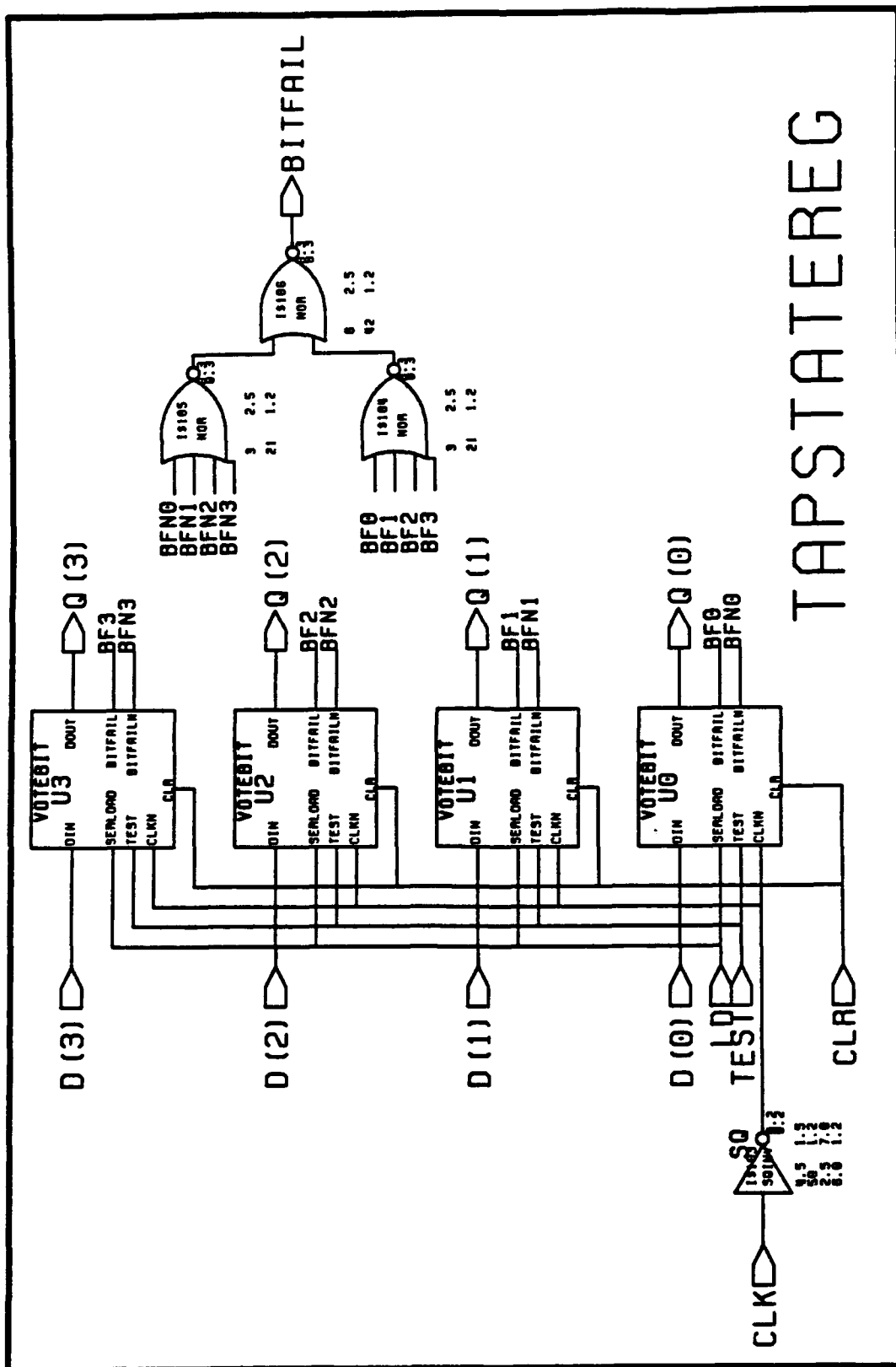








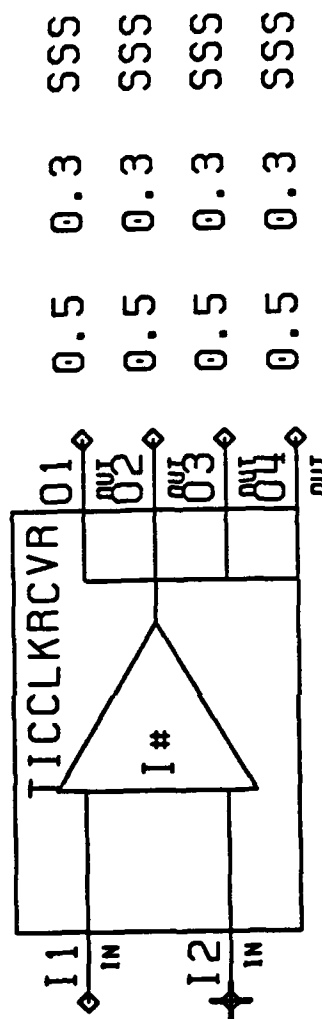




VITESSE GAAS CELL LIBRARY  
Version 0.8

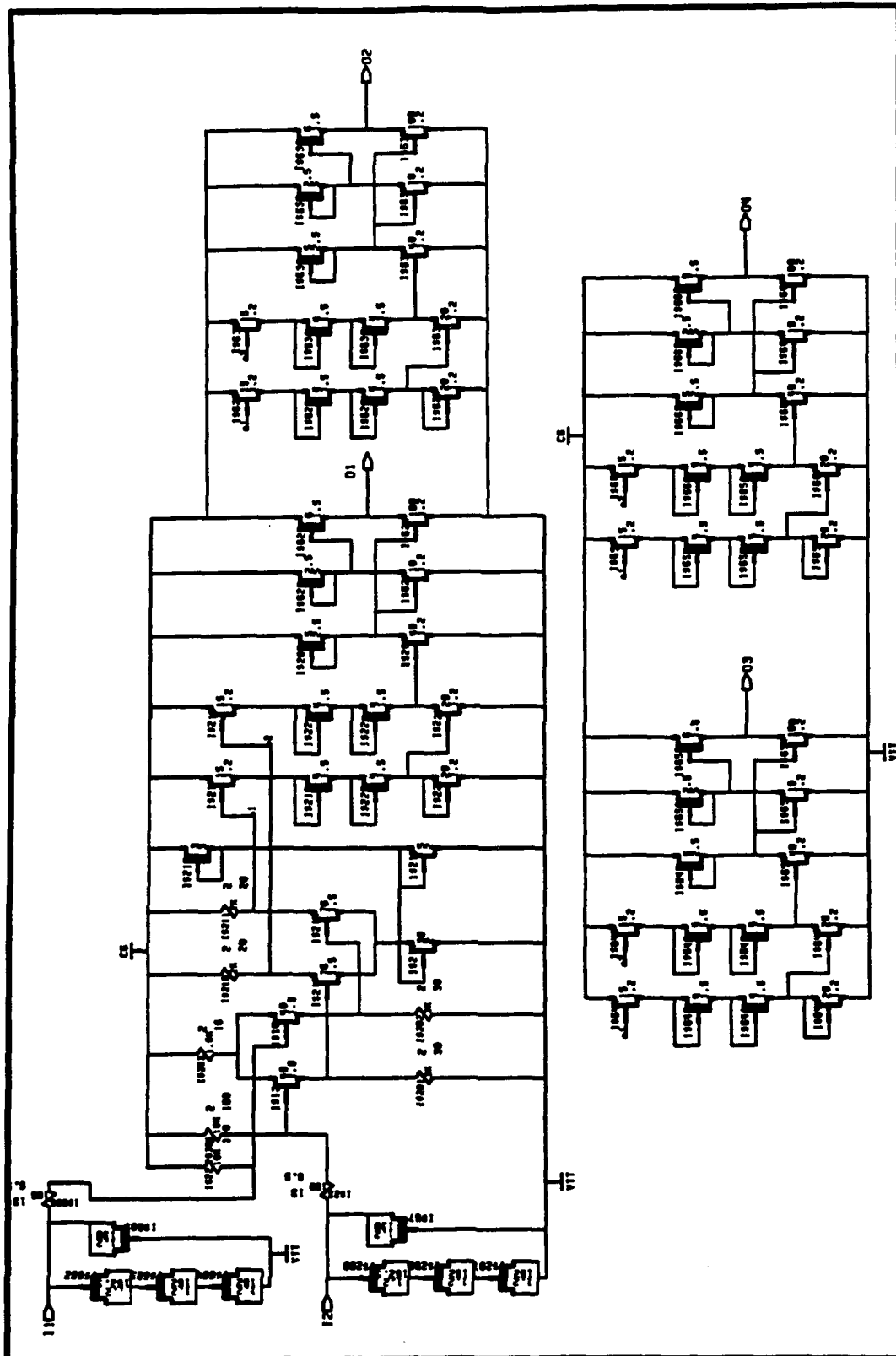
NAME: CLKRCVR

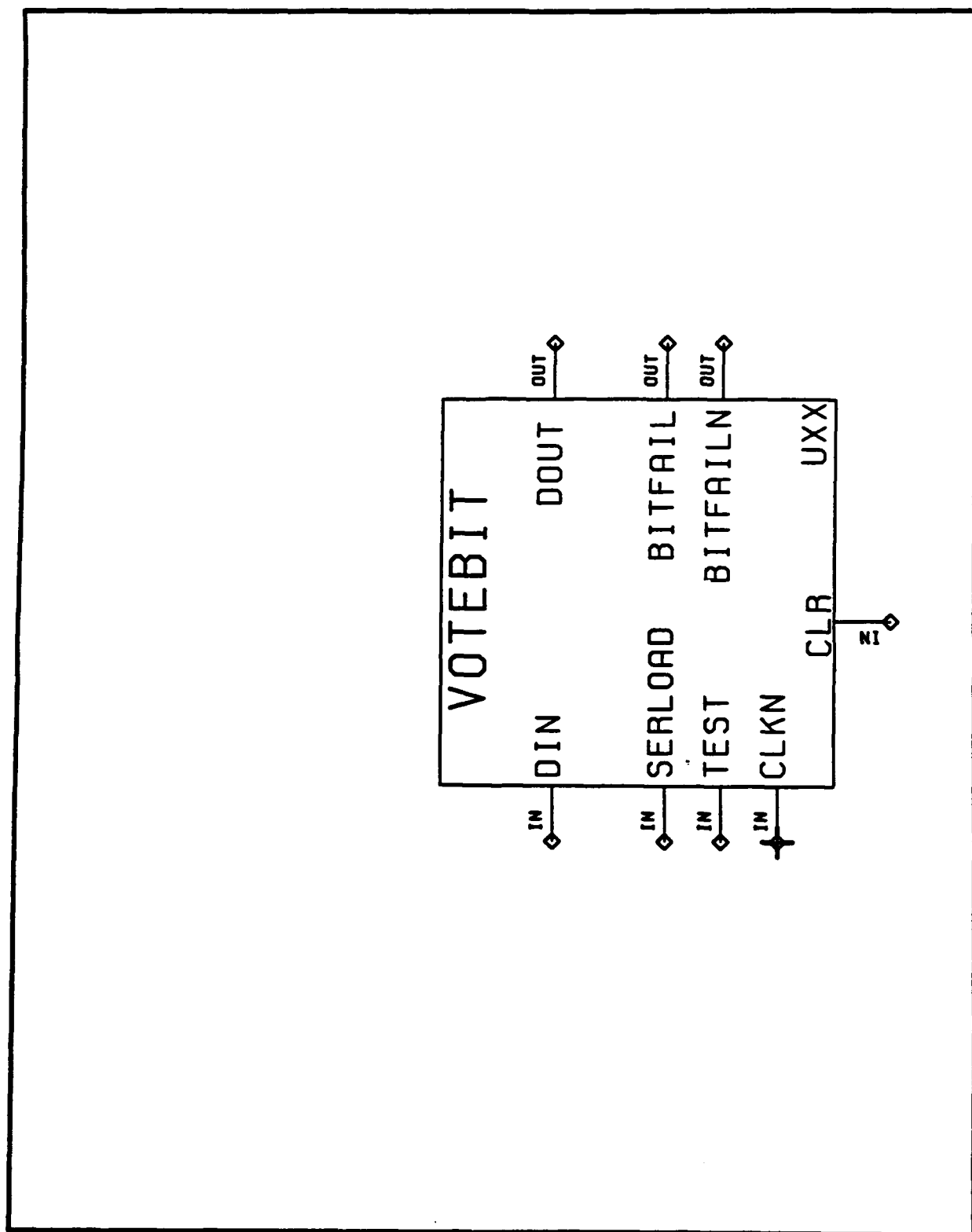
DESCRIPTION: DIFFERENTIAL INPUT CLOCK RECEIVER



TICCLKRCVR

ticclkrcvr.bin







VOTE BIT

